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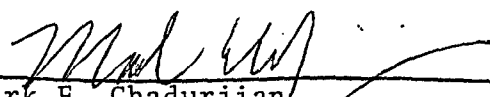
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Respectfully submitted,
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Serial No.:

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For: THREE-DIMENSIONAL MULTICHIP PACKAGES AND METHODS OF
FABRICATION

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THREE-DIMENSIONAL MULTICHIP
PACKAGES AND METHODS OF FABRICATION

Background of the Invention

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Technical Field

The present invention relates in general to high density electronic packaging which permits optimization of the number of circuit elements to be included in a given volume. More particular, the present invention relates to a method for fabricating a three-dimensional multichip package having a densely stacked array of semiconductor chips interconnected at least partially by means of a plurality of metallized trenches in the semiconductor chips.

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Description of the Prior Art

Since the development of integrated circuit technology, computers and computer storage devices have been made from wafers of semiconductor material comprising a plurality of integrated circuits. After a wafer is made, the circuits are typically separated from each other by dicing the wafer into small chips. Thereafter, the chips are bonded to carriers of various types, interconnected by wires and packaged. Along with being time consuming, costly and

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unreliable, the process of physically attaching wires to interconnect chips often produces undesirable signal delays, especially as the frequency of device operation increases.

5 As an improvement over this traditional
technology, stack or packages of multiple
semiconductor chips have become popular, e.g.,
reference U.S. Patent No. 4,525,921, entitled
"High-Density Electronic Processing
10 Package - Structure and Fabrication." Figure 1
depicts a typical semiconductor chip stack, generally
denoted 10, consisting of multiple integrated circuit
chips 12 which are adhesively secured together. A
metallization pattern 14 is provided on one or more
15 sides of stack 10 for chip interconnections and for
electrical connection to circuitry external to the
stack. Metallization pattern 14 includes both
individual contacts 16 and bussed contacts 18. Stack
20 10, with metallization 14 thereon, is positioned on
the upper surface 21 of a substrate 20 which has its
own metallization pattern 22 thereon. Although
superior to the more conventional technique of
individually placing chips on a board, substrate or
multichip carrier, both in terms of reliability and
25 circuit performance, this multichip stack approach is
still susceptible to improvement in terms of density
and reduction in the length of chip wiring.
Obviously, any improvements in such package
characteristics will produce a lower cost, lower
30 power higher density, reliability and thereby
providing better performing device.

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