



US005202754A

United States Patent [19]

[11] Patent Number: **5,202,754**

Bertin et al.

[45] Date of Patent: **Apr. 13, 1993**

[54] THREE-DIMENSIONAL MULTICHIP PACKAGES AND METHODS OF FABRICATION

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[21] Appl. No.: **760,041**

[22] Filed: **Sep. 13, 1991**

[51] Int. Cl.⁵ **H01L 29/78; B44C 1/22**

[52] U.S. Cl. **257/684; 257/777; 257/723; 257/725**

[58] Field of Search **357/75, 80, 74, 71, 357/72**

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Primary Examiner—Eugene R. LaRoche

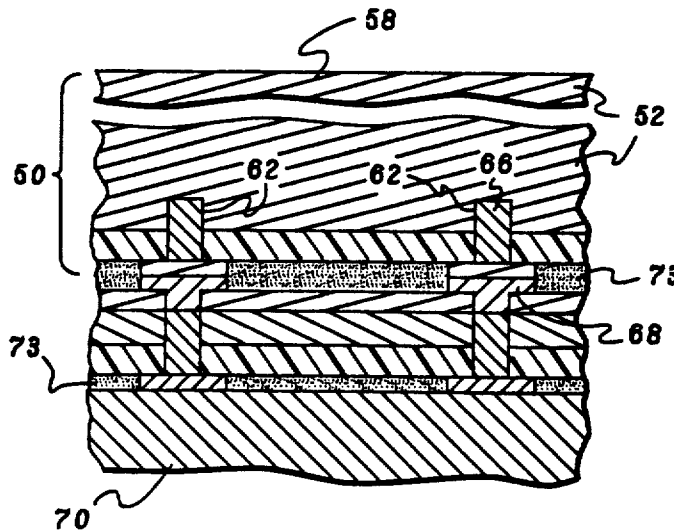
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[57] ABSTRACT

A fabrication method and resultant three-dimensional multichip package having a densely stacked array of semiconductor chips interconnected at least partially by means of a plurality of metallized trenches are disclosed. The fabrication method includes providing an integrated circuit chip having high aspect ratio metallized trenches therein extending from a first surface to a second surface thereof. An etch stop layer is provided proximate the termination position of the metallized trenches with the semiconductor substrate. Next the integrated circuit device is affixed to a carrier such that the surface of the supporting substrate is exposed and substrate is thinned from the integrated circuit device until exposing at least some of the plurality of metallized trenches therein. Electrical contact can thus be made to the active layer of the integrated circuit chip via the exposed metallized trenches. Specific details of the fabrication method and the resultant multichip package are set forth.

6 Claims, 8 Drawing Sheets



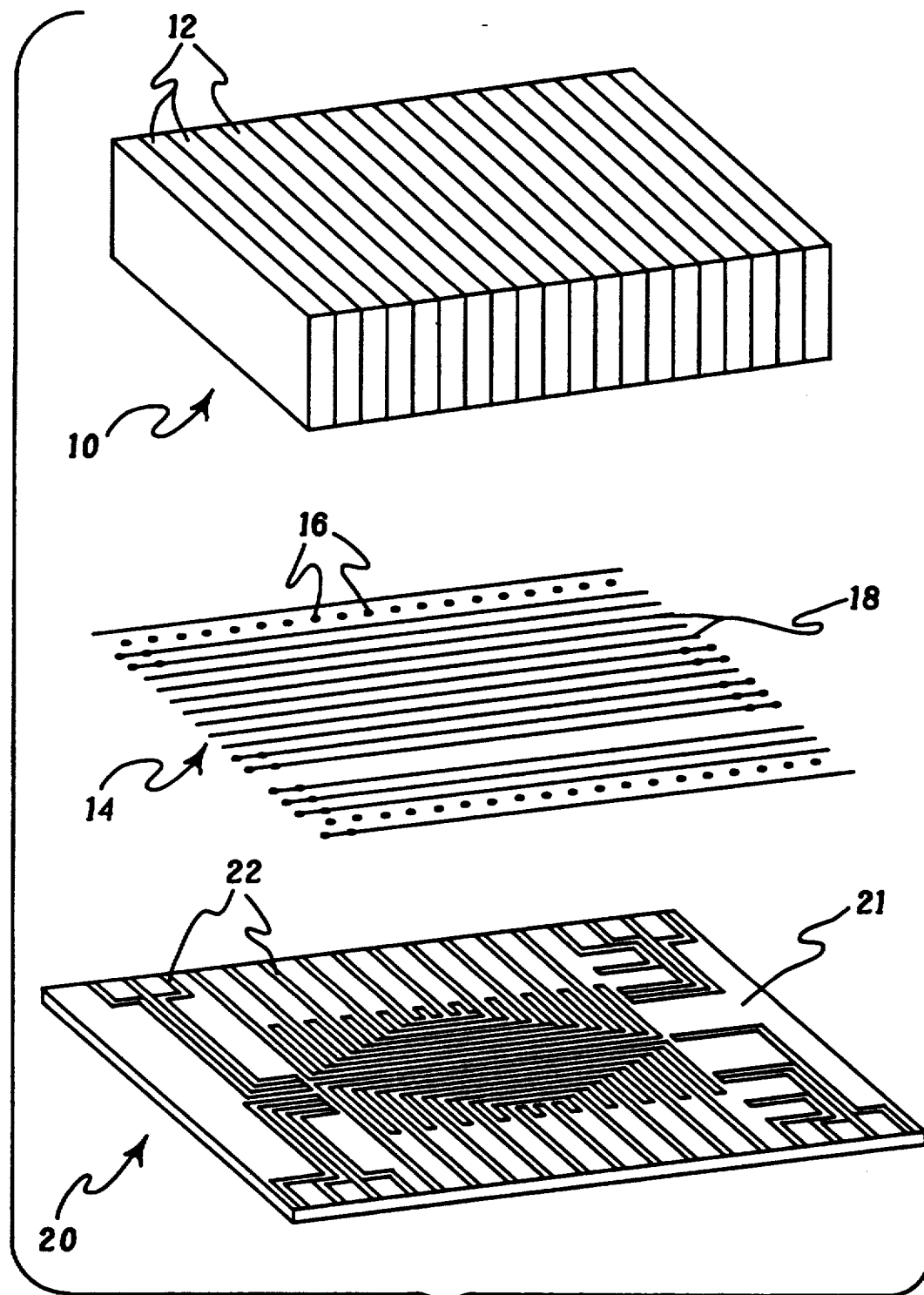


fig. 1
(PRIOR ART)

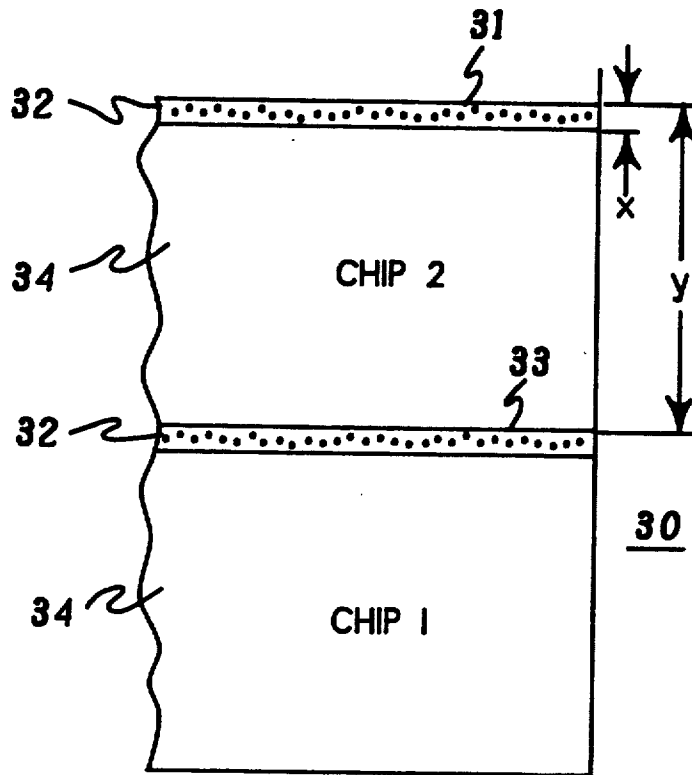


fig. 2a

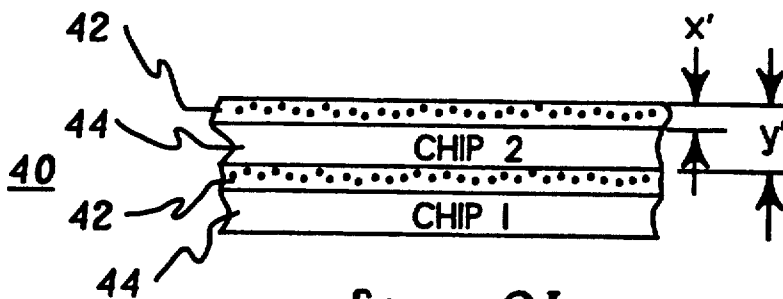
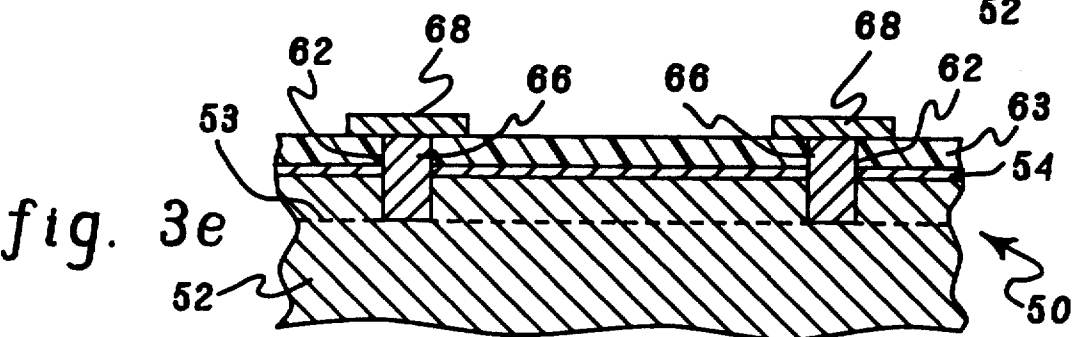
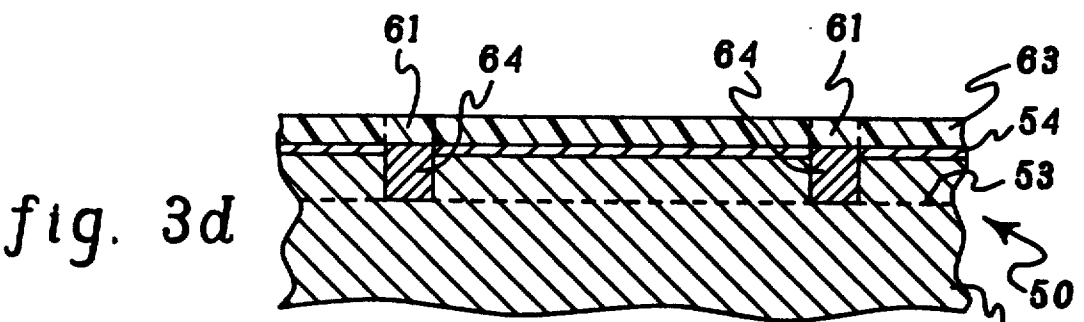
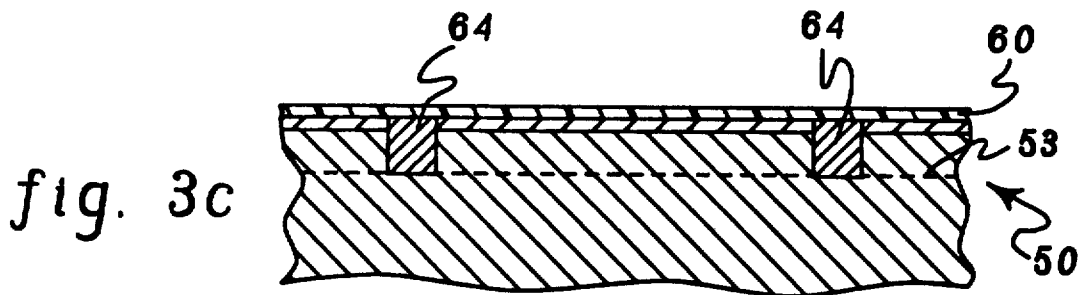
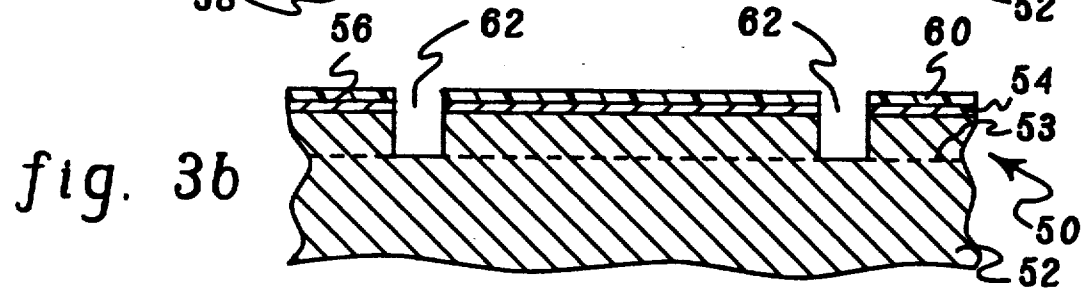
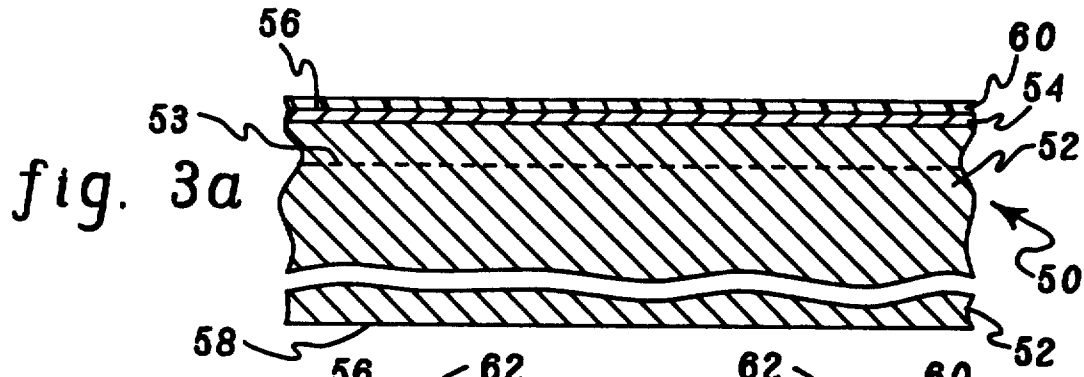


fig. 2b



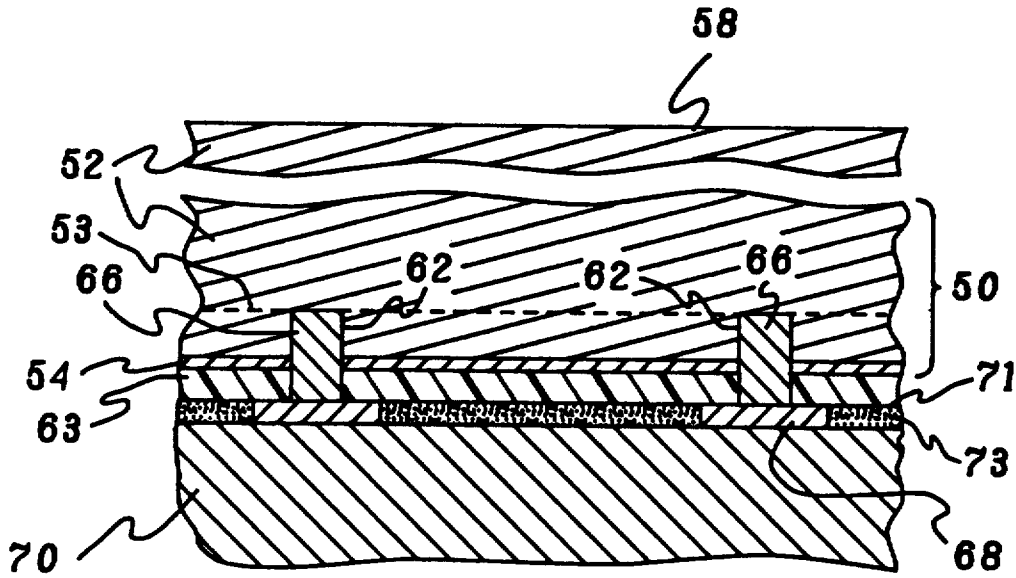


fig. 3f

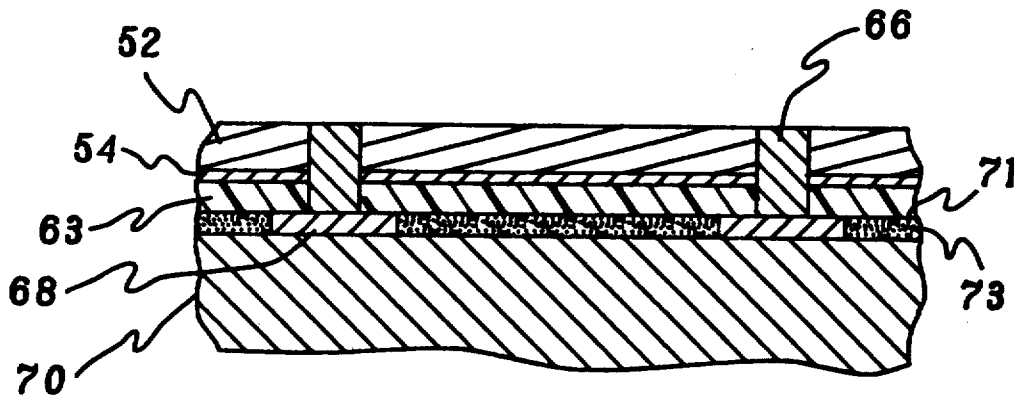


fig. 3g

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