US005080730A

United States Patent [19]

Wittkower

[11] **Patent Number: 5,080,730**

[45] **Date of Patent: Jan. 14, 1992**

[54] **IMPLANTATION PROFILE CONTROL WITH SURFACE SPUTTERING**

[75] Inventor: **Andrew B. Wittkower**, Rockport, Mass.

[73] Assignee: **IBIS Technology Corporation**, Danvers, Mass.

[21] Appl. No.: **342,484**

[22] Filed: **Apr. 24, 1989**

[51] **Int. Cl.**[5] **H01L 21/265**

[52] **U.S. Cl.** **148/33;** 437/24; 437/26; 437/62; 148/DIG. 158

[58] **Field of Search** .... 437/24, 26, 61, 62; 148/33, DIG. 158; 204/192.37, 192.25; 250/492.21

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,033,788	7/1977	Hunsperger et al.	148/1.5
4,241,359	12/1980	Izumi et al.	357/49
4,394,180	7/1983	Dearnaley et al.	148/1.5
4,452,646	6/1984	Zuleeg	148/1.5
4,704,302	11/1987	Bruel et al.	427/38

FOREIGN PATENT DOCUMENTS

2581795	11/1986	France	437/24
0031971	3/1978	Japan	437/61
0059090	5/1979	Japan	437/24
0208851	11/1984	Japan	437/62

OTHER PUBLICATIONS

"Sputter Etch Removal Rates of Insulators, Semiconductors, and Conductors", Larry L. Fritz, Solid State Technology, Dec. 1971, pp. 43–48.

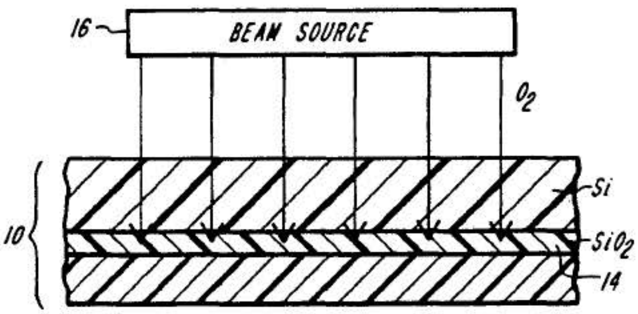
"Nucleation and Growth of SiO_2 Precipitates in SOI/-SIMOX Related Materials–Dependence Upon Damage and Atomic Oxygen Profiles", Nuclear instruments and methods in Physics research, Section B (Beam interactions with materials and Atoms) Mar. 1989, vol. B39, No. 1–4, Hemment et al., pp. 210–214.

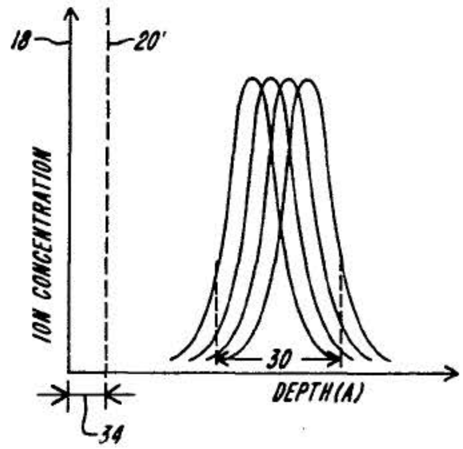
Primary Examiner—Olik Chaudhuri
Assistant Examiner—Ourmafd Ojan
Attorney, Agent, or Firm—Weingarten, Schurgin, Gagnebin & Hayes

[57] **ABSTRACT**

An ion implantation process for producing a buried insulating layer of silicon dioxide in a silicon substrate which takes advantage of the effects of surface erosion and sputtering inherent to the ion implantation process. The process allows the production of an insulating layer buried within a silicon semiconductor wherein the width of the insulating layer can be contoured by controlling the beam energy during implantation.

8 Claims, 3 Drawing Sheets





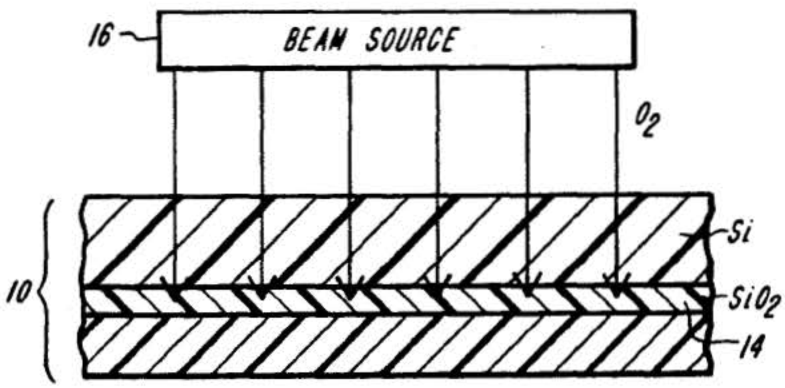


FIG. 1A

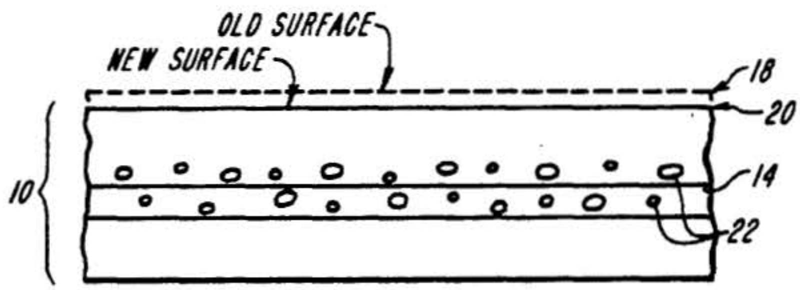


FIG. 1B

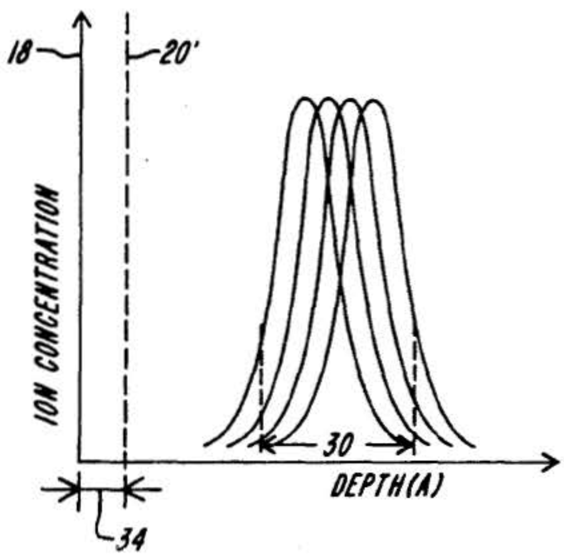


FIG. 1C

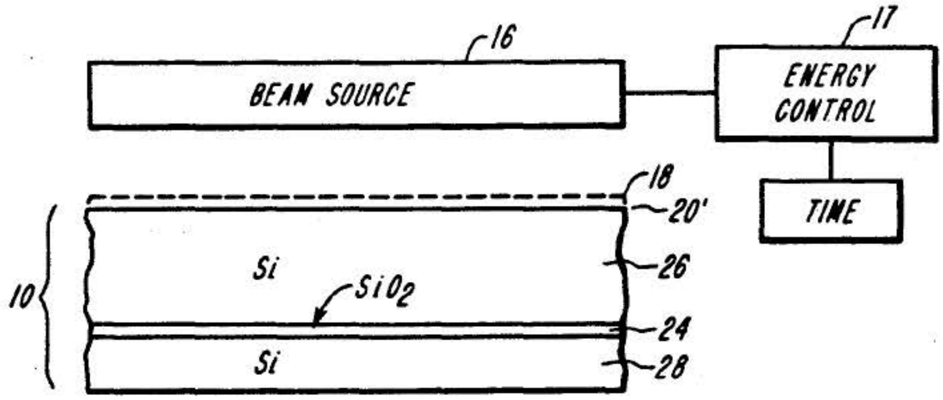


FIG. 2A

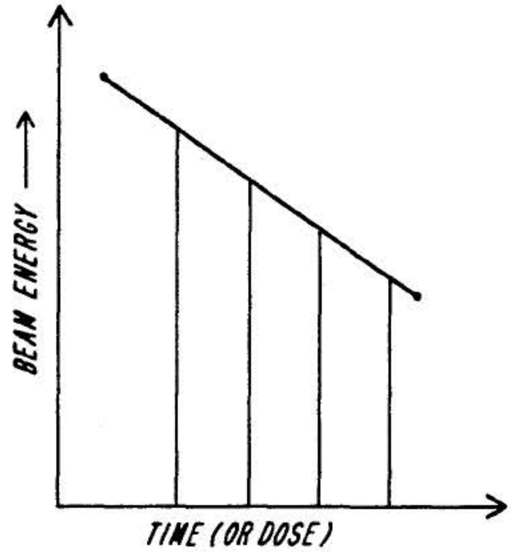


FIG. 2B

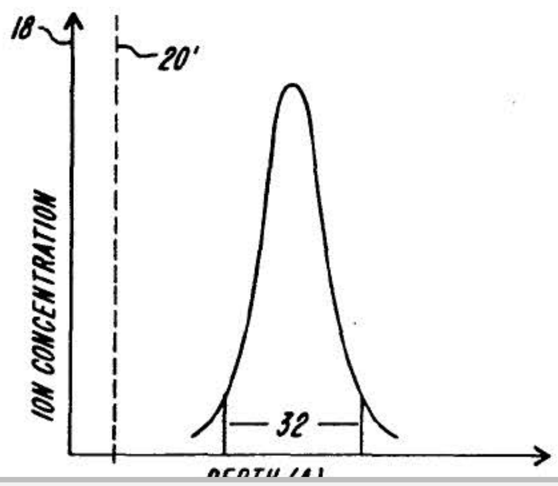


FIG. 3A

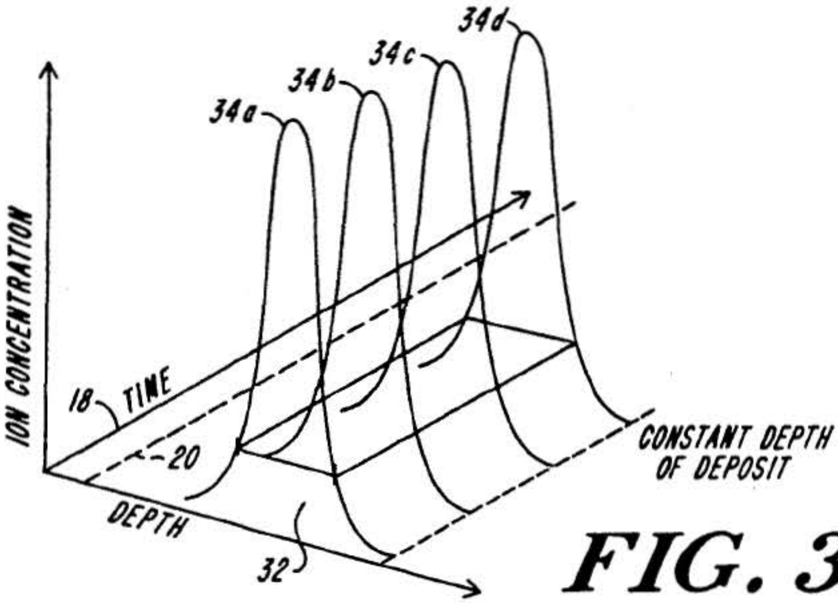


FIG. 3B

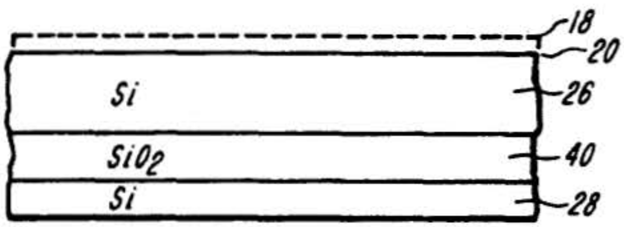


FIG. 4A

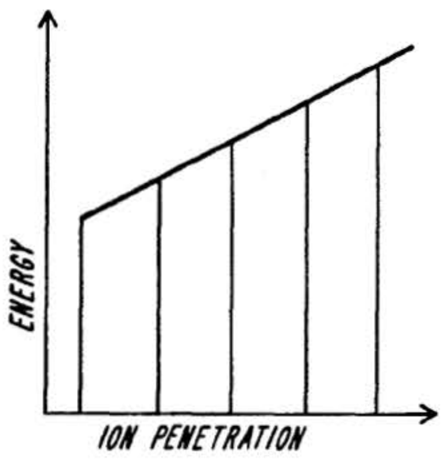


FIG. 4B

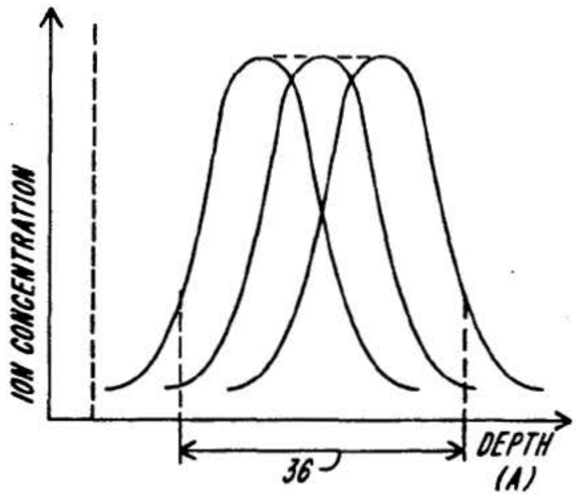


FIG. 5

IMPLANTATION PROFILE CONTROL WITH SURFACE SPUTTERING

FIELD OF THE INVENTION

This invention relates to a process used in semiconductor production and, more particularly, relates to a process for contouring an insulating layer formed in a semiconductor substrate by ion implantation.

BACKGROUND OF THE INVENTION

Ion implantation is a process in which atomic particles are introduced into a substrate for the purpose of changing the electrical or chemical properties of the substrate. This process uses high energies to accelerate ions which enter the surface and are slowed down by electronic or nuclear collisions with the substrate atoms, and come to rest some small distance below the surface. Modern semiconductor technology is one field in which ion implantation is particularly useful and wherein implanted ions are used to alter the conductivity of the base material as well as to form buried insulating layers. One object, in the case of buried insulating layers, is the minimization of the volume of electrically active semiconductor material to reduce parasitic effects such as device-to-device effects (known as latch-up), leakage capacitance, resistance, etc. and to minimize sensitivity to radiation.

In the early 1980's, a process known as separation by implanted oxygen or SIMOX was developed in which a high-dose of oxygen ions are implanted into a solid monocrystalline silicon substrate, making it possible to form a buried layer of silicon dioxide SiO_2). The resultant layer dielectrically isolates circuit elements, enabling the fabrication of smaller, closer and faster circuits which are immune to the noted parasitic and radiation effects which cause latch-up and add to circuit capacitance.

Using the SIMOX process, oxygen ions are implanted into silicon at a constant beam energy between 150 and 200 keV at a dose of approximately 1.6×10^{18} ions/cm^2. After implantation, the material is annealed to form the chemically bonded silicon dioxide. A typical anneal cycle involves heating the substrate to approximately **1300** degrees for six hours. This annealing phase redistributes the oxygen ions which are implanted in a roughly Gaussian profile with respect to the most probable depth (range) such that the silicon/silicon dioxide boundary on either side of the silicon dioxide layer becomes markedly more abrupt, thus forming a sharp and well-defined region centered at the most probable depth.

During implantation, incoming high-speed oxygen ions sputter silicon ions from the surface resulting in surface erosion. Due to the effect of this surface erosion, the original surface of the silicon layer is displaced, causing ions implanted toward the end of the implant cycle to come to rest at a depth deeper than ions implanted at the start of the implant cycle. In practice, this erosion effect is magnified when a surface layer of silicon dioxide is provided to protect surface features because silicon dioxide erodes more rapidly than silicon during implantation. As a result of the variation in implantation depth of oxygen ions, a broader band of silicon oxide layer is created. This, in turn, increases the minimal acceptable dose of oxygen ions required to create the silicon dioxide layer, thereby causing even greater surface damage and longer processing times.

SUMMARY OF THE INVENTION

The present invention relates to a process for producing a buried insulating layer, typically of silicon dioxide (SiO_2) or silicon nitride (Si_3N_4), within a silicon substrate in a manner which advantageously regulates the implantation energies in response to the surface erosion to produce a thinner, low dosage insulating layer suitable for typical low voltage use, or a thicker, more even layer in a semiconductor substrate wherein the thickness of the buried insulative layer is determined by controlling the beam energy used to implant ions into the silicon layer as a function of surface erosion. The silicon layer erodes at a rate which is dependent on the density of the ions being implanted into the silicon. The peak ion distribution is maintained at a constant position by reducing the beam energy and corresponding penetration by an amount corresponding to the depth of erosion. This more rapidly achieves the ion density required to fully form an oxide barrier with less exposure of the substrate to ion implantation effects. The oxide barrier thus formed, while thinner, provides protection for most semiconductor applications which are typically low voltage applications.

Conversely, by increasing the beam energy over the implantation period, the peak of the ion implantation distribution occurs at progressively deeper depths, advantageously benefited by the surface erosion which allows the distribution to shift naturally. In this case, the oxide barrier is formed over a greater depth to provide additional insulative protection in high voltage applications.

The process for producing a buried insulating layer according to the present invention is advantageous for producing an active component of an integrated circuit positioned on crystalline silicon material above an insulating layer. This technique produces a radiation hardened material and also dielectrically isolates circuit elements enabling smaller, closer and faster circuits to be fabricated with a marked reduction in stray capacitance and an increase in the operating speed of the circuits. Additionally, the material shows great promise for mixed application such as BI-CMOS circuits which combine power and logic on the same chip.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

Figs. **1A** to **1B** are diagrammatic representations showing a prior art ion implantation process for producing a buried insulating layer in a semiconductor substrate at different stages in the process;

FIG. **1C** is a graph of ion concentration with respect to the depth of deposition according to the prior art;

FIG. **2A** is a diagrammatic representation of a modified ion implantation process for producing a narrowed buried insulating layer according to a first embodiment of the invention;

FIG. **2B** is an energy profile diagram showing the energy tapering according to the first embodiment of the invention;

FIGS. **3A** and **3B** are graphs showing the Gaussian distribution of the ions with respect to the distance from the top face of the silicon layer in the first embodiment of the invention;

FIG. **4A** is a diagrammatic representation of ion implantation for producing a widened buried insulating

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.

WHAT WILL YOU BUILD? | sales@docketalarm.com | 1-866-77-FASTCASE