United States Patent [19]

Miura et al.

[54] SEMICONDUCTOR DEVICE HAVING SEMICONDUCTOR-ON-INSULATOR STRUCTURE

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- [73] Assignee: Fujitsu Limited, Kawasaki, Japan
- [21] Appl. No.: 447,524
- [22] Filed: Dec. 7, 1989

[30] Foreign Application Priority Data

Dec. 8, 1988 [JP] Japan 63-310458

- [51]
 Int. Cl.⁵
 H01L 29/78

 [52]
 U.S. Cl.
 357/23.7; 357/2;
- 357/4: 357/23.45

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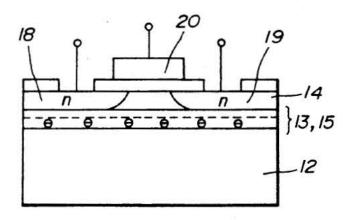
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Primary Examiner-Rolf Hille Assistant Examiner-Tan Ho Attorney, Agent, or Firm-Staas & Halsey

[57] ABSTRACT

A method of producing a semiconductor-on-insulator structure generates a first fixed charge in an insulator layer of a base substrate. An active substrate which is made of a semiconductor is bonded on the insulator layer of the base substrate to thereby generate a second fixed charge at an interface of the insulator layer and the active substrate. The first and second fixed charges have mutually opposite polarities. A portion of the active substrate is removed to form the active substrate to an arbitrary thickness.

8 Claims, 9 Drawing Sheets



Δ

FIG.IA PRIOR ART



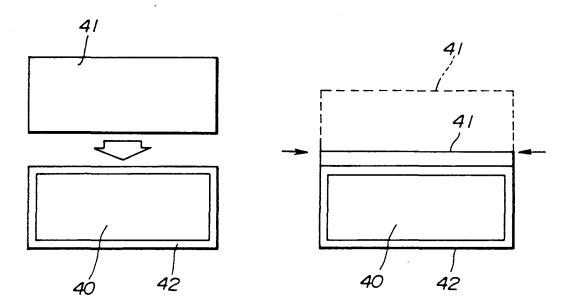
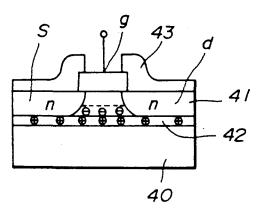


FIG.2 PRIOR ART



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FIG.3 PRIOR ART

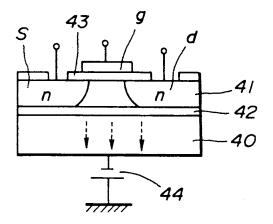
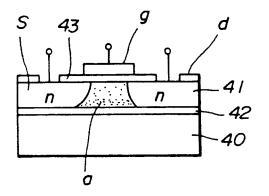


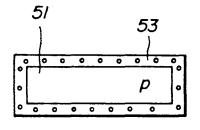
FIG.4 PRIOR ART

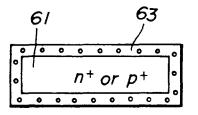


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FIG.5A







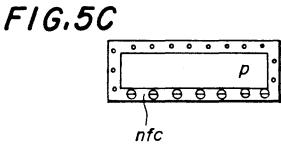


FIG.5D

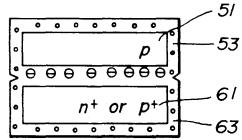
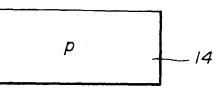


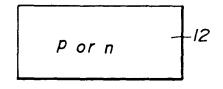
FIG.5E

Α

$$\begin{array}{c}
 p \\
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 \hline
 n^+ \ or \ p^+ \\
 \bullet \bullet \bullet \bullet \bullet \bullet \\
 \end{array}$$

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F/G.6C

FIG.6B

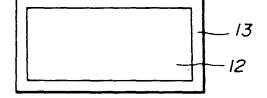
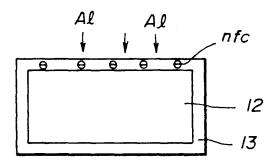
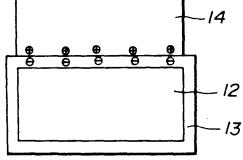


FIG.6D







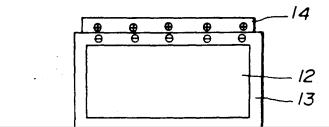


FIG.6F

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