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Poon et al.

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[54] **METHOD FOR POLISH PLANARIZING A SEMICONDUCTOR SUBSTRATE BY USING A BORON NITRIDE POLISH STOP**

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[51] **Int. Cl.**[5] **B05D 3/06**

[52] **U.S. Cl.** ..... **427/39**; 427/255.2; 427/255.7; 427/355; 51/281 R; 51/310

[58] **Field of Search** ..... 51/326, 281 R, 310; 264/162; 437/225; 427/34, 248.1, 264, 39, 255.7, 355, 255.2; 501/96

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,627,991	12/1986	Seki et al.	427/39
4,671,851	6/1987	Beyer et al.	156/645
4,789,648	12/1988	Chow et al.	437/225
4,910,155	3/1990	Cote et al.	437/8
4,944,836	7/1990	Beyer et al.	156/645

OTHER PUBLICATIONS

"Properties of the B-Si-N Ceramic Thin Films by Plasma-CVD" Takahiro Nakahigashi et al., Shinku (Vacuum), vol. 31, No. 9, pp. 789-795 (1988) Translation provided.

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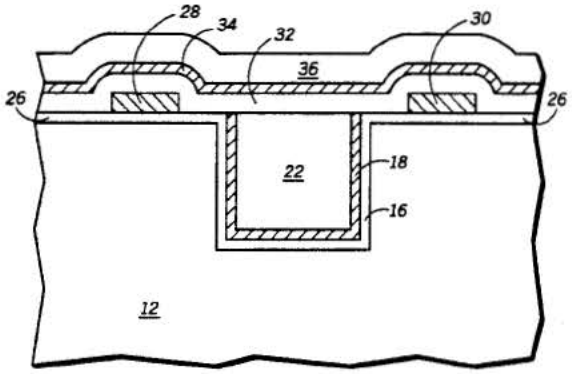
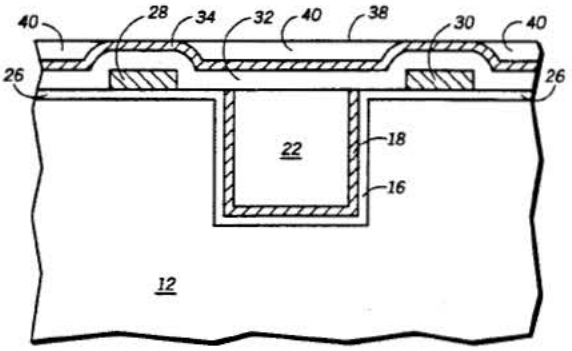
[57] **ABSTRACT**

In a polish palnarization process using a polishing apparatus and an abrasive slurry, a boron nitride (BN) polish stop layer (**18**) is provided to increase the polish selectivity. The BN layer deposited in accordance with the invention has a hexagonal-close-pack crystal orientation and is characterized by chemical inertness and high hardness. The BN layer has a negligible polish removal rate yielding extremely high polish selectivity when used as a polish stop for polishing a number of materials commonly used in the fabrication of semiconductor devices. In accordance with the invention, a substrate (**12**) is provided having an uneven topography including elevated regions and recessed regions. A BN polish stop layer (**18**) is desposited to overlie the substrate (**12**) and a fill material (**20, 36**) which can be dielectric material or a conductive material, is deposited to overlie the BN polish stop (**18**) and the recessed regions of the substrate. The fill material is then polished back until the BN polish stop is reached resulting in the formation of a planar surface (**38**).

11 Claims, 2 Drawing Sheets





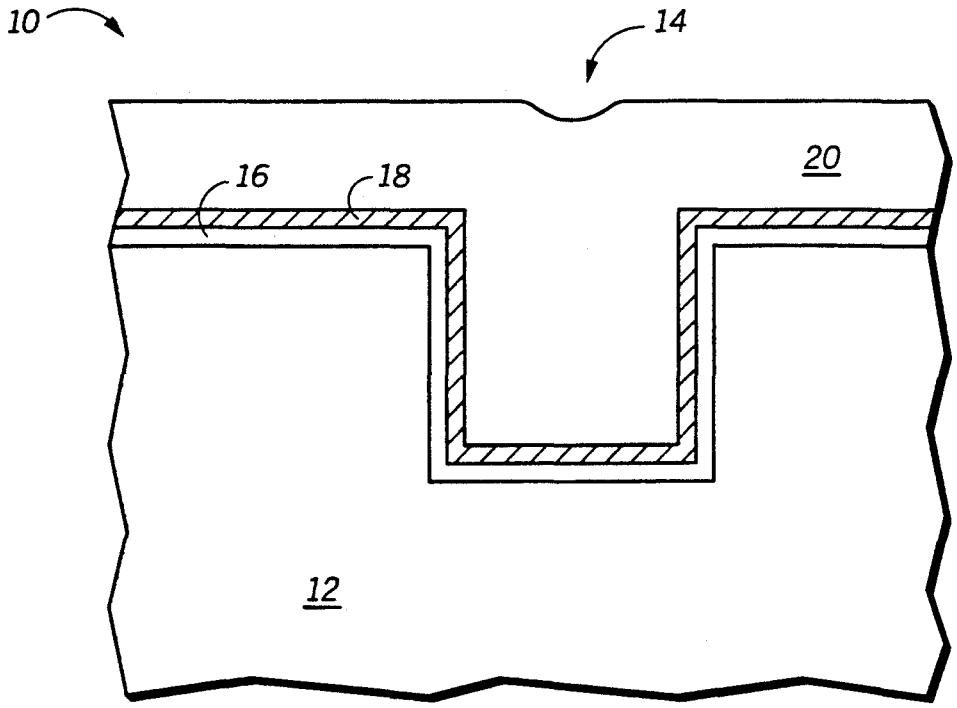


FIG.1

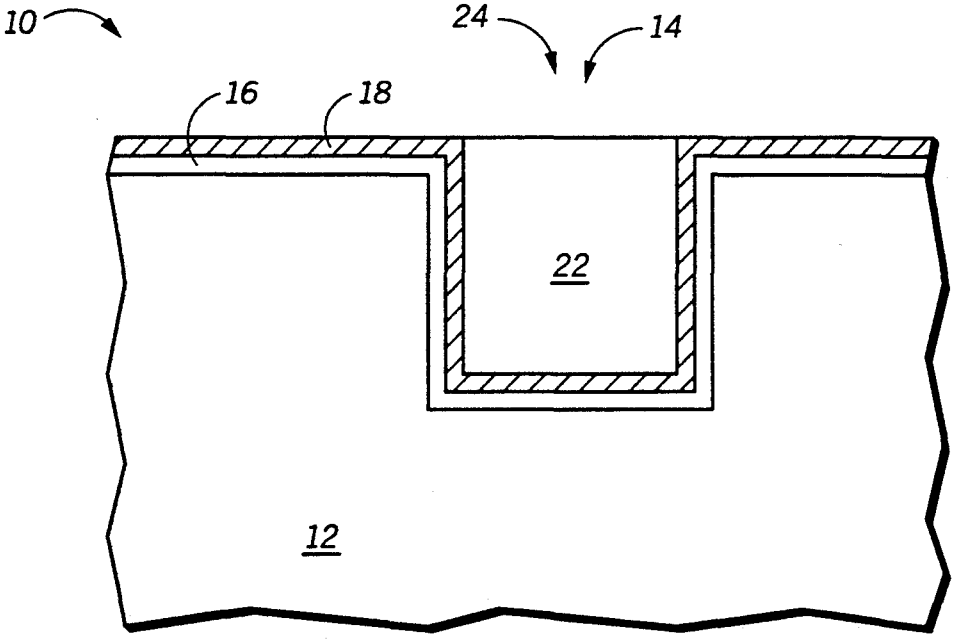


FIG.2

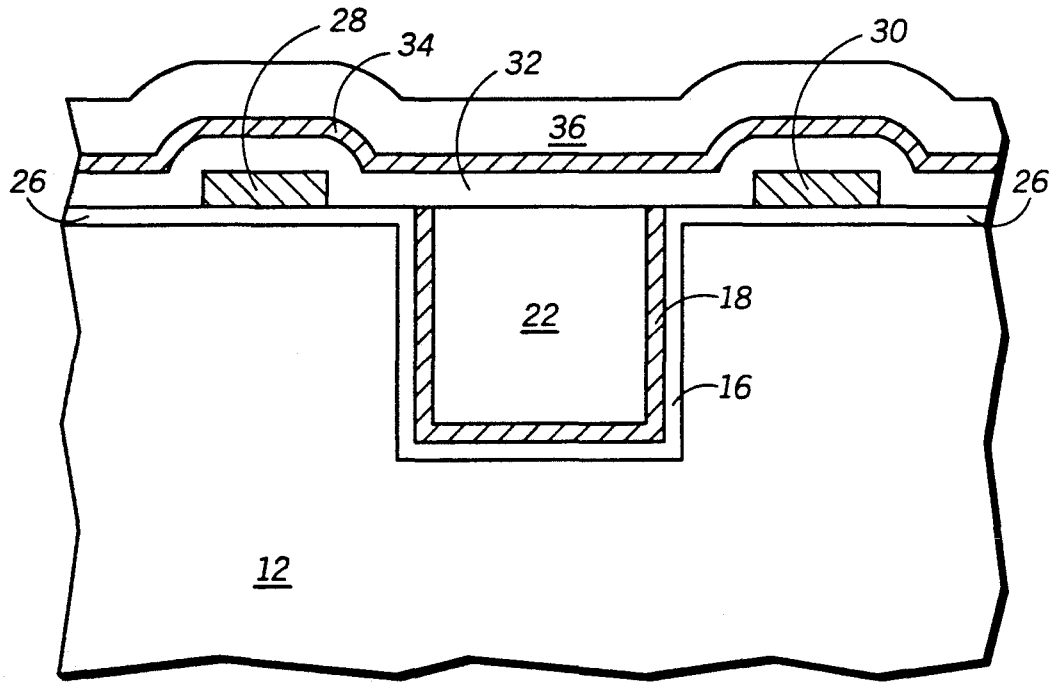


FIG.3

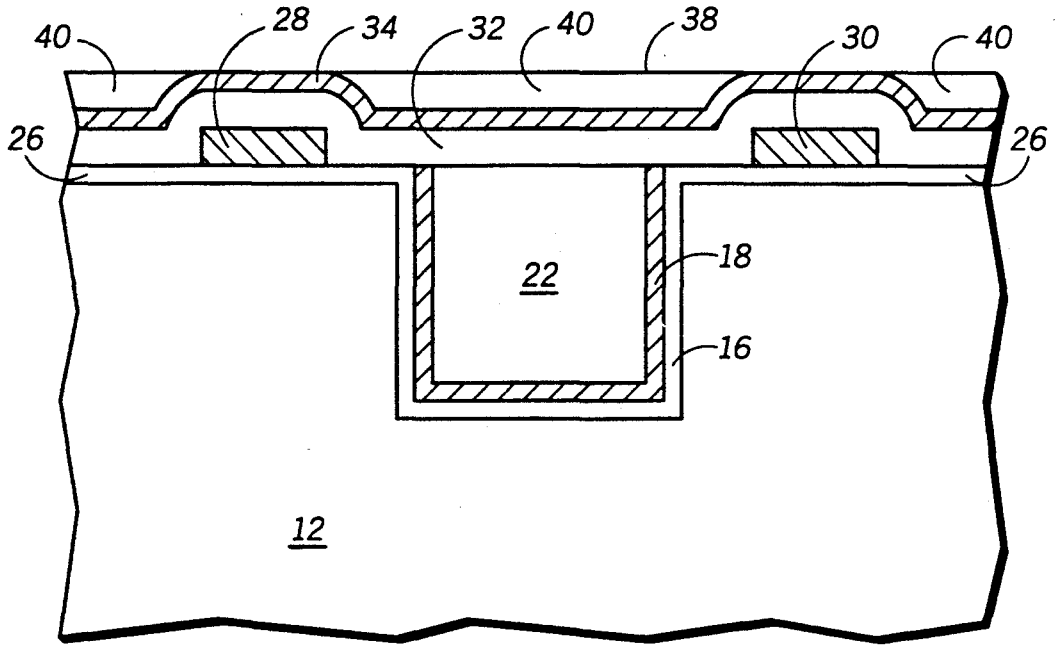


FIG.4

METHOD FOR POLISH PLANARIZING A SEMICONDUCTOR SUBSTRATE BY USING A BORON NITRIDE POLISH STOP

FIELD OF THE INVENTION

This invention relates in general to a method for fabricating a semiconductor device, and more particularly to a method for polish planarizing a semiconductor substrate with an improved polish stop.

BACKGROUND OF THE INVENTION

In order to build faster and more complex integrated circuits, semiconductor manufacturers have increased the number of components in the integrated circuit while reducing the overall size of the circuit. The small circuit size requires multiple overlying conductive layers to electrically interconnect the vast number of components within the integrated circuit. As successive layers of conductors and dielectric materials are deposited over previously defined structures, the surface topography can become uneven. To be manufactured reliably, the conductive layers need to be deposited, and an interconnect pattern defined on a smooth, planar surface. A planarization process is typically performed after the deposition of a dielectric passivation layer to reduce the topographic contrast of the passivation layer. A conductive layer is then deposited on a smooth, even surface and the interconnect pattern reliably defined using conventional photolithography.

One method for planarizing the substrate surface during integrated circuit fabrication is a polish planarization process. Recently, polishing processes have been developed which abrasively removed elevated portions of a passivation layer overlying an uneven substrate. In this process, known as chem-mech polishing, the passivated surface of the substrate is brought into contact with a rotating polish pad in the presence of an abrasive slurry. A portion of the passivation layer is then abrasively removed by the mechanical action of the polish pad and the chemical action of the slurry. The slurry serves to lubricate the surface and contains a fill material such as silica to provide additional abrasive force. Additional chemicals are sometimes added to the slurry to adjust the pH and to chemically etch the surface of the layer to be polished. See for example, U.S. Pat. No. 4,910,155 to W. Cote. Wafer polishing has the advantage of being very versatile and not limited by the particular material being polished. The polishing technique can also be used to remove irregularities from the surface of a silicon substrate.

A common requirement of all polishing processes is that the substrate be uniformly polished. In the case of polishing back a passivation layer, it is desirable to polish the layer uniformly from edge to edge on the substrate. To insure that a planar surface is obtained, the passivation layer overlying elevated surface regions must be uniformly removed. Uniform polishing can be difficult because, typically, there is a strong dependence in the polish removal rate with localized variations in the surface topography of the substrate. For example, in substrate areas having a high degree of surface variation, such as areas having closely spaced adjacent trenches, the polishing rate is higher than in areas lacking a high degree of surface contrast, such as areas having large active device regions. The effect of surface topography on the removal rate requires the polishing time to be extended beyond that required to just remove the passivation layer from the most elevated regions. However, the polish time cannot be extended indefinitely or layers underlying the passivation layer can be damaged. The polish selectivity can be defined as the ratio of the removal rate of an overlying layer to that of an underlying layer. The polish selectivity must be maximized in order to improve the edge to edge polish rate uniformity and the ultimate ability of the polish process to form a planar surface. One technique used to increase polishing selectivity, described in U.S. Pat. No. 4,944,836 to K. Beyer, adjusts the composition and pH of the slurry solution depending upon the polish characteristics of the particular material to be polished and the underlying layer. More commonly, a hard, thin film referred to as a polish stop layer is deposited to overlie the uneven surface of the substrate prior to depositing the passivation layer. The polish stop layer underlying the passivation layer is more resistant to abrasive removal than the passivation layer. During polishing, when the polish stop overlying the most elevated surface regions of the substrate is exposed, the removal rate of material from the substrate declines and ideally stops altogether as all of the elevated portions of the polish stop layer become exposed. If the polish stop material is sufficiently resistant to abrasive removal and chemically unreactive with the components in the slurry, the polishing time can be extended for a long enough period to uniformly polish the passivation layer without damaging underlying layers.

While potentially offering wide versatility and a high degree of uniformity, the polish process must be controlled to avoid damaging underlying layers. Although previous investigators have adjusted various elements of the polishing process to increase the polish selectivity, such as the slurry composition and the polish pad material, the preferred method remains the use of a polish stop layer. A variety of polish stop materials have been reported including silicon nitride, alumina and magnesium oxide with silicon nitride being the most widely used. For example, the use of silicon nitride is described in U.S. Pat. No. 4,671,851 to K. Beyer et al. The polish stop material must be chemically inert, have high hardness and have deposition and removal characteristics which are compatible with existing process techniques. While materials such as silicon nitride and alumina are well characterized and widely used in semiconductor fabrication, they lack the necessary characteristics needed for a highly selective polish process.

BRIEF SUMMARY OF THE INVENTION

In practicing the present invention there is provided a method for forming a BN polish stop layer in which the BN has a hexagonal-close-pack crystal orientation. The BN layer has a negligible polish removal rate yielding extremely high polish selectivity when used as a polish stop for polishing a number of materials commonly used in the fabrication of semiconductor devices. In accordance with the invention, a substrate is provided having an uneven topography including elevated regions and recessed regions. A BN polish stop layer is deposited to overlie the elevated regions and a fill material is deposited to overlie the BN polish stop and the recessed regions of the substrate. The fill material is polished back until the BN polish stop is reached forming a planar surface.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1** and **2** illustrate, in cross section, one embodiment of a planarization process in accordance with the invention; and

FIGS. **3** and **4** illustrate, in cross section, another embodiment of a planarization process in accordance with the invention.

It will be appreciated that for simplicity and clarity of illustration elements shown in the FIGURES have not necessarily been drawn to scale. For example, the dimensions of some of the elements are exaggerated relative to each other for clarity. Further, where considered appropriate, reference numerals have been repeated among the FIGURES to indicate corresponding elements.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

In a search for suitable semiconductor materials that can be polished to form a planar surface, it has been discovered that boron nitride (BN) forms an excellent polish stop having very good adhesiveness to silicon and dielectric materials, such as silicon dioxide. The boron nitride can be easily deposited, preferably by plasma-enhanced-chemical-vapor-deposition (PECVD), or alternatively, by thermal chemical-vapor-deposition (CVD), to form a continuous layer of high hardness on the surface of a substrate. The selected PECVD deposition conditions produce a BN film having a hexagonal-close-pack crystal orientation similar to that of graphite. Despite the well known softness characteristics of graphite, the BN film deposited in accordance with the invention is characterized by substantial resistance to abrasive and chemical removal during a polishing process. The development of a polish stop material that is both chemically unreactive with many polish slurry compositions and of high hardness, greatly increases the utility of a polishing process used during semiconductor device fabrication.

The BN material used to form a polish stop layer is preferably deposited onto a semiconductor substrate in a PECVD reactor such as a Plasma III system manufactured by ASM of Phoenix, Arizona. The deposition is carried out by flowing about 100 to 250 standard-cubic-centimeters-per-minute (SCCM) of diborane (B_2H_6), about 500 to 1500 SCCM of ammonia (NH_3) and about 3000 to 5000 SCCM of a carrier gas such as argon (Ar) into the reactor. A total gas pressure of about 1 to 3 Torr is maintained and a plasma is created by applying about 1500 to 2000 Watts of RF power to the anode located within the reactor chamber. A substrate temperature of about 250° to 400° C. is maintained during the deposition.

Infra-Red (IR) spectrographic analysis of BN formed using the reactor conditions given above indicates the BN film has a hexagonal-close-pack crystal orientation. It has also been found that at a higher substrate temperature and RF power, BN having a cubic crystal orientation is obtained. While the cubic form of BN possesses high hardness, it does not have the desirable adhesive properties of the hexagonal-close-pack form of BN. Experiments carried out to determine film characteristics of hexagonal BN deposited on a silicon substrate have shown hexagonal BN to have high hardness and to adhere strongly to silicon. In addition, the hexagonal BN film is substantially unreactive with common chemical etchants such as hydrofluoric acid (HF) and phosphoric acid (H_3PO_4).

A particular advantage of the forming a hexagonal BN layer in accordance with the invention is the relatively low deposition temperature used during the deposition process. The deposition temperature at which hexagonal BN is deposited is sufficiently low such that unwanted thermally catalyzed dopant diffusion and material deformation are avoided. For example, in the 250° to 400° C. deposition range of hexagonal BN, the diffusion of dopants previously introduced into the semiconductor substrate will not occur. Furthermore, at the deposition temperature of hexagonal BN, materials having low thermal tolerances, such as aluminum or aluminum-silicon alloys will not soften. In contrast, a deposition temperature of about 600° to 900° C. is necessary to deposit cubic BN which is detrimental to aluminum conductors and can induce dopant diffusion. The low deposition temperature of the hexagonal BN polish stop layer thus enables the use of a polishing process at various stages in a semiconductor fabrication process including after the formation of doped regions and metal interconnects.

Typically, in a fabrication process in which a planarization step is to be used, the substrate has an uneven surface topology characterized by recessed regions and elevated regions. Once the BN polish stop is deposited onto a substrate surface, one or more layers to be planarized are deposited to overlie the BN polish stop. The polishing operation is then preferably carried out in a polishing apparatus having a rotating polish wheel with a polyurethane polishing pad disposed thereon. One such commercially available polishing apparatus is the "Westech 372" manufactured by Westech Inc. of Phoenix, Ariz. A commercially available slurry comprised of colloidal silica suspended in potassium hydroxide (KOH) is applied to the polishing pad and the one or more layers overlying the BN are removed until the BN layer is reached. Upon exposure of the BN layer, the removal of any remaining portions of the substrate, and layers thereon, ceases resulting in a smooth planar surface.

The removal rate of hexagonal BN deposited using the PECVD process previously described has been measured and compared with other materials commonly used in semiconductor device fabrication. Under standard polishing conditions and a pad pressure ranging from 3 to 10 pounds-persquare-inch (psi), a negligible removal rate of BN polish stop has been observed. The other polishing conditions are summarized as follows: platen temperature of 38° C.; 15 rpm platen speed; slurry flow rate about 175 SCCM, (Cabot SC1 slurry manufactured by Nalco Chemical Co.); 35 rpm carrier speed; Suba4/IC60 polish pad, manufactured by Rodel Products Corp. of Scottsdale, Ariz. Following the primary polish, a KOH and deionized water rinse solution is applied at a secondary platen. The removal rates for various materials at pad pressures of 5 and 7 psi and polishing times of 3 min. were determined by film thickness measurements using a Nanospec AFT optical interferometer manufactured by Nanospec Inc. The results are presented in Table I.

TABLE I

MATERIAL	PAD PRESSURE (PSI)	REMOVAL RATE (NM/MIN)
LTO	5	79
LTO	7	103

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