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SPECIFICATION

1. Title of the Invention:

METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

2. Claim

(1) A method for manufacturing a semiconductor device characterized by comprising the steps of:

forming an element and wiring on a semiconductor substrate which has a buried insulating layer formed by ion implantation, and bonding a supporting substrate thereon;

polishing the back surface of said semiconductor substrate by chemical mechanical polishing to the lower surface of said buried insulating layer; and

opening a through-hole at a given position in said buried insulating layer and forming back surface wiring therein.

3. Detailed Description of the Invention

[Field of Industrial Application]

The present invention relates to a method for manufacturing semiconductor devices, in particular, to a method for manufacturing semiconductor devices having a structure where active or passive elements, or both, are stacked in multiple layers.

[Related Art]

In order to increase the scale and density of semiconductor integrated circuits, there has been proposed a structure where active elements such as transistors are stacked in multiple layers on the surface of a semiconductor substrate. A method for producing such a structure is comprised of depositing an insulating film on the surface of a bulk silicon substrate on which a transistor and wiring of a first layer have been formed, growing single-crystal silicon thereon by SOI (Silicon-on-Insulator) crystal growth, forming a transistor and wiring of a second layer thereon, and thereafter, repeating the combination of insulating film deposition, SOI crystal growth, and transistor and wiring forming step to form multiple layers.

However, no SOI crystal growth technology has been established thus far to uniformly form single-crystal silicon over a wide area. Furthermore, it is not preferable to increase the number of manufacturing steps in proportion to the number of layers as it inevitably reduces the throughput and yield. This has given rise to a conceivable method of preparing unit structures by parallel processing where a silicon layer on which an insulating layer and element have been formed, and wiring are layered, which are subsequently made thin, and sequentially bonded together to form multiple layers.

Thinning techniques have been used, not for the primary purpose of multi-layering active layers,

but to increase the radiation resistance, processing rate, and breakdown voltage in cases where the elements formed on bulk silicon substrates are transferred onto supporting substrates which are bonded on the upper surfaces of the elements by thinning the silicon substrates by means of chemical mechanical polishing applied from the back surfaces.

[Problems to be Solved by the Invention]

In cases where bulk silicon substrates on which elements have been formed are chemical mechanical polished from the back surfaces, however, the polishing time must be given a range so as to be long enough to deal with substrate thickness variations, which might occasionally polish off the silicon in the element regions that are supposed to be left behind. Moreover, the polishing rate is dependent on the exposed silicon area, which might restrict mask pattern designing.

It is an object of the present invention to provide a method for manufacturing semiconductor devices free of the problems described above.

[Means for Solving the Problems]

The method for manufacturing semiconductor devices according to the present invention is characterized by including the steps of:

forming an element and wiring on a semiconductor substrate which has a buried insulating layer formed by ion implantation, and bonding a supporting substrate thereon;

polishing the back surface of said semiconductor substrate by chemical mechanical polishing to the lower surface of said buried insulating layer; and

opening a through-hole at a given position in said buried insulating layer and forming back surface wiring therein.

[Embodiment]

An exemplary embodiment of the present invention will be described with reference to FIG. 1.

As shown in FIG. 1(a), a buried oxide layer 12 comprised of a silicon oxide film is formed by implanting oxygen ions at a dose of 2×10^{18} cm^{-2} across the entire surface of a p-type silicon substrate 11 at an accelerating voltage of 150 keV, followed by annealing at about 1,200°C. Then, an n-channel MOS transistor 13, wiring 14, and an insulating film 15 comprised of a silicon oxide film are formed thereon.

Next, as shown in FIG. 1(b), a supporting silicon substrate 16 is bonded on the insulating film 15 with an epoxy resin or the like, and the silicon substrate 11 is polished from the back surface by chemical mechanical polishing. Since the buried oxide film layer 12 is present, chemical mechanical polishing stops at the lower surface of the buried oxide film layer. Accordingly, the silicon substrate 11 would be polished off from the back surface to the lower surface of the buried oxide film layer 12.

Next, as shown in FIG. 1(c), a through-hole is formed in the buried oxide film layer 12, and back-surface wiring 17 is formed therein.

Next, as shown in FIG. 1(d), by superposing the back surface wiring side thereof on the upper surface of the base substrate 18, which has been separately prepared by forming an element on a bulk silicon substrate by following the same steps as those described above, and removing the supporting silicon substrate 16, a two-layer active layer structure is formed. Repeating the steps described above enables the production of a semiconductor device where three or more active layers are stacked.

In the above embodiment, oxygen ions were used for ion implantation to form the buried insulating layer 12, but nitrogen ions or the like may alternatively be used.

In the above embodiment, moreover, a method for manufacturing a semiconductor device structured with n-channel MOS transistors being stacked in multiple layers was described, but the same steps can also manufacture those structured with p-channel MOS transistors. Moreover, the method of

course can manufacture semiconductor devices where both an n-channel and p-channel MOS transistors are present in the same layers, or n-channel and p-channel MOS transistors are alternately present in the layers.

[Effect of the Invention]

The present invention uses a semiconductor substrate on which a buried insulating layer is formed across the entire surface of the substrate by ion implantation using oxygen, nitrogen, or the like, and thus chemical mechanical polishing from the back surface of the semiconductor substrate stops at the lower surface of the buried insulating layer, thereby enabling uniform thinning substantially unaffected by the initial semiconductor substrate thickness variations. Furthermore, the buried insulating layer itself can concurrently serve as an interlayer insulating film. The present invention, therefore, is effective in forming unit structures for stacking multiple active layers.

4. Brief Description of the Drawing

FIG. 1 shows cross-sectional views of the manufacturing steps explaining one example of the manufacturing method according to the present invention.

11 ⋯ silicon substrate
12 ⋯ buried oxide film layer
13 ⋯ MOS transistor
14 ⋯ wiring
15 ⋯ insulating film
16 ⋯ supporting silicon substrate
17 ⋯ back surface wiring
18 ⋯ base substrate on which element is mounted

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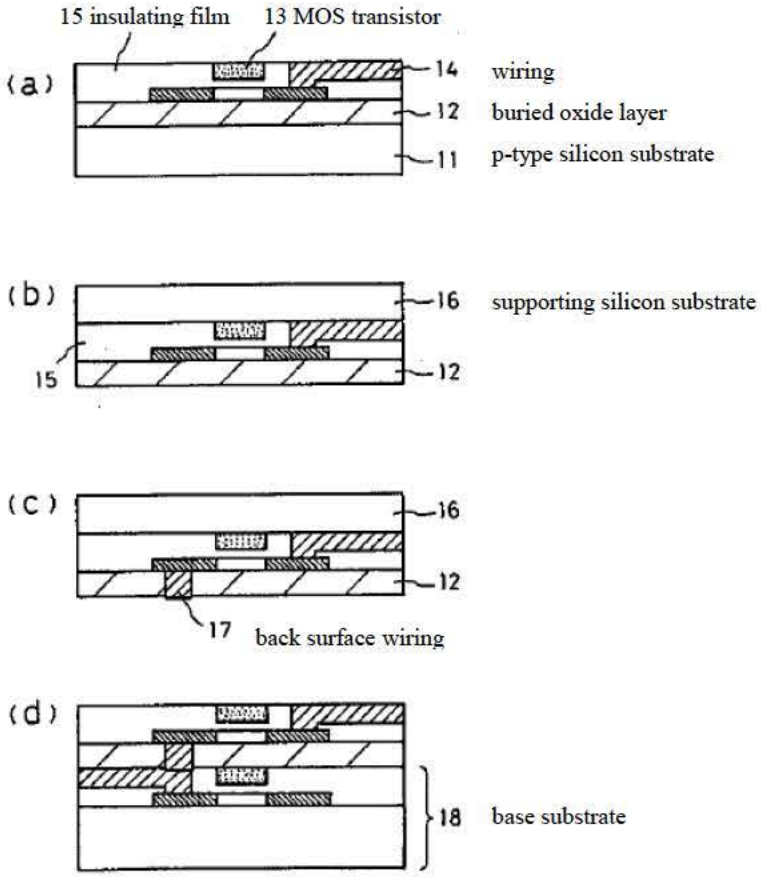
FIG. 1



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CERTIFICATION OF TRANSLATION

I, Asami Isomichi, hereby declare:

1. I am a Japanese language translator.
2. I have over 25 years experience translating technical, legal, and business documents from Japanese to English, and from English to Japanese.
3. I certify that the English translation of the document identified below is a true and correct translation, to the best of my knowledge and ability, of the original Japanese document:

   • Japanese Unexamined Patent Application Publication No. S64-18248

I hereby certify under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed this 16th day of March, 2015.

By: _____

Asami Isomichi