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Novel SOI Technology Using Preferential Polishing

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The paper describes a device transfer technique using preferential polishing having considerably different polishing rates between silicon and silicon dioxide to form an SOI structure by extracting only a device layer from a wafer by using the field oxide layer within the device layer as a polishing stopper, and bonding the device to an insulating substrate. As a result of applying this technique to bipolar and MOS devices, a notable improvement in the voltage resistance was achieved without degrading transistor characteristics.

1. Introduction

SOI (silicon-on-insulator) technology for forming LSI's on insulators is important for achieving high speed LSI's, as well as increasing their breakdown voltage and radiation resistance.

Conventional exemplary SOI forming methods include heteroepitaxy, such as SOS (silicon on sapphire)[1], for example, recrystallization using a laser[2] and an electron beam[3], and single-crystal separation, such as SIMOX (separation by implanted oxygen)[4]. However, these methods have not been able to produce crystals of high enough quality to form VLSI's.

This gave rise to the development of a device transfer technique where only the device layer from the silicon wafer which has completed a device formation process is extracted and transferred onto an insulator. This technique, although depends on how the device layer and insulator are bonded, can form a SOI structure at low temperatures. A device transfer technique was first reported by Nielen, et al.[5] They used etching as a method to remove the substrate while leaving only the device layer behind. Utilizing the dependency of etching rates on impurity concentrations, they formed the device by forming an epitaxial layer on a substrate having a high impurity concentration. However, this method requires epitaxial growth, as well as a high impurity concentration substrate, thereby restricting the type of devices that can be formed.

Meanwhile, chemical mechanical polishing has been widely used in silicon wafer processing, and is characterized by the planarization ability without imparting strain. Moreover, using an amine for the chemical solution, the processing rate for silicon becomes markedly higher than that of silicon dioxide. This is referred to as "preferential polishing."

In preferential polishing, field oxide layers, which are provided in the device layers for separating individual transistors, can serve as processing stoppers, enabling the extraction of only the device layers[6].

This paper discusses an SOI structure which was formed by separating only a device layer by using preferential polishing.

2. Preferential Polishing

Polishing is a method for processing a wafer by pressing the wafer against the surface of a polishing cloth provided on a rotary disk, which is operated while supplying a processing solution.

Preferential polishing provides selectivity in processing rates, and the materials having the selectivity vary depending on the chemical solutions used. Generally speaking, ethylenediamine pyrocatechol is known as an etchant for silicon. The silicon etching mechanism using this etchant[7] is such that $Si(OH)_6^{2-}$ are formed on the silicon surface by the ionization and redox reactions of amine, which are then chelated with pyrocatechol and dissolved in the solution.

In preferential polishing, the removal of $Si(OH)_6^{2-}$ with pyrocatechol is replaced with a mechanical action, i.e., "wiping" with a polishing cloth. The polishing is performed in two stages: a chemical reaction process by amine, water, and silicon, and a mechanical removal process of "wiping" with the polishing cloth.

FIG. 1 shows the results of the experiments performed to confirm the two stages of preferential polishing.

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Silicon is slightly etched by amine. Silicon is not polished with water alone. Polishing becomes possible only when amine is used in the chemical solution, and the combined effect of the chemical reaction of amine and the mechanical action of the polishing cloth allows the polishing to progress. Silicon dioxide, on the other hand, does not react with amine, and thus is not polished at all.

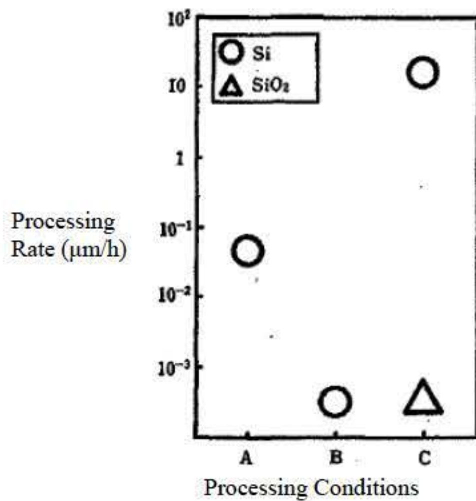

FIG. 1
Preferential polishing mechanism. Polishing conditions are A: chemical etching with an aqueous amine solution, B: polishing with water at a pressure of 1.9×10^4 Pa, and C: polishing with an aqueous amine solution at a pressure of 1.9×10^4 Pa.
Si: n-type (100), 8 to 10 Ω·cm, SiO_2: thermal oxide film grown at 950°C.

FIG. 1 shows the case of an n-type (100) orientation silicon wafer. The same tendency is shown in cases of a p-type and other orientations (111) and (110). The chemical etching rate for the (111) orientation is about 1/10 of those of the (100) and (110) orientations, but no difference in polishing rate based on orientations was observed. Thus, the etching rate using amine is presumably limited by the separation of the reaction products from the silicon surface.

FIG. 2 shows a cross-sectional view of a wafer having a field oxide film being polished. In the region where silicon dioxide is not exposed at the surface (on the right hand side of the figure), $Si(OH)_6^{2-}$ formed at the surface is wiped off by a polyester fiber polishing cloth, and polishing progresses. In the region where silicon dioxide is exposed (on the left hand side of the figure), silicon dioxide prevents the wiping of $Si(OH)_6^{2-}$ because the polishing cloth is flat-shaped. As a result, the polishing does not progress, and thus the silicon (device layer) surrounded by the field oxide can be preserved.

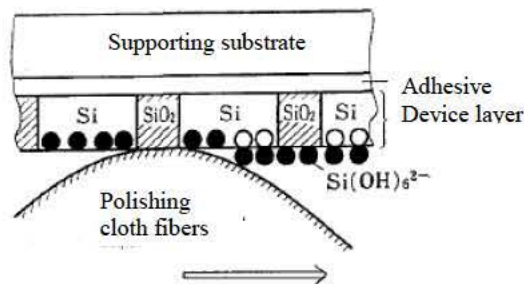

FIG. 2
Polishing of a substrate having a field oxide film. The oxide film is not exposed on the right side of the figure, and $Si(OH)_6^{2-}$ is removed by a polishing cloth. The oxide film is exposed on the left side of the figure, and $Si(OH)_6^{2-}$ is not removed.

FIG. 3 is a cross-sectional scanning electron micrograph of the substrate with the oxide film exposed after forming 2 μm wide, 3 μm deep trenches in a device layer, burying the polysilicon by covering the surface with a 200 nm oxide film, and polishing from the opposite side of the device surface (back surface). Polishing stopped at the oxide film having a thickness of only 200 nm, and the polished surface was flat. This indicates that the polishing progressed on the flat surface, and at the instant silicon dioxide was exposed, polishing of silicon no longer progressed. Thus, preferential polishing enables processing using the field oxide film as a stopper, removing the substrate while leaving only the device layer behind.

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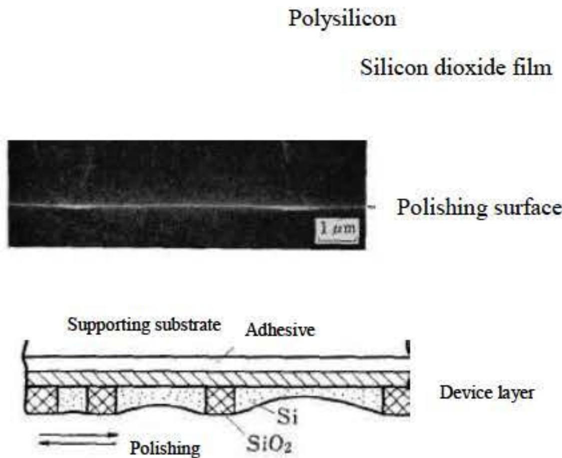

FIG. 3
Scanning electron micrograph of a cross section of a substrate with the field oxide film exposed. The field oxide film is covered with silicon dioxide of 200 nm in thickness on the surface, and includes trenches filled with polysilicon.

FIG. 4
Schematic cross-sectional view of a substrate illustrating the size and the polished shape of a transistor (silicon) region.

Since the polishing cloth is composed of fibers, the greater the spaces between silicon dioxide which is a stopper, i.e., the greater the areas of open silicon regions, the easier for the polishing cloth fibers to enter, resulting in excessive polishing and creating recesses as shown in FIG. 4. This indicates that the smaller the areas of open silicon regions, i.e., the higher the integration density of a device, the more effective preferential polishing becomes.

3. Formation of SOI by Device Transfer

FIG. 5 shows the device transfer process. FIG. 5(a) illustrates a silicon wafer on which a device has already been formed, but before processing, and (b) illustrates the state where the device surface is bonded to a supporting substrate A. An epoxy- or polyimide-based adhesive is used. As illustrated in FIG. 5 (c), most of the thickness (about 430 μm) of the wafer on which the device has been formed is removed by lapping (rough polishing). Alumina was used as abrasive grains. The remainder was removed by preferential polishing to leave only the device layer behind. Since lapping utilizes the action of abrasive grains, strain remains on the processed surface although the processing rate is high. Accordingly, at least 40 μm is removed by polishing in order to impart no strain to the device layer. Since the relationship between the lapping amount and time is linear, the processing amount is easily controlled by time.

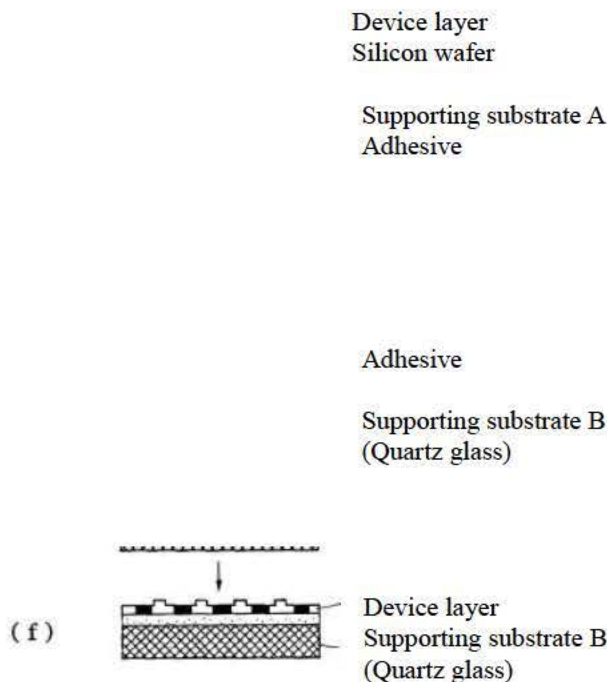

FIG. 5
Device transfer process: (a) silicon wafer on which a device layer is formed, (b) bonding of the silicon wafer and supporting substrate A, (c) removal of the silicon wafer (lapping + preferential polishing), (d) bonding with supporting substrate B (quartz glass wafer), (e) removal of the supporting substrate A, and (f) removal of an adhesive, thereupon the device layer is transferred to supporting substrate B.

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As shown in FIG. 5 (d), the device layer left behind by preferential polishing is bonded to a supporting substrate B (quartz glass). As shown in FIG. 5 (e), the supporting substrate A is removed by lapping and preferential polishing in the same manner as that for exposing the device surface. In this case, the adhesive serves as a polishing stopper. Finally, as illustrated in FIG. 5 (f), the adhesive is removed by oxygen plasma ashing to complete the process of transferring only the device active layer onto another supporting substrate across the entire wafer.

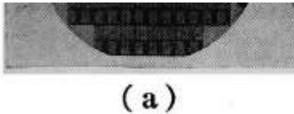

FIG. 6
A 100-mm-diameter wafer; (a) before transfer, and (b) after transfer. On the wafer, an array of 10,000 bipolar transistor chips is formed within the device layer of 1 μm in thickness. After the transfer, letters can be seen through the device layer on the wafer.

Figure 6 shows the state where an array of 10,000 parallel connected bipolar transistors formed on a wafer of 100 mm in diameter was transferred onto a quartz glass wafer. The device layer is 1 μm in thickness, and the characters can be seen through the wafer after the transfer. As shown in FIG. 7, the transistor structure is formed within a 1-μm-thick epitaxial layer, the depths of the base and emitter being 0.2 μm and 0.08 μm, respectively, and the LOCOS (local Oxidation of Silicon) isolation layer serves as a preferential polishing stopper.

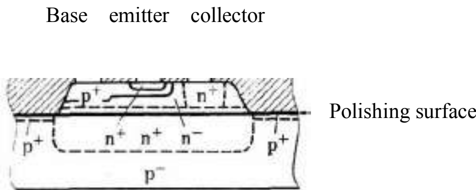

FIG. 7
Structure of a bipolar transistor. The transistor is formed in a 1-μm-thick epitaxial layer and has a base depth of 0.2 μm and an emitter depth of 0.08 μm.

FIG. 8 shows the characteristics of the transferred transistor array: (a) the collector-base breakdown voltage, and (b) the collector current and collector voltage. There were no changes observed in these characteristics before or after the transfer, meaning that preferential polishing did not cause any damage to the transistors. Furthermore, the breakdown voltage between the transistors is considerably improved from 12 V before the transfer to 100 V or higher. This is because the breakdown voltage before the transfer depends on the n^+-p^+ junction between the buried collector and channel stopper regions, as opposed to the pressure resistance of the adhesive after the transfer.

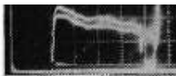

FIG. 8
Characteristics of the bipolar transistor array after the transfer: (a) collector-base breakdown voltage, and (b) the collector current vs. the collector voltage.

FIG. 9 is a scanning electron micrograph of a cross section of the substrate after transferring a 0.4-μm-thick MOSFET device layer onto a quartz glass. As is clear from the figure, the use of preferential polishing is also applicable to thinning of a submicron-thickness device.

The foregoing transfer process requires two polishing steps. It is possible to create a hole from the rear surface of the device layer exposed by polishing through the silicon dioxide layer to the aluminum pad, as shown in FIG. 5(c), to expose the aluminum electrode at the rear surface for connection (e.g., wire bonding)[8)] to perform only one polishing step. This method not only shortens the device transfer process, but also provides superior

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characteristics, such as forming wiring on both surfaces of the device layer, as well as controlling the substrate potential, which was difficult to do using conventional SOI techniques.

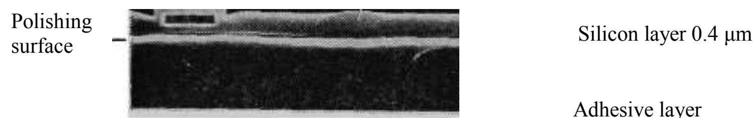

FIG. 9
Scanning electron micrograph of a cross section of a substrate after the transfer of MOS transistors.

4. Conclusions

Preferential polishing progresses in two stages of chemical reaction and mechanical removal, and is capable of polishing silicon at a rate that is at least 10^4 times that of silicon dioxide. This technology enables the formation of an SOI device by device transfer where the wafer is thinned by utilizing the oxide film formed within the device layer as a stopper, and transferring only the device active layer onto an insulating substrate.

Various applications are conceivable for the device transfer technology because of its ability to form only a device layer on a variety of substrates. For example, transferring a device layer onto a high thermal conductive substrate would resolve thermal problems. Bonding or stacking different types of devices together, such as gallium arsenide devices and silicon devices, for example, or stacking the silicon devices together, would enable the formation of a hybrid, multifunctional, high integration density three-dimensional LSI, and so on – dreams keep growing. In order to realize these, however, technological development in interlayer connection, etc., is necessary.

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