United States Patent [19]

Hayashi et al.

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[54] **METHOD OF MAKING A THIN FILM TRANSISTOR**

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[73] Assignee: **Sony Corporation,** Tokyo, Japan

[21] Appl. No.: **433,449**

[22] Filed: **Nov. 13, 1989**

Related U.S. Application Data

[63] Continuation of Ser. No. 265,798, filed as PCT JP88/00078 on Jan. 29, 1988, published as WO88/05961 on Aug. 11, 1988, abandoned.

[30] **Foreign Application Priority Data**

Jan. 30, 1987 [JP] Japan .... 62-12445[U]
Sep. 25, 1987 [JP] Japan .... 62-241932[U]

[51] **Int. Cl.⁵** **H01L 21/70**
[52] **U.S. Cl.** **437/41**; 437/29; 437/40; 437/62; 437/83; 437/86; 437/186; 437/915; 437/974; 357/23.7
[58] **Field of Search** 437/29, 34, 40, 41, 437/83, 86, 186, 225, 249, 974, 915; 357/23.7

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Primary Examiner—Brian E. Hearn
Assistant Examiner—Tom Thomas
Attorney, Agent, or Firm—Hill, Van Santen, Steadman & Simpson

[57] **ABSTRACT**

The present invention relates to a semiconductor device in which a semiconductor element is formed on a semiconductor layer (3) supported on a substrate (1) via at least insulating layers (2) and (4) as shown in FIGS. 1 and 2 and a method of fabricating the same. The semiconductor layer (3) has wiring layers (5) and (6) on both surfaces thereof, thus leading itself well for increasing the density of wiring and for increasing the operation speed in a large-scale integrated circuit device.

1 Claim, 3 Drawing Sheets

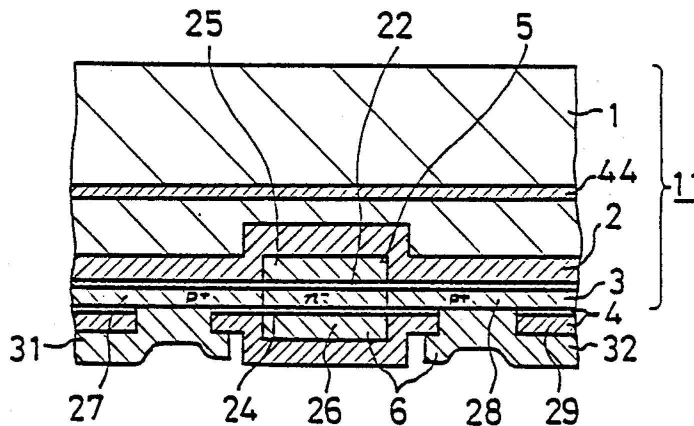

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FIG. 1A

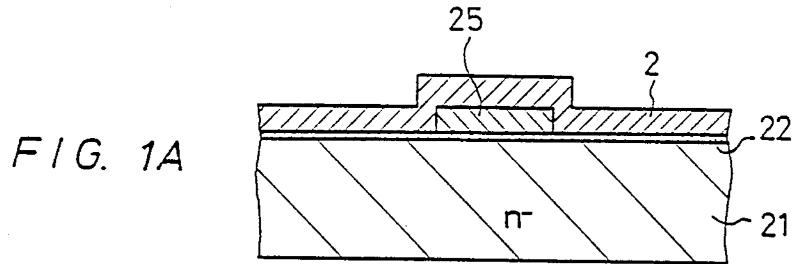


FIG. 1B

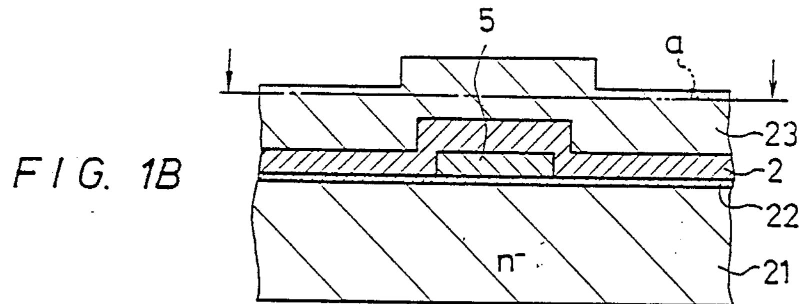
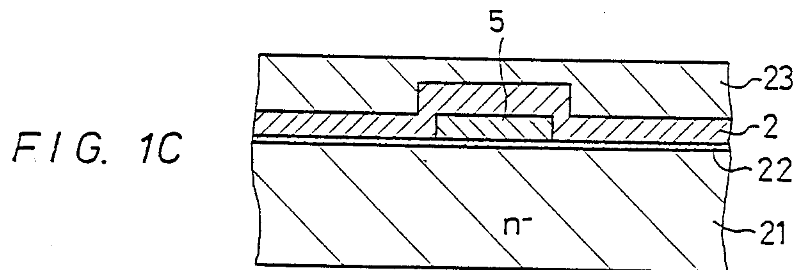


FIG. 1C



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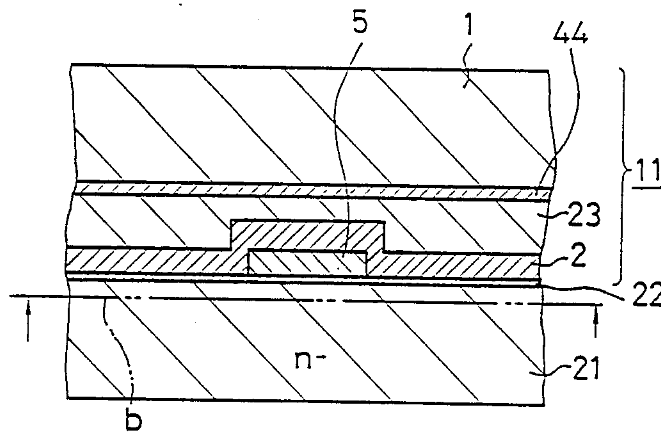

FIG. 1D

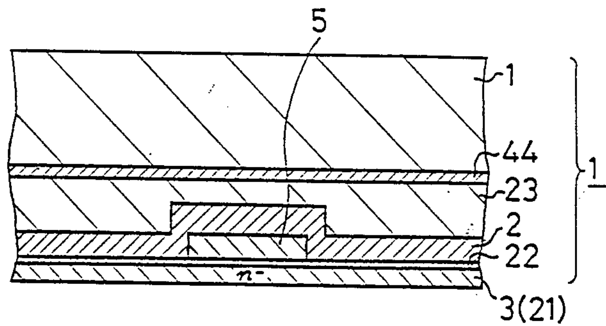

FIG. 1E

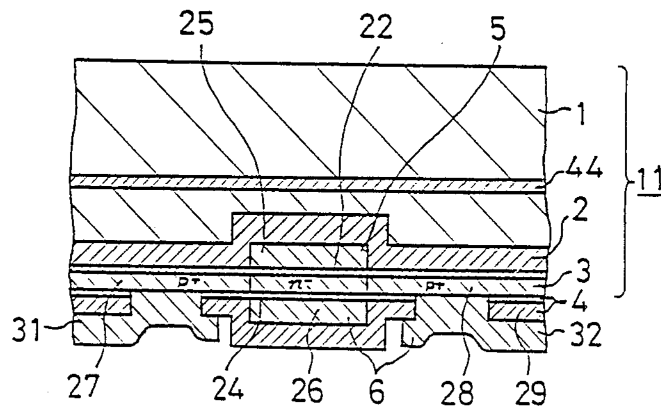

FIG. 1F

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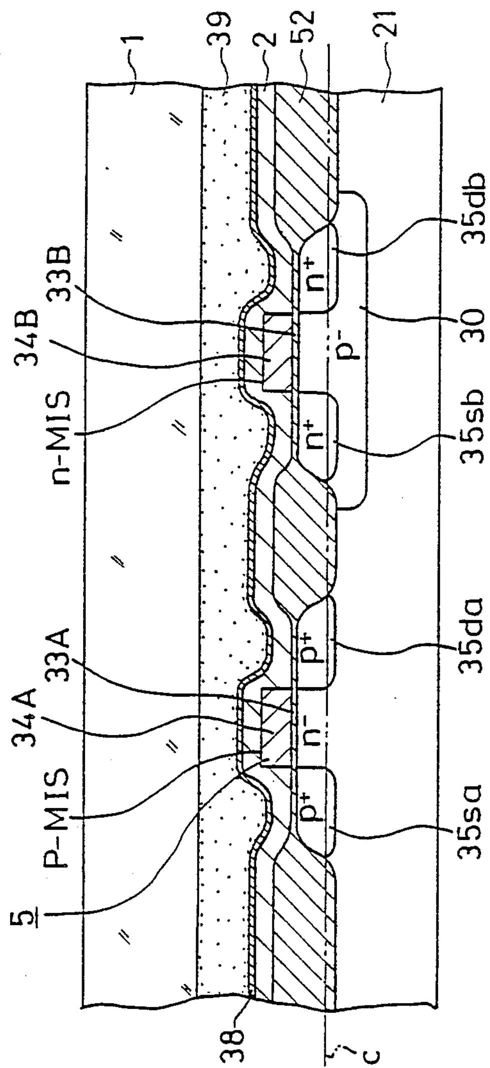

FIG. 2A

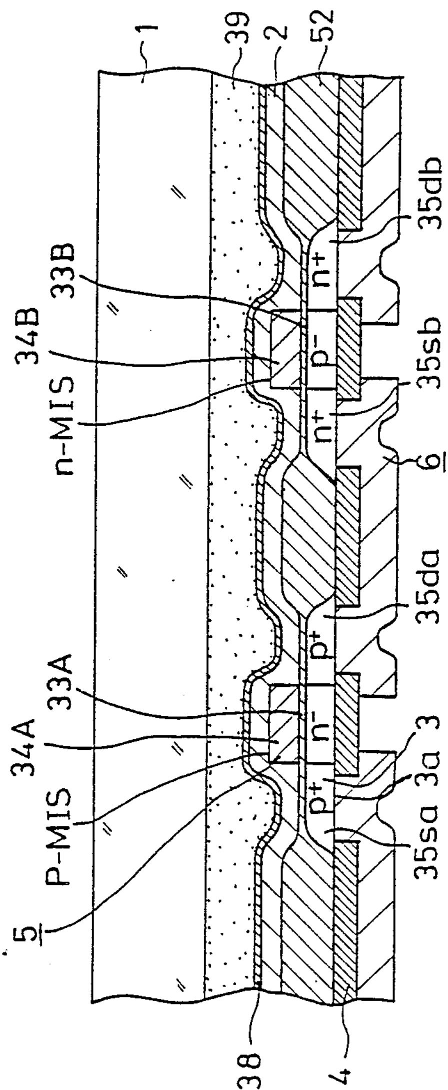

FIG. 2B

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METHOD OF MAKING A THIN FILM TRANSISTOR

This is a continuation, of application Ser. No. 265,798, filed as PCT JP88/00078 on Jan. 29, 1988, published as WO88/05961 on Aug. 11, 1988, now abandoned.

TECHNICAL FIELD

The present invention relates to a semiconductor device using a thin film semiconductor layer and a method of fabricating the same and particularly to a semiconductor device which has high-density wiring layers such as a gate electrode, a wiring electrode and so on formed on both sides of a semiconductor layer and a method of fabricating the same.

Also, the present invention relates to a semiconductor device which is formed on a semiconductor layer on an insulating substrate and is capable of high-speed operation and a method of fabricating the same.

BACKGROUND ART

As a semiconductor device using a thin film semiconductor layer formed on an insulating substrate, the present applicant has proposed an MIS transistor having a 100 to 750 angstrom thick-semiconductor layer which can be operated at high speed as is disclosed in U.S. Patent applications, Ser. Nos. 683860 and 683932.

Further, JOURNAL OF ELECTROCHEMICAL SOCIETY: SOLID-STATE SCIENCE AND TECHNOLOGY (Journal of Electrochemical Society: SOLID-STATE SCIENCE AND TECHNOLOGY), Vol. **120**, No. **11**, pp. **1563** to **1566** discloses a method in which a silicon substrate is bonded on an insulating substrate and then the silicon substrate is lapped or polished to have a predetermined thickness.

This kind of semiconductor device formed on the insulating substrate can be operated at high speed because a parasitic capacitance between its semiconductor region and the substrate can be reduced.

Even this kind of semiconductor device is, however, requested to make its wiring in a multi-layer fashion or to make its wiring in a very small layout pattern with the increase of integration of semiconductor elements. In this case, the wiring is made only on the upper portion of the semiconductor layer so that due to a difference by the insulating film or contact-hole between the wiring on the under layer and the upper layer. There is caused a step-cut in the wiring on the upper layer. As a result, there is then a problem that reliability of the semiconductor device is lowered.

DISCLOSURE OF INVENTION

The present invention is to provide a semiconductor device which can be operated at high speed because it has a less parasitic capacitance for a substrate.

Also, the present invention is to provide a semiconductor device formed on a thin film semiconductor layer supported on an insulating substrate and a method of fabricating the same.

Particularly, the present invention is to provide an MIS transistor formed on a thin film semiconductor layer supported on an insulating substrate and a method of fabricating the same.

Further, the present invention is to provide a semiconductor device which can increase the density of wiring and a method of fabricating the same.

Further, the present invention is to provide a semiconductor device which can prevent reliability from being lowered by a step-cut in the multi-layer wiring and a method of fabricating the same.

Furthermore, the present invention is to provide a semiconductor device in which the wiring of semiconductor elements can be made with an increased freedom and a method of fabricating the same.

In addition, the present invention is to provide a semiconductor device having a multi-layer wiring which can be made with smaller pattern by making the upper portion of the wiring flat and a method of fabricating the same.

In order to achieve the above-mentioned objects, the present invention is to provide a semiconductor device in which semiconductor elements are formed on a semiconductor layer supported on a substrate via at least an insulating layer and a method of fabricating the same. The semiconductor layer has wiring layers formed on both surfaces thereof, thus leading itself well for increasing the density of wiring and for increasing the operation speed in a large-scale integrated circuit device.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1** is a process diagram of an embodiment of a semiconductor device according to the present invention and a method of fabricating the same and FIG. **2** is a process diagram of another embodiment of a semiconductor device according to the present invention and a method of fabricating the same.

BEST MODE FOR CARRYING OUT THE INVENTION

A method of obtaining a double-side gate type MIS semiconductor device which can improve the effective carrier mobility will be described with reference to FIG. **1**. In this case, as shown in FIG. **1**A, a single crystal silicon semiconductor substrate **21** of, for example, n− type is provided. A gate insulating film **22** is formed on its one major surface by means of a surface thermal oxidation treatment or the like, on which a first gate electrode **25**, i.e., a first wiring layer **5** formed of a polycrystalline silicon layer having low resistivity is formed with a predetermined pattern, for example, with a predetermined wiring pattern covering the first gate electrode **25**. The first wiring layer **5**, i.e., the first gate electrode **25** in the illustrated example is formed by depositing a polycrystalline silicon layer on the entire surface by, for example, chemical vapor deposition method (CVD method) or the like and patterning the same by means of a photolithography or the like.

As shown in FIG. **1**B, an intermediate layer **23** made of, for example, a polycrystalline silicon or the like of relatively large thickness is deposited on an insulating layer **2** by means of the CVD method or the like.

Then, as shown in FIG. **1**C, the intermediate layer **23** is etched flat from its surface side to the position shown by a chain line a in FIG. **1**B by techniques such as, for example, mechanical grading, mechanical and chemical polishing or the like.

As shown in FIG. **1**D, an insulating layer **44** made of, for example, an SiO_2 or the like is formed on the flat surface of the intermediate layer **23** by a surface thermal oxidation process or the like. On this insulating layer, a single crystal or polycrystalline silicon substrate **1** is bonded or the substrate **1** made of polycrystalline silicon is grown by means of the CVD method or the like. Then, the semiconductor substrate **21** is supported on a supporting member **11** which includes this substrate **1**.

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