United States Patent [19]

Matsuda et al.

[11] **4,131,909**

[45] **Dec. 26, 1978**

[54] **SEMICONDUCTOR INTEGRATED CIRCUIT ISOLATED THROUGH DIELECTRIC MATERIAL AND A METHOD FOR MANUFACTURING THE SAME**

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[73] Assignee: **Tokyo Shibaura Electric Co., Ltd.**, Tokyo, Japan

[21] Appl. No.: **735,784**

[22] Filed: **Oct. 26, 1976**

[30] **Foreign Application Priority Data**

Oct. 25, 1975 [JP] Japan 50-128773

[51] **Int. Cl.**[2] **H01L 27/12**; H01L 29/78; H01L 27/02; H01L 29/04

[52] **U.S. Cl.** **357/49**; 357/23; 357/41; 357/59; 357/67; 29/571

[58] **Field of Search** 357/23, 41, 49, 59, 357/67

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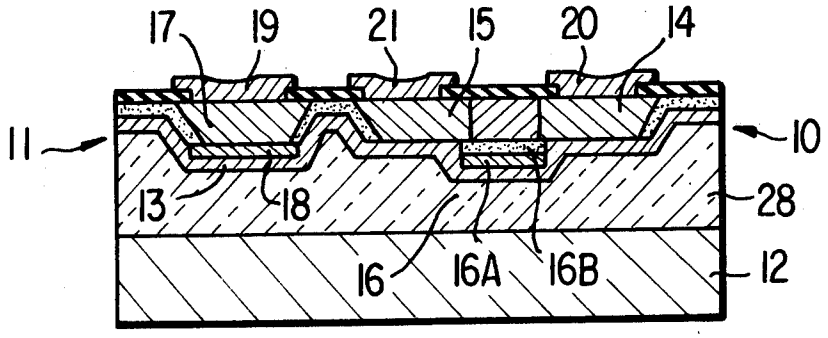
Primary Examiner—William D. Larkins
Assistant Examiner—Gene M. Munson
Attorney, Agent, or Firm—Oblon, Fisher, Spivak, McClelland & Maier

[57] **ABSTRACT**

A semiconductor integrated circuit includes first and second island regions, surrounded by a bottomed dish-like dielectric layer formed on one side of a support body. A MOS transistor element is formed in the first island region, whose gate region is located at the bottom side of the island region. The gate electrode is connected to a bottom portion of the second island region, which is used as a gate electrode contact region, in the support body using a interconnection lead. There is a method for manufacturing the above device.

6 Claims, 13 Drawing Figures



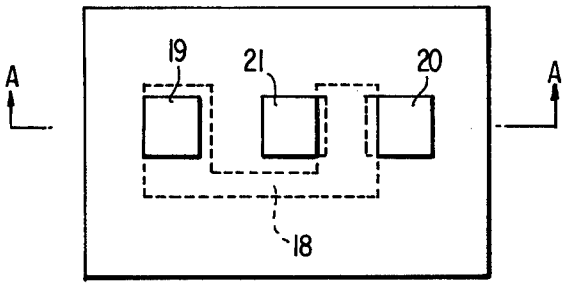


FIG.1

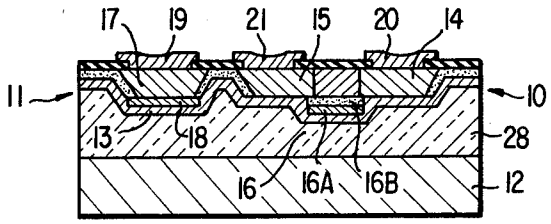


FIG.2

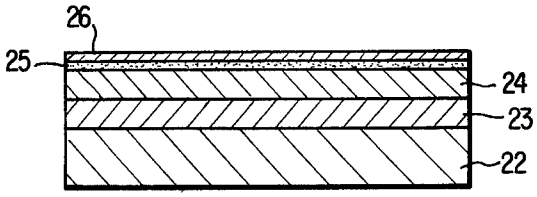


FIG.3A

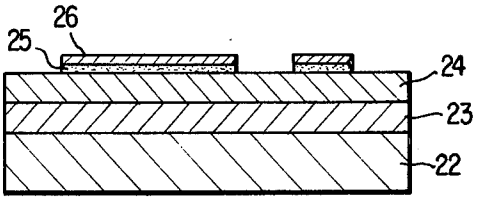


FIG.3B

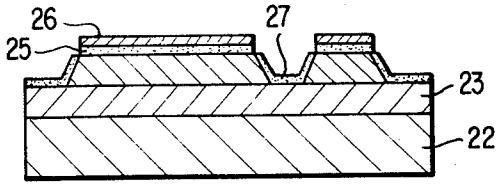


FIG. 3C

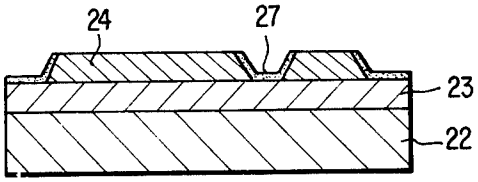


FIG. 3D

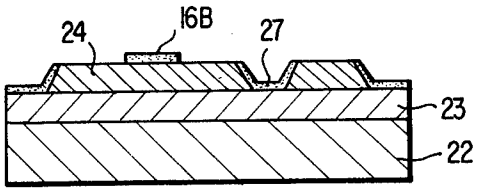


FIG. 3E

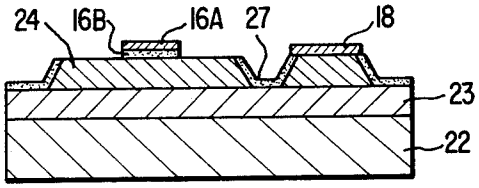


FIG. 3F

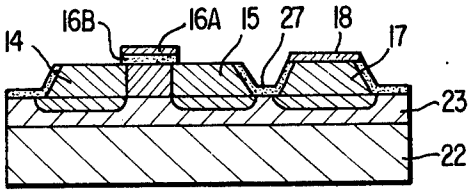


FIG. 3G

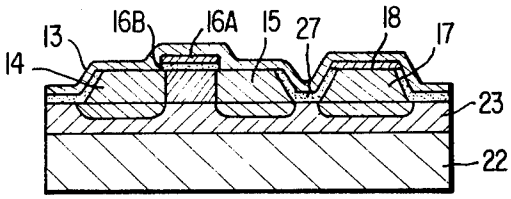


FIG. 3H

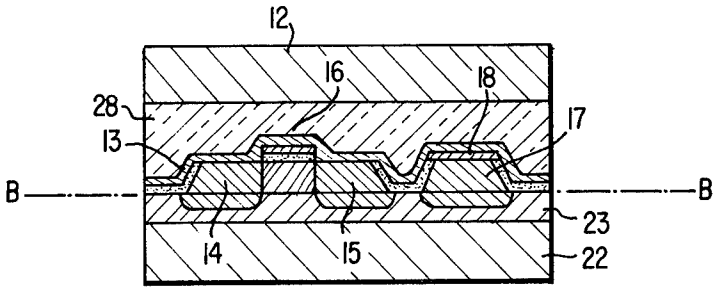


FIG. 3I

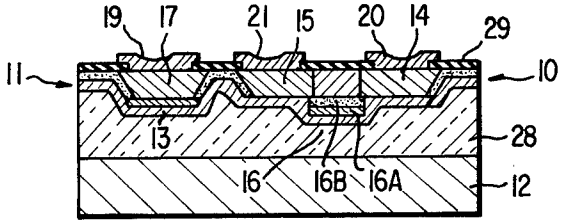


FIG. 3J

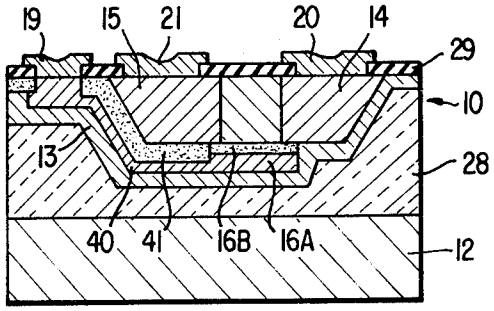


FIG. 4

SEMICONDUCTOR INTEGRATED CIRCUIT ISOLATED THROUGH DIELECTRIC MATERIAL AND A METHOD FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

Field of Invention

This invention relates to a semiconductor integrated circuit whose island region is electrically isolated through a dielectric layer, and a method for manufacturing the same.

Description of the Prior Art

It is known that a digital integrated circuit using Metal Oxide Semiconductor Transistor (hereinafter referred to merely as MOS transistor) is superior to a circuit using bipolar transistors in such points as integration density, power consumption and ease of manufacture.

However, in operating speed, the former is inferior to the latter. To overcome this shortcoming of the MOS integrated circuit, namely to increase the operating speed, the SOS (Silicon on Sapphire or Spinel) technique was recently developed. This technique is as follows: after growing a silicon layer having 1 μm thickness on one surface of sapphire monocrystalline substrate by using epitaxial process, a selective etching is made to remove the epitaxial layer selectively, leaving some portions where circuit elements are formed. This technique has some merits as follows compared with the conventional one.

1) High speed of the circuit operation owing to the decrease of parastic capacitance according to the decrease of PN junctions.

2) High integration density of the integrated circuit owing to the decrease of the area of isolation region between circuit elements. However, this SOS technique is accompanied with such inconvenient phenomenon as lattice defects owing to the difference of lattice constant and crystal construction between silicon and sapphire, occurrence of aluminum impurity by reaction of the sapphire substrate with silicon layer and warp of the sapphire substrate owing to the difference of the expansion coefficients of both. These increase the leakage current of the device two to three fold compared with bulk silicon's, which makes the power consumption high. Furthermore, the carrier mobility becomes smaller sharply, and accordingly, the operating speed of the integrated circuit is decreased. For these reasons, it is difficult to apply this SOS technique to CMOS (Complementary Metal Oxide Semiconductor) circuit and the Dynamic circuit.

On the other hand conventionally known is a semiconductor integrated circuit in which an electrical insulation is made between semiconductor elements using a dielectric layer. A plurality of semiconductor elements of the integrated circuit are arranged at a predetermined interval on one side of a semiconductor polycrystalline layer, and a dielectric layer or insulator separation layer is formed in a manner to insulate the semiconductor elements from the polycrystalline layer. In this integrated circuit, the floating capacitance is very small, so that high break down voltage is obtained. Accordingly the abovementioned technique is especially used in the bipolar integrated circuit in which the thickness of monocrystalline layer is about 3 μm to 10 μm, so that therefore, the scatter of the thickness is of little matter. However in the MOS integrated circuit, the thickness of the monocrystalline layer is about 1 μm. Accordingly it is very difficult to make the thickness constant within a scattering value of ±0.1 μm using a lapping method or an etching process. Therefore, application of this technique to the MOS integrated circuit is very difficult.

Furthermore, in the process where a polycrystalline layer is formed by gas phase growth, at first the size of a polycrystalline particle is small. However it becomes larger and larger with the advance of the polycrystalline growth, which causes a warp of the semiconductor substrate owing to the difference of the expansion coefficient of the polycrystalline layer in the direction of its depth. Furthermore, warping occurs also owing to the difference of expansion coefficient between the polycrystalline layer and the monocrystalline layer in which the semiconductor element is formed. This warp of the semiconductor substrate is difficult to be got rid of, and make the subsequent photoetching process difficult.

For these reasons, the prior art as above mentioned is unsuitable for manufacturing the semiconductor integrated circuit.

SUMMARY OF THE INVENTION

This invention overcomes the problems arising from the processing sequence and the construction of the prior art wherein the polycrystalline layer is grown by gas phase.

One object of this invention is to provide a method capable of easily manufacturing a semiconductor integrated circuit isolated through dielectric material.

Another object of this invention is to provide a semiconductor integrated circuit having an island region isolated through dielectric material, and having a MOS transistor element in the island region, whose gate region is located at the bottom side of the island region.

Yet another object of this invention is to provide a semi-conductor integrated circuit without warp of the support body.

Further object of this invention is to provide a semiconductor integrated circuit whose power consumption is small and operating speed is very high.

In one aspect of this invention, a semiconductor integrated circuit comprises a support body, at least one bottomed enclosed dielectric layer whose one end is open at one surface of the support body forming an island region, a MOS transistor element in the island region having source, drain and gate regions, wherein said source and drain regions are formed adjacent to said one surface of the support body and the gate region is formed at a bottom portion of the island region.

In another aspect of this invention, a method for manufacturing a semiconductor integrated circuit comprises the steps of: forming a mask layer on one side surface of first semiconductor substrate having first conductivity; removing at least two portions of the mask layer; etching the semiconductor substrate down to a predetermined depth through the exposed portions thereof to form first and second mesa regions; forming a gate insulating layer at a portion on the top surface of the first mesa region; forming source and drain regions in the first mesa region and gate electrode contact region in second island region so as to reach to the bottom of the mesa regions respectively, by diffusing an impurity having second conductivity type forming a gate electrode on said gate insulating layer and an intercon-

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