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PD-92651

GRAY EXAMINER

A1M1/1210

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ART UNIT	PAPER NUMBER
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1107

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DATE MAILED:

12/13/93

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

This application has been examined Responsive to communication filed on 5-27-98 This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), — days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

- 1. Notice of References Cited by Examiner, PTO-892.
- 2. Notice re Patent Drawing, PTO-948.
- 3. Notice of Art Cited by Applicant, PTO-1449.
- 4. Notice of Informal Patent Application, Form PTO-152.
- 5. Information on How to Effect Drawing Changes, PTO-1474.
- 6.

Part II SUMMARY OF ACTION

- 1. Claims 1-21 are pending in the application.
Of the above, claims _____ are withdrawn from consideration.
- 2. Claims _____ have been cancelled.
- 3. Claims _____ are allowed.
- 4. Claims 1-21 are rejected.
- 5. Claims _____ are objected to.
- 6. Claims _____ are subject to restriction or election requirement.
- 7. This application has been filed with Informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
- 8. Formal drawings are required in response to this Office action.
- 9. The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are acceptable. not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
- 10. The proposed additional or substitute sheet(s) of drawings, filed on _____, has (have) been approved by the examiner. disapproved by the examiner (see explanation).
- 11. The proposed drawing correction, filed on _____, has been approved. disapproved (see explanation).
- 12. Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has been received not been received been filed in parent application, serial no. _____; filed on _____.
- 13. Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
- 14. Other

EXAMINER'S ACTION

PTOL-326 (Rev. 9-89)

Claims 1-7, 10-18 and 21^{are} rejected under 35 U.S.C. § 103 as being unpatentable over Riseman in combination with Yasumoto.

Riseman teaches a device made by the method comprising the steps of providing a silicon substrate 21, a silicon dioxide etch-stop layer 20 overlying the silicon layer and a single crystal silicon wafer 10 overlying the SiO₂ layer; forming a microelectronic circuit element 13 in the single crystal wafer; etching the silicon substrate 21 with a liquid etchant down to the silicon dioxide layer, and forming an electrical connection 27 to the circuit element through the patterned 25 silicon dioxide layer and through the wafer. See column 4, line 52 to column 7, line 16.

However, Riseman does not teach a device made by the method of attaching the front surface of the single crystal wafer to a second substrate containing a second microelectronic circuit element and electrically contacting the first and second circuit elements.

Nonetheless, Yasumoto teaches such an embodiment. See column 4, line 56 to column 7, line 41.

It would have been obvious to combine the methods of Riseman and Yasumoto because the method of Yasumoto would increase circuit density.

Claims 8 and 20 are rejected under 35 U.S.C. § 103 as being unpatentable over Riseman in combination with Yasumoto as applied

to claims 1-7, 10-18 and 21 above, and further in view of Raschke.

Riseman in combination with Yasumoto teaches all the essential elements of claims 8 and 20 except for the steps of placing a layer of epoxy between the single crystal wafer and the second substrate and degassing and curing the epoxy.

Nevertheless, Yasumoto teaches that the two circuits are adhered by an adhesive resin. See column 7, lines 21-24.

In addition, Raschke teaches a method of adhering circuit elements using epoxy resin and degassing the resin. See column 3, lines 38-47.

Because the method of Raschke enables the adhesion of circuit elements, it would have been obvious to combine the methods of the applied prior art.

Claim 9 is rejected under 35 U.S.C. § 103 as being unpatentable over Riseman in combination with Yasumoto as applied to claims 1-7, 10-18 and 21 above, and further in view of Stoller.

Riseman in combination with Yasumoto teaches all the essential elements of claim 9, except for the step of fixing the second element to an etching support that is resistant to an attack by an etchant.

Still, Stoller teaches that such a support 22, 24 enables wafer support during etching. See column 2, line 48 to column 3,

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line 10. Hence it would have been obvious to combine the applied prior art methods.

Claim 19 is rejected under 35 U.S.C. § 103 as being unpatentable over Riseman in combination with Yasumoto as applied to claims 1-7, 10-18 and 21 above, and further in view of applicant's admitted prior art and admissions of non-criticality.

Riseman in combination with Yasumoto does not explicitly teach the specific claimed substrate dimensions.

Notwithstanding, applicant teaches that these dimensions are both conventional and non-critical, and that they are simply dictated by design constraints. See page 7, lines 1-19.


Hence, such dimensions would have been obvious.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill whose telephone number is (703) 308-2947.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0661.

D

DGraybill:vr
December 06, 1993


Dilk Chaudhuri
Supervisory Patent Examiner
Patent Examining Group 110