IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

RAYTHEON COMPANY, *Plaintiff* vs. SAMSUNG ELECTRONICS CO., LTD., ET AL., *Defendants*	Civil Action No. 2:15-CV-341-JRG-RSP LEAD CASE JURY TRIAL DEMANDED

JOINT CLAIM CONSTRUCTION AND PREHEARING STATEMENT PURSUANT TO LOCAL PATENT RULE ("P.R.") 4-3

Pursuant to the Court's Docket Control Order of August 17, 2015 (Dkt. 60), and P.R. 4-3, Plaintiff RAYTHEON COMPANY and Defendants SONY KABUSHIKI KAISHA (A/K/A SONY CORPORATION), SONY CORPORATION OF AMERICA, SONY SEMICONDUCTOR CORPORATION, SONY EMCS CORPORATION, SONY ELECTRONICS INC., SONY MOBILE COMMUNICATIONS INC., SONY MOBILE COMMUNICATIONS AB, SONY MOBILE COMMUNICATIONS (USA) INC.(collectively, the "Sony Defendants"), OMNIVISION TECHNOLOGIES, INC. ("OmniVision"), APPLE INC. ("Apple"), SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG TELECOMMUNICATIONS AMERICA, LLC (collectively, the "Samsung Defendants"), hereafter referred to as "the Parties," hereby submit this Joint Claim Construction and Prehearing Statement ("Joint Statement").

The Joint Statement addresses the terms, phrases or clauses in U.S. Patent No. 5,591,678 (the "'678 Patent"), entitled "Process of Manufacturing a Microelectronic Device Using a Removable Support Substrate and Etch-Stop." The included terms, phrases, or clauses for the '678 Patent were identified by one or more parties pursuant to P.R. 4-1 as requiring construction.

I. Agreed Claim Constructions (P.R. 4-3(a))

The parties agree on the construction of the following phrase:

Claim Term	Claims	Construction
"degassing and curing the epoxy"	Claims 10 and 18	to remove gas and solidify the epoxy

II. Disputed Claim Constructions (P.R. 4-3(b))

Pursuant to P.R. 4-3(b), the Plaintiff's and Defendants' proposed constructions of disputed claim terms, phrases, or clauses are reflected in the following table:

Claim Term	Raytheon's Proposal	Defendants' Proposal
"first substrate" (Claims 1, 6-9, 11, 13, and 17-18)	A first solid support material.	A structure that initially has at least three distinct material layers.
"etchable layer" (Claims 1, 5, 10, 11-13, and 17)	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this term to mean, "a portion of the first substrate that is readily etched, relative to the etch stop layer."	A support layer of the first substrate, distinct from the etch-stop layer and the wafer, having an etch rate much higher than that for the etch-stop layer.
"etch-stop layer" (Claims 1-5 and 10-17)	A portion of the first substrate that is etched less readily, relative to the etchable layer.	***Sony Defendants/OmniVision/ Apple*:** A layer of the first substrate, distinct from the etchable layer and the wafer, which stops the etching process by virtue of it having a lower etch rate than the etchable layer. ***Samsung Defendants*:** A layer of

		the first substrate distinct from the etchable layer and the wafer, grown upon the etchable layer used for stopping the etching process.
"overlying" (Claims 1, 11, and 13)	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this term to mean, "lying on."	Lying over or upon.
"wafer" (Claims 1, 3-5, 7-8, 11-13, and 15-17)	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this term to mean, "a portion of the first substrate in or on which the microelectronic circuit element is formed."	***Sony Defendants/OmniVision/ Apple*:** A layer of the first substrate, distinct from the etch-stop layer and the etchable layer, and within which some portion of microelectronic circuit elements are formed. ***Samsung*:** A layer of the first substrate distinct from the etch-stop layer and the etchable layer, deposited on or bonded to the etch-stop layer.
"microelectronic circuit element" (Claims 1, 6-7, 11, 13, and 15)	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this term to mean, "a patterned element in an electrical circuit."	A component of an active circuit element or passive circuit structure.
"attaching" (Claims 1, 7-9, 11, 13, and 18)	Joining together two surfaces.	Fastening or joining.
"second substrate" (Claims 1, 6-9, 11, 13, and 18)	A second solid support material that is part of the complete device.	A structure separate and distinct from the first substrate (as construed) that provides support to the first substrate through the etching process.
"etching" (Claims 1, 2, 9, 10, 11, 13, 14)	No construction necessary. Plain and ordinary meaning. If the Court believes this term	A subtractive process in the course of which a solid is dissolved in liquid chemicals (wet

	requires construction, the Court should construe this term to mean, "removing material with an etchant."	etching) or converted into gaseous compound (dry etching).
"etching away the etchable layer… down to the etch stop layer" (Claims 1, 11, and 13)	Etching the etchable layer to at least the etch-stop layer.	An etching process that removes the etchable layer and then is stopped by the etch-stop layer.
"the step of attaching includes the step of making an electrical contact…" (Claim 7)	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this phrase should mean "making a contact in which current can flow in either direction with minimal resistance."	Electrical contact between the first and second microelectronic circuit elements must be made as part of the step of attaching the first and second substrates together.
The order of the recited method steps (All Claims)	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe that each step is started before the step of etching.	The steps of independent claims 1 and 13 must be performed in the order in which they are recited.

Plaintiff and Defendants also provide the attached **Exhibits A and B**, respectively, in support of their proposed constructions. These Exhibits contain all references from the specification or prosecution history, as well as any extrinsic evidence, that support the proposed constructions. The parties expressly reserve the right to rely on any intrinsic and extrinsic evidence identified by the other party, and any evidence obtained, or that may be obtained, through claim construction discovery. The parties expressly reserve the right to amend, correct, or supplement the claim construction positions and supporting evidence in response to any change of position by another party, in response to information received through claim

construction discovery, including inventor depositions and expert depositions concerning claim construction declarations, or for other good cause.

III. Length of Claim Construction Hearing (P.R. 4-3(c))

The Court set the Claim Construction Hearing to begin at 9:00 a.m. on February 26, 2016 before Judge Payne. The parties request 90 minutes per side (3 hours total) for the hearing.

IV. Live Witness Testimony at Claim Construction Hearing (P.R. 4-3(d))

The parties do not intend to call live witnesses at the Claim Construction hearing.

V. Other Issues (P.R. 4-3(e))

According to the Docket Control Order, there is no prehearing conference scheduled before the claim construction hearing. The parties hereby list the following issues that may be appropriately taken up at a prehearing conference prior to the Claim Construction Hearing:

1. Raytheon contends that the Court should construe terms for Claims 1-18 of the '678 Patent. The Sony Defendants and Apple contend that the Court should only construe terms for Claims 1, 5-10, 13, and 18. OmniVision contends that the Court should only construe terms for Claims 1 and 9-10. The Samsung Defendants contend that the Court should only construe terms for Claims 1 and 8-10.
2. Resolution of the Sony Defendants', OmniVision's and Apple's Motion to Transfer Venue to the Northern District of California, filed July 28, 2015 [D.I. 30], and the Samsung Defendants' Motion to Transfer Venue to the Northern District of California, filed September 8, 2015 [D.I. 69];
3. Resolution of a motion to stay the case pending inter partes review, to be filed shortly. The parties presently are conducting meet and confer discussions over this issue.

Dated: December 9, 2015

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CERTIFICATE OF SERVICE

The undersigned certifies that a true and correct copy of the above and foregoing submission, pursuant to P.R. 4-3, was served on this 9th day of December, 2015, via electronic mail on the below counsel of record who are deemed to have consented to electronic service per Local Rule CV-5(a)(3).

Counsel of record for Defendants Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; Samsung Electronics Co., Ltd.; Sony Kabushiki Kaisha; Sony Corporation of America; Sony Semiconductor Corporation; Sony EMCS Corporation; Sony Electronics, Inc.; Sony Mobile Communications, (USA) Inc.; Sony Mobile Communications AB; Sony Mobile Communications; OmniVision Technologies, Inc.; and Apple, Inc.

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RAYTHEON COMPANY, *Plaintiff* vs. SAMSUNG ELECTRONICS CO., LTD., ET AL., *Defendants*	Civil Action No. 2:15-CV-341-JRG-RSP LEAD CASE JURY TRIAL DEMANDED

EXHIBIT A – Plaintiff Raytheon's Intrinsic and Extrinsic Support for its Proposed Construction of the Disputed Terms of the U.S. Patent No. 5,591,678 Patent

Claim Term	Raytheon's Proposal
"first substrate" (Claims 1, 6-9, 11, 13, and 17-18)	A first solid support material. <u>Intrinsic Evidence Support:</u> '678 specification, *passim*; Figs. 1-4; and, U.S. Patent No. 5,227,656 (Timlin), 4:67; Id. at 9:60, Id. at 10:11; U.S. Patent No. 5,182,624 (Tran), *passim*; U.S. Patent No. 5,043,582 (Cox), *passim*; U.S. Patent No. 5,034,343 (Rouse), *passim*; U.S. Patent No. 5,024,724 (Goesele), *passim*; U.S. Patent No. 4,980,308 (Hayashi), 5:27; and U.S. Patent No. 4,943,491 (Norton), 1:62; U.S. Patent No. 4,829,018 (Wahlstrom), *passim*; U.S. Patent No. 4,783,594 (Schulte), *passim*; U.S. Patent No. 4,467,340 (Rode), *passim*;

	U.S. Patent No. 4,612,083 (Yasumoto), *passim*; U.S. Patent No. 4,169,000 (Riseman), *passim*; U.S. Patent No. 4,131,909 (Matsuda), *passim*; U.S. Patent No. 3,632,219 (Stoller), *passim*; U.S. Patent No. 3,332,137 (Kenney), *passim*. Amendments and Remarks Filed June 4, 1994. Extrinsic Evidence Support: Declaration of Dr. A. Bruce Buckman; Spencer, Donald D. *Webster's New World Dictionary of Computer Terms*. 4th ed., New York, Prentice Hall, 1992; Parker, Sybil P., ed. *The McGraw-Hill Dictionary of Scientific and TechnicalTerms*. 4th ed. New York, NY, McGraw-Hill, 1989; and Turner, Rufus P., and Gibilisco, Stan. *The Illustrated Dictionary of Electronics*. 5th ed. McGraw-Hill, 1991.
"etchable layer" (Claims 1, 5, 10, 11-13, and 17)	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this term to mean "a portion of the first substrate that is readily etched, relative to the etch stop layer." Intrinsic Evidence Support: '678 at 2:20-22; Id. at 3:12-21; Id. at 4:3-6, 41-44; Figs. 1-4; Claim 10; U.S. Patent No. 4,815,208 (Raschke), 2:30-36; and Amendments and Remarks Filed June 4, 1994. Extrinsic Evidence Support: Declaration of Dr. A. Bruce Buckman.
"etch-stop layer" (Claims 1-5 and 10-17)	A portion of the first substrate that is etched less readily, relative to the etchable layer. Intrinsic Evidence Support: '678 at 2:20-22, 3:12-21,4:1-5, and 4: 41-44; Id. at Abstract;

	Figures 1-4; Claim 10; U.S. Patent No. 5,227,656 (Timlin), 7:58-59; Id. at 8:27-30; Id., Figs. 3-7; U.S. Patent No. 5,182,624 (Tran), 9:27-30; U.S. Patent No. 5,043,582 (Cox), 7:66-68; U.S. Patent No. 5,034,343 (Rouse), 1:41-44; U.S. Patent No. 5,024,723 (Goesele), Abstract; Id. at 3:7-9, 12:-20; U.S. Patent No. 4,839,018 (Wahlstrom), 2:11-15, 67-68; U.S. Patent No. 4,815,208 (Raschke), 3:21-38; U.S. Patent No. 4,169,000 (Riseman), Fig. 1-6; U.S. Patent No. 4,612,083 (Yasumoto), 5:43-45; U.S. Patent No. 4,131,909 (Matsuda), 4:51-53, Figs. 3I, 3J; U.S. Patent No. 3,623,219 (Stoller), 2:9-11; Id. at 3:61-62; U.S. Patent No. 3,332,137 (Kenney), 4:75-5:7; and Amendments and Remarks Filed June 4, 1994. <u>Extrinsic Evidence Support:</u> Declaration of Dr. A. Bruce Buckman.
"overlying" (Claims 1, 11, and 13)	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this term to mean "lying on." <u>Intrinsic Evidence Support:</u> '678 at 3:67-4:2; Id. at 4:27-31; Id. at Abstract; Figs. 1-4; U.S. Patent No. 5,227,656 (Timlin), 8:31-38, Fig. 7; U.S. Patent No. 5,182,624 (Tran), 9:27-30; U.S. Patent No. 5,043,582 (Cox), 7:66-68; U.S. Patent No. 5,034,343 (Rouse), *passim*; U.S. Patent No. 5,024,723 (Goesele), *passim*;

	U.S. Patent No. 4,815,208 (Raschke), 2:30-36. U.S. Patent No. 4,829,018 (Wahlstrom), 2:11-17; U.S. Patent No. 478,594 (Schulte), 2:57-59; U.S. Patent No. 4,670,653 (McConkle), 4:30-31; U.S. Patent No. 4,612,083 (Yasumoto), 5:43-45. U.S. Patent No. 4,169,000 (Riseman), 6:48-68 U.S. Patent No. 4,131,909 (Hayashi), 1:28-30; U.S. Patent No., 3,623,219 (Stoller), *passim*; U.S. Patent No. 3,332,137 (Kenney), *passim*; and Amendments and Remarks Filed June 4, 1994. <u>Extrinsic Evidence Support:</u> Declaration of Dr. A. Bruce Buckman.
"wafer" (Claims 1, 3-5, 7-8, 11-13, and 15-17)	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this term to mean "a portion of the first substrate in or on which the microelectronic circuit element is formed." <u>Intrinsic Evidence Support:</u> '678 at 1:45-48, 2:8-9, 15-24, 29-40, and 47-50; Id. at 4:1-2, 10-1127-30, and 37-40; Id. at 5:3-6; Id. at 6:28-42, 59-7:8; Id. at Abstract; Figs. 1-4; '678 claims 1, 3-5, 7-8, 11-13, and 15-17; U.S. Patent No. 5,227,656 (Timlin), 4:67; Id. at 9:60, Id. at 10:11; U.S. Patent No. 5,182,624 (Tran), 13:21; Id. at 16:57; U.S. Patent No. 5,043,582 (Cox), *passim*; U.S. Patent No. 5,034,343 (Rouse), *passim*; U.S. Patent No. 5,024,723 (Gosele), 2:27-30; U.S. Patent No. 4,829,018 (Wahlstrom), 2:12, 18:19; U.S. Patent No. 4,612,083 (Yasumoto), *passim*;

	U.S. Patent No. 4,467,340 (Rode), 2:27; U.S. Patent No. 4,169,000 (Riseman), *passim*; U.S. Patent No. 4,131,909 (Matsuda), 3:55-56, 59-62 Fig. 3A; U.S. Patent No. 3,623,219 (Stoller), *passim*; U.S. Patent No. 3,332,137 (Kenney), *passim*; and Amendments and Remarks Filed June 4, 1994. Extrinsic Evidence Support: Declaration of Dr. A. Bruce Buckman; First Petition for *Inter Partes* Review for U.S. Patent No. 5,591,678, IPR2015-01201; Second Petition for *Inter Partes* Review for U.S. Patent No. 5,591,678, IPR2016-00209; Spencer, Donald D. *Webster's New World Dictionary of Computer Terms*. 4th ed., New York, Prentice Hall, 1992; Parker, Sybil P., ed. *The McGraw-Hill Dictionary of Scientific and Technical Terms*. 4th ed. New York, NY, McGraw-Hill, 1989; and Turner, Rufus P., and Gibilisco, Stan. *The Illustrated Dictionary of Electronics*. 5th ed. McGraw-Hill, 1991.
"microelectronic circuit element" (Claims 1, 6-7, 11, 13, and 15)	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this term to mean "a patterned element in an electrical circuit." Intrinsic Evidence Support: '678 at 1:14-17, 2:9-14, 49-51 and 59-61; Id. at 4:39-56; Id. at 7: 21-22 and 47-51; Figs. 1-4; '678 claims 2-4 and 14-16; and, U.S. Patent No. 5,043,582 (Cox), *passim*; U.S. Patent No. 5,034,343 (Rouse), *passim*; U.S. Patent No. 5,024,724 (Goesele), *passim*; U.S. Patent No. 4,980,308 (Hayashi), 5:27; and

	U.S. Patent No. 4,943,491 (Norton), 1:17; Id. at 3:2; U.S. Patent No. 4,829,018 (Wahlstrom),1:49, 65; U.S. Patent No. 4,815,208 (Raschke), *passim*; U.S. Patent No. 4,783,594 (Schulte), *passim*; U.S. Patent No. 4,670,653 (McConkle), 2:65-66; Id. at 9:64; Id. at 11:14; Id., Fig. 12; U.S. Patent No. 4,467,340 (Rode), *passim*; U.S. Patent No. 4,612,083 (Yasumoto), *passim*; U.S. Patent No. 4,169,000 (Riseman), 1:15-16; U.S. Patent No. 4,131,909 (Matsuda), *passim*; U.S. Patent No. 3,632,219 (Stoller), *passim*; U.S. Patent No. 3,332,137 (Kenney), 3:28-4:48, Figs. 3-7; and Amendments and Remarks Filed June 4, 1994. <u>Extrinsic Evidence Support:</u> Declaration of Dr. A. Bruce Buckman; First Petition for *Inter Partes* Review for U.S. Patent No. 5,591,678, IPR2015-01201; Second Petition for *Inter Partes* Review for U.S. Patent No. 5,591,678, IPR2016-00209; Spencer, Donald D. *Webster's New World Dictionary of Computer Terms*. 4th ed., New York, Prentice Hall, 1992; Turner, Rufus P., and Gibilisco, Stan. *The Illustrated Dictionary of Electronics*. 5th ed. McGraw-Hill, 1991.
"attaching" (Claims 1, 7-9, 11, 13, and 18)	Joining together two surfaces. <u>Intrinsic Evidence Support:</u> '678 at 1:11-13; Id. at 2:21-22, 51-53; Id. at 5:14-18, 29-39, 46-48; Id. at 7:38-41 and45-47; Figs. 1 and 4; '678 claims 7, 8, 9, 11, 13 and 18; U.S. Patent No. 4,169,000 (Riseman), *passim*; Amendments and Remarks Filed June 4, 1994.

	Extrinsic Evidence Support: Declaration of Dr. A. Bruce Buckman.
"second substrate" (Claims 1, 6-9, 11, 13, and 18)	A second solid support material that is part of the complete device. Intrinsic Evidence Support: '678 at 1:11-12; Id. at 2:21-23, 59-61; Id. at 3:6-8; Id. at 5: 14-21, 25-28, 33-37 and 47-51; Figs. 1-4; U.S. Patent No. 5,227,656 (Timlin), *passim*; U.S. Patent No. 4,815,208 (Raschke), *passim*; U.S. Patent No. 4,612,083 (Yasumoto), *passim*; U.S. Patent No. 4,467,340 (Rode), 3:55; U.S. Patent No. 4,169,000 (Riseman), *passim*; U.S. Patent No. 4,131,909 (Matsuda), *passim*; and Amendments and Remarks Filed June 4, 1994 Extrinsic Evidence Support: Declaration of Dr. A. Bruce Buckman; Spencer, Donald D. *Webster's New World Dictionary of Computer Terms*. 4th ed., New York, Prentice Hall, 1992; Parker, Sybil P., ed. *The McGraw-Hill Dictionary of Scientific and Technical Terms*. 4th ed. New York, NY, McGraw-Hill, 1989; and Turner, Rufus P., and Gibilisco, Stan. *The Illustrated Dictionary of Electronics*. 5th ed. McGraw-Hill, 1991.
"etching" (Claims 1, 2, 9, 10, 11, 13, 14, and 18)	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this term to mean "removing material with an etchant." Intrinsic Evidence Support: '678 at 3:15-21; Id. at 6: 22-27; and U.S. Patent No. 5,227,656 (Timlin), 8:31-38, Fig. 7;

	U.S. Patent No. 5,182,624 (Tran), 9:27-30; U.S. Patent No. 5,043,582 (Cox), 7:66-68; U.S. Patent No. 5,034,343 (Rouse), *passim*; U.S. Patent No. 5,024,723 (Goesele), *passim*; U.S. Patent No. 4,815,208 (Raschke), 2:30-36. U.S. Patent No. 4,829,018 (Wahlstrom), 2:11-17; U.S. Patent No. 478,594 (Schulte), 2:57-59; U.S. Patent No. 4,670,653 (McConkle), 4:30-31; U.S. Patent No. 4,612,083 (Yasumoto), 5:43-45. U.S. Patent No. 4,169,000 (Riseman), 6:48-68 U.S. Patent No. 4,131,909 (Hayashi), 1:28-30; U.S. Patent No., 3,623,219 (Stoller), *passim*; U.S. Patent No. 3,332,137 (Kenney), *passim*; and Amendments and Remarks Filed June 4, 1994. <u>Extrinsic Evidence Support:</u> Declaration of Dr. A. Bruce Buckman; First Petition for *Inter Partes* Review for U.S. Patent No. 5,591,678, IPR2015-01201; Second Petition for *Inter Partes* Review for U.S. Patent No. 5,591,678, IPR2016-00209; Parker, Sybil P., ed. *The McGraw-Hill Dictionary of Scientific and Technical Terms*. 4th ed. New York, NY, McGraw-Hill, 1989; and Turner, Rufus P., and Gibilisco, Stan. *The Illustrated Dictionary of Electronics*. 5th ed. McGraw-Hill, 1991.
"etching away the etchable layer… down to the etch stop layer" (Claims 1, 11, and 13)	Etching the etchable layer to at least the etch-stop layer. <u>Intrinsic Evidence Support:</u> '678 at 3:15-21; Id. at 6: 22-27; and U.S. Patent No. 5,227,656 (Timlin), 8:31-38, Fig. 7;

	U.S. Patent No. 5,182,624 (Tran), 9:27-30; U.S. Patent No. 5,043,582 (Cox), 7:66-68; U.S. Patent No. 5,034,343 (Rouse), *passim*; U.S. Patent No. 5,024,723 (Goesele), *passim*; U.S. Patent No. 4,815,208 (Raschke), 2:30-36. U.S. Patent No. 4,829,018 (Wahlstrom), 2:11-17; U.S. Patent No. 478,594 (Schulte), 2:57-59; U.S. Patent No. 4,670,653 (McConkle), 4:30-31; U.S. Patent No. 4,612,083 (Yasumoto), 5:43-45. U.S. Patent No. 4,169,000 (Riseman), 6:48-68 U.S. Patent No. 4,131,909 (Hayashi), 1:28-30; U.S. Patent No., 3,623,219 (Stoller), *passim*; U.S. Patent No. 3,332,137 (Kenney), *passim*; and Amendments and Remarks Filed June 4, 1994. <u>Extrinsic Evidence Support:</u> Declaration of Dr. A. Bruce Buckman; First Petition for *Inter Partes* Review for U.S. Patent No. 5,591,678, IPR2015-01201; Second Petition for *Inter Partes* Review for U.S. Patent No. 5,591,678, IPR2016-00209; Parker, Sybil P., ed. *The McGraw-Hill Dictionary of Scientific and Technical Terms*. 4th ed. New York, NY, McGraw-Hill, 1989; and Turner, Rufus P., and Gibilisco, Stan. *The Illustrated Dictionary of Electronics*. 5th ed. McGraw-Hill, 1991.
"the step of attaching includes the step of making an electrical contact…" (Claim 7)	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this term to mean "making a contact in which current can flow in either direction with minimal resistance." <u>Intrinsic Evidence Support:</u> '678 at 2:21-22, 51-53; Id. at 3:8-12; Id. at 5:14-18, 29-39, 46-

	48; Id. at 7:38-41 and45-47; Figs. 1 and 4; '678 claims 7, 8, 9, 11, 13 and 18; U.S. Patent No. 4,169,000 (Riseman), *passim*; and Amendments and Remarks Filed June 4, 1994. Extrinsic Evidence Support: Declaration of Dr. A. Bruce Buckman.
The order of the recited method steps (All claims)	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this term to mean each step is started before the step of etching away. Intrinsic Evidence Support: '678 at 1:1-5 and 10-13; 65-2:14; Id. at 2:55-3:14; Id. at 7: 18-19 and 32-34; Id. at Abstract; and Figs 1-4. Extrinsic Evidence Support: Declaration of Dr. A. Bruce Buckman.

Exhibit B

	TERM | ASSERTED CLAIMS	DEFENDANTS' PROPOSED CONSTRUCTIONS	DEFENDANTS' SUPPORT
1.	"first substrate" (Claims 1, 6-9, 11, 13, and 17-18)	A structure that initially has at least three distinct material layers.	**Specification Support** Abstract, FIG. 1, Col. 1:44-2:2, 2:5-28, 2:43-3:21, 3:64-4:37, 4:38-5:13, 6:50-7:37. **Prosecution History Support** Amendment, appl'n s.n. 08/006,120, pp. 5-8 (June 1994) **Extrinsic Evidence** Ruzyllo, Semiconductor Glossary, 14, 16, 145, 172 (2004). substrate: in a microcircuit, the supporting material upon which or within which an integrated circuit is fabricated, or to which an integrated circuit is attached. Business Dictionary of Computers, p. 354 (1993). substrate: the support material on which an integrated circuit is constructed or to which it is attached. Academic Press Dictionary of Science and Technology, p. 2125 (1992). Declaration of Jerzy Ruzyllo
2.	"etchable layer" (Claims 1, 5, 10, 11-13, and 17)	A support layer of the first substrate, distinct from the etch-stop layer and the wafer, having an etch rate much higher than that for the etch-stop layer.	**Specification Support** Abstract, FIGS. 1-2, Col. 1:44-2:2, 2:5-28, 2:43-3:21, 3:64-4:37, 5:44-6:9, 6:50-7:37. **Prosecution History Support** Amendment, appl'n s.n. 08/006,120, pp. 5-8 (June 1994) **Extrinsic Evidence**

TERM | ASSERTED CLAIMS	DEFENDANTS' PROPOSED CONSTRUCTIONS	DEFENDANTS' SUPPORT
		Ruzyllo, Semiconductor Glossary, 50, 135 (2004). Declaration of Jerzy Ruzyllo
3. "etch-stop layer" (Claims 1-5 and 10-17)	***Sony/OmniVision/Apple*:** A layer of the first substrate, distinct from the etchable layer and the wafer, which stops the etching process by virtue of it having a lower etch rate than the etchable layer. ***Samsung*:** A layer of the first substrate distinct from the etchable layer and the wafer, grown upon the etchable layer used for stopping the etching process.	**Specification Support** Abstract, FIGS. 1-3, Col. 2:5-28, 2:43-58, 3:6-21, 3:64-4:37, 5:44-6:9, 6:19-43, 6:50-7:37. **Prosecution History Support** Amendment, appl'n s.n. 08/006,120, pp. 5-8 (June 1994) **Extrinsic Evidence** Ruzyllo, Semiconductor Glossary, 50, 135 (2004). U.S. Patent No. 4,426,768, col. 1:43-65. U.S. Patent No. 4,601,779, col. 3:59-4:20. U.S. Patent No. 4,875,086, col. 3:46-59, col. 4:45-59. U.S. Patent No. 4,889,832, col. 2:5-8, col. 3:2-9, 5:24-28. U.S. Patent No. 4,959,328, col. 1:52-56, col. 2:31-34. U.S. Patent No. 5,013,681, col. 3:45-59, col. 5:51-6:9. U.S. Patent No. 5,024,723, col. 3:7-55. U.S. Patent No. 5,102,821, col. 3:47-51. U.S. Patent No. 5,202,754, col. 4:4-10, col. 5:17-22. U.S. Patent No. 5,227,313, col. 3:60-4:6, col.

	TERM | ASSERTED CLAIMS	DEFENDANTS' PROPOSED CONSTRUCTIONS	DEFENDANTS' SUPPORT
			4:36-5:4. D. Godbey, et al., Advanced Silicon on Insulator Technology (Naval Research Laboratory 1991), pp. 226-27. S Mahajan & LC Kimerling, Concise Encyclopedia of Semiconducting Materials & Related Technologies (Pergamon Press, 1992), p. 466. Andrew L. Robinson, Silicon-on-Insulator Photonics, Rome Laboratory (1992), p. s-1. R. Peter Smith, et al., A New Fabrication Technique for Back-to-Back Varactor Diodes, Third International Symposium on Space Terahertz Technology (1992), p. 159-161. Declaration of Jerzy Ruzyllo
4.	"overlying" (Claims 1, 11, and 13)	Lying over or upon.	**Specification Support** Abstract, FIGS. 1-4, Col. 2:5-28, 2:43-58, 3:64-4:37, 6:50-7:37. **Extrinsic Evidence** overlie: to lie over; lie or rest upon. Webster's Third New Int'l Dictionary, p. 1608 (1993). overlie: to lie over or on. The American Heritage College Dictionary, p. 974 (3d ed. 1997). Declaration of Jerzy Ruzyllo
5.	"wafer" (Claims 1, 3-5, 7-8, 11-	***Sony/OmniVision/Apple*:** A layer of the first substrate, distinct from the etch-stop layer and the etchable layer, and within which some	**Specification Support** Abstract, FIG. 1, Col. 1:44-2:2, 2:5-28, 2:43-58,

	TERM | ASSERTED CLAIMS	DEFENDANTS' PROPOSED CONSTRUCTIONS	DEFENDANTS' SUPPORT
	13, and 15-17)	portion of microelectronic circuit elements are formed. ***Samsung*:** A layer of the first substrate distinct from the etch-stop layer and the etchable layer, deposited on or bonded to the etch-stop layer.	3:6-21, 3:64-5:13, 6:28-43, 6:50-7:37. **Prosecution History Support** Amendment, appl'n s.n. 08/006,120, pp. 5-8 (June 1994) **Extrinsic Evidence** Ruzyllo, Semiconductor Glossary, 2, 14, 172 (2004). wafer: a thin slice from a silicon ingot that is the basis of the chip. Business Dictionary of Computers, p. 396 (1993). wafer: a flat semiconductor slice on which microcircuits or individual microcircuit devices can be fabricated. Academic Press Dictionary of Science and Technology (1992). wafer: a large single crystal of semiconductor, usually silicon, that is used as the substrate on which *integrated circuits are manufactured. Dictionary of Computing, p. 534 (4th ed. 1996). wafer: a thin disk of a purified crystalline semiconductor, typically silicon, that is cut into chips after processing. Typically, a wafer is about one fiftieth of an inch thick and four to five inches in diameter. Newton's Telecom Dictionary, p. 1135 (8th ed. 1994). Declaration of Jerzy Ruzyllo
6.	"microelectronic circuit element"	A component of an active circuit element or passive circuit structure.	**Specification Support** Abstract, FIGS. 1-4, Col. 1:44-2:2, 2:5-28, 2:37-

	TERM | ASSERTED CLAIMS	DEFENDANTS' PROPOSED CONSTRUCTIONS	DEFENDANTS' SUPPORT
	(Claims 1, 6-7, 11, 13, and 15)		3:21, 3:37-40, 4:38-5:43, 6:28-43, 6:50-7:37. **Extrinsic Evidence** microelectronics: the special methods and techniques used in producing miniature circuits. Academic Press Dictionary of Science and Technology, p. 1373 (1992). circuit: an interconnection of electrical elements forming one or more complete paths for the flow of current. Academic Press Dictionary of Science and Technology, p. 433 (1992). element: any circuit or device that performs a basic data-processing function. Academic Press Dictionary of Science and Technology, p. 733 (1992). Declaration of Jerzy Ruzyllo
7.	"attaching" (Claims 1, 7-9, 11, 13, and 18)	Fastening or joining.	**Specification Support** Abstract, FIGS. 1-4, Col. 2:5-28, 2:37-3:21, 5:14-43, 6:50-7:37. **Extrinsic Evidence** attach: to fasten or affix; join; connect. Webster's Encyclopedic Unabridged Dictionary, 133 (1996). attach: to fasten, secure, or join. The American Heritage College Dictionary, 88 (3d ed. 1997). Declaration of Jerzy Ruzyllo
8.	"second substrate" (Claims 1, 6-9, 11, 13,	A structure separate and distinct from the first substrate (as construed) that provides support to	**Specification Support** Abstract, FIGS. 1-4, Col. 2:5-28, 2:43-3:21, 5:14-

	TERM | ASSERTED CLAIMS	DEFENDANTS' PROPOSED CONSTRUCTIONS	DEFENDANTS' SUPPORT
	and 18)	the first substrate through the etching process.	43, 6:50-7:37.
9.	"etching" (Claims 1, 2, 9, 10, 11, 13, 14, and 18)	A subtractive process in the course of which a solid is dissolved in liquid chemicals (wet etching) or converted into gaseous compound (dry etching).	**Specification Support** Abstract, FIGS. 1-3, Col. 2:5-28, 2:43-3:21, 5:44-6:9, 6:50-7:37. **Extrinsic Evidence** Ruzyllo, Semiconductor Glossary, 50, 135 (2004). U.S. Patent No. 4,426,768, col. 1:43-65. U.S. Patent No. 4,601,779, col. 4:65-5:58. U.S. Patent No. 4,875,086, col. 3:46-59, col. 4:45-59. U.S. Patent No. 4,889,832, col. 6:47-61. U.S. Patent No. 4,959,328, col. 1:52-56, col. 2:31-34. U.S. Patent No. 5,013,681, col. 4:32-65. U.S. Patent No. 5,024,723, col. 3:7-55. U.S. Patent No. 5,102,821, col. 3:47-51. U.S. Patent No. 5,202,754, col. 4:4-10, col. 5:17-22. U.S. Patent No. 5,227,313, col. 4:36-5:4. D. Godbey, et al., Advanced Silicon on Insulator Technology (Naval Research Laboratory 1991), pp. 226-27. S Mahajan & LC Kimerling, Concise Encyclopedia of Semiconducting Materials & Related Technologies (Pergamon Press, 1992), p.

TERM | ASSERTED CLAIMS	DEFENDANTS' PROPOSED CONSTRUCTIONS	DEFENDANTS' SUPPORT
		466. Andrew L. Robinson, Silicon-on-Insulator Photonics, Rome Laboratory (1992), p. s-2. R. Peter Smith, et al., A New Fabrication Technique for Back-to-Back Varactor Diodes, Third International Symposium on Space Terahertz Technology (1992), p. 159-161. Declaration of Jerzy Ruzyllo
10. "etching away the etchable layer … down to the etch stop layer" (Claims 1, 11, and 13)	An etching process that removes the etchable layer and then is stopped by the etch-stop layer.	**Specification Support** Abstract, FIGS. 1-3, Col. 2:5-28, 2:43-3:21, 5:44-6:9, 6:50-7:37. **Prosecution History Support** Amendment, appl'n s.n. 08/006,120, pp. 5-8 (June 1994) **Extrinsic Evidence** Ruzyllo, Semiconductor Glossary, 50, 135 (2004). Declaration of Jerzy Ruzyllo
11. "the step of attaching includes the step of making an electrical contact…" (Claim 7)	Electrical contact between the first and second microelectronic circuit elements must be made as part of the step of attaching the first and second substrates together.	**Specification Support** FIGS. 1-4, Col. 1:44-2:2, 2:5-28, 2:37-3:21, 5:14-43, 6:50-7:37. **Extrinsic Evidence** step: one instruction or operation in a routine. Academic Press Dictionary of Science and Technology, p. 2092 (1992). contact: a point of instance of touching or interaction; the conducting part of a component,

TERM | ASSERTED CLAIMS	DEFENDANTS' PROPOSED CONSTRUCTIONS	DEFENDANTS' SUPPORT
		such as a switch or relay, that interacts with another conducting part to make or break a circuit. Academic Press Dictionary of Science and Technology, p. 505 (1992). Declaration of Jerzy Ruzyllo
12. The order of the recited method steps (All asserted claims)	The steps of independent claims 1 and 13 must be performed in the order in which they are recited.	**Specification Support** Abstract, FIGS. 1-4, Col. 1:44-2:2, 2:5-28, 2:43-3:21, 3:64-6:9, 6:50-7:37. **Extrinsic Evidence** Declaration of Jerzy Ruzyllo **Prosecution History Support** Amendment, appl'n s.n. 08/006,120, pp. 5-8 (June 1994).

EXHIBIT A

P.R.4-5(D) Joint Claim Construction Chart

Claim Language	Claim Terms	Raytheon's Proposal	Defendants' Proposal	Court's Construction
CLAIM 1 A method of fabricating a microelectronic device, comprising the steps of: furnishing a **first substrate** having an **etchable layer**, an **etch-stop layer overlying** the **etchable layer**, and a **wafer** overlying the **etch-stop layer**; forming a **microelectronic circuit element** in the exposed side of the **wafer** of the **first substrate** opposite to the side **overlying** the **etch-stop layer**;	**First Substrate**	A first solid support material.	A structure that initially has at least three distinct material layers.	
	Etchable Layer	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this term to mean, "a portion of the first substrate that is readily etched, relative to the etch stop layer."	A support layer of the first substrate, distinct from the etch-stop layer and the wafer, having an etch rate much higher than that for the etch-stop layer.	
	Etch-stop Layer	A portion of the first substrate that is etched less readily, relative to the etchable layer.	A layer of the first substrate, distinct from the etchable layer and the wafer, which stops the etching process by virtue of it having a lower etch rate than the etchable layer.	

[1] Raytheon contends that the Court should construe terms for Claims 1-18 of the '678 Patent. The Sony Defendants and Apple contend that the Court should only construe terms for Claims 1, 5-10, 13, and 18. OmniVision contends that the Court should only construe terms for Claims 1 and 9-10. The Samsung Defendants contend that the Court should only construe terms for Claims 1 and 8-10.

Claim Language	Claim Terms	Raytheon's Proposal	Defendants' Proposal	Court's Construction
attaching the **wafer** of the **first substrate** to a **second substrate**; and **etching** away the **etchable layer** of the **first substrate down to the etch-stop layer.**	**Overlying**	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this term to mean, "lying on."	Lying over or upon.	
	Wafer	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this term to mean, "a portion of the first substrate in or on which the microelectronic circuit element is formed."	***Sony Defendants/OmniVision/ Apple*:** A layer of the first substrate, distinct from the etch-stop layer and the etchable layer, and within which some portion of microelectronic circuit elements are formed. ***Samsung*:** A layer of the first substrate distinct from the etch-stop layer and the etchable layer, deposited on or bonded to the etch-stop layer.	
	Microelectronic Circuit Element	No construction necessary. Plain and ordinary meaning. If the Court believes this	A component of an active circuit element or passive circuit structure.	

[1] Raytheon contends that the Court should construe terms for Claims 1-18 of the '678 Patent. The Sony Defendants and Apple contend that the Court should only construe terms for Claims 1, 5-10, 13, and 18. OmniVision contends that the Court should only construe terms for Claims 1 and 9-10. The Samsung Defendants contend that the Court should only construe terms for Claims 1 and 8-10.

Claim Language	Claim Terms	Raytheon's Proposal	Defendants' Proposal	Court's Construction
		term requires construction, the Court should construe this term to mean, "a patterned element in an electrical circuit."		
	Attaching	Joining together two surfaces.	Fastening or joining.	
	Second Substrate	A second solid support material that is part of the complete device.	A structure separate and distinct from the first substrate (as construed) that provides support to the first substrate through the etching process.	
	Etching	AGREED	AGREED	Removing material with an etchant
	"etching away the etchable layer… down to the etch stop layer"	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe this phrase should mean "making a contact in which current can flow in either direction with	Electrical contact between the first and second microelectronic circuit elements must be made as part of the step of attaching the first and second substrates together.	

[1] Raytheon contends that the Court should construe terms for Claims 1-18 of the '678 Patent. The Sony Defendants and Apple contend that the Court should only construe terms for Claims 1, 5-10, 13, and 18. OmniVision contends that the Court should only construe terms for Claims 1 and 9-10. The Samsung Defendants contend that the Court should only construe terms for Claims 1 and 8-10.

Claim Language	Claim Terms	Raytheon's Proposal	Defendants' Proposal	Court's Construction
		minimal resistance."		
	The order of the recited method steps	No construction necessary. Plain and ordinary meaning. If the Court believes this term requires construction, the Court should construe that each step is started before the step of etching.	The steps of independent claims 1 and 13 must be performed in the order in which they are recited.	
CLAIM 2[1] The method of claim 1, further including an additional step, after the step of **etching**, of patterning the **etch-stop layer**.	The highlighted Claim Terms are addressed in Claim 1. This claim has not been asserted against Defendants subject to Raytheon's pending Motion for Leave to Amend P.R. 3-1 Infringement Contentions, which Defendants oppose. Defendants have not undertaken a review of these claims to determine whether they recite other terms, for example, "patterning," that require construction, and therefore object to the inclusion of this claim in the Joint Claim Construction Chart.			

[1] Raytheon contends that the Court should construe terms for Claims 1-18 of the '678 Patent. The Sony Defendants and Apple contend that the Court should only construe terms for Claims 1, 5-10, 13, and 18. OmniVision contends that the Court should only construe terms for Claims 1 and 9-10. The Samsung Defendants contend that the Court should only construe terms for Claims 1 and 8-10.

Claim Language	Claim Terms	Raytheon's Proposal	Defendants' Proposal	Court's Construction
CLAIM 3[1] The method of claim 2, further including an additional step, after the step of patterning, of forming an electrical connection to the **microelectronic circuit element** through the patterned **etch-stop layer** and through the **wafer**.	The highlighted Claim Terms are addressed in Claim 1. This claim has not been asserted against Defendants subject to Raytheon's pending Motion for Leave to Amend P.R. 3-1 Infringement Contentions, which Defendants oppose. Defendants have not undertaken a review of these claims to determine whether they recite other terms, for example, "patterning," that require construction, and therefore object to the inclusion of this claim in the Joint Claim Construction Chart.			
CLAIM 4[1] The method of claim 2, further including an additional step, after the step of patterning, of forming an electrical connection to the **wafer** through the patterned **etch-stop layer**.	The highlighted Claim Terms are addressed in Claim 1. This claim has not been asserted against Defendants subject to Raytheon's pending Motion for Leave to Amend P.R. 3-1 Infringement Contentions, which Defendants oppose. Defendants have not undertaken a review of these claims to determine whether they recite other terms, for example, "patterning," that require construction, and therefore object to the inclusion of this claim in the Joint Claim Construction Chart.			

[1] Raytheon contends that the Court should construe terms for Claims 1-18 of the '678 Patent. The Sony Defendants and Apple contend that the Court should only construe terms for Claims 1, 5-10, 13, and 18. OmniVision contends that the Court should only construe terms for Claims 1 and 9-10. The Samsung Defendants contend that the Court should only construe terms for Claims 1 and 8-10.

Claim Language	Claim Terms	Raytheon's Proposal	Defendants' Proposal	Court's Construction
CLAIM 5[1] The method of claim 1, wherein the **etchable layer** is silicon, the **etch-stop layer** is silicon dioxide, and the **wafer** is single-crystal silicon.	The highlighted Claim Terms are addressed in Claim 1			
CLAIM 6[1] The method of claim 1, wherein the **second substrate** contains a second **microelectronic circuit element**.	The highlighted Claim Terms are addressed in Claim 1			
CLAIM 7[1] The method of claim 6, wherein the step of **attaching** includes the step of making an electrical contact from the **microelectronic circuit element** on the wafer of the **first substrate** to the second **microelectronic circuit element** on the **second substrate**.	The highlighted Claim Terms are addressed in Claim 1			

[1] Raytheon contends that the Court should construe terms for Claims 1-18 of the '678 Patent. The Sony Defendants and Apple contend that the Court should only construe terms for Claims 1, 5-10, 13, and 18. OmniVision contends that the Court should only construe terms for Claims 1 and 9-10. The Samsung Defendants contend that the Court should only construe terms for Claims 1 and 8-10.

Claim Language	Claim Terms	Raytheon's Proposal	Defendants' Proposal	Court's Construction
CLAIM 8[1] The method of claim 1, wherein the step of **attaching** includes the steps of placing a layer of epoxy between the **second substrate** and the **wafer** portion of the **first substrate**, and **degassing and curing the epoxy.**	The disputed terms "attaching," "second substrate," "wafer," and "first substrate" are addressed in Claim 1			
	Degassing and Curing the Epoxy	AGREED	AGREED	to remove gas and solidify the epoxy
CLAIM 9 The method of claim 1, further including an additional step, after the step of **attaching** and before the step of **etching**, of fixing the **second substrate** to an etching support that is resistant to attack by an etchant.	The highlighted Claim Terms are addressed in Claim 1			
CLAIM 10 The method of claim 1, wherein the step of **etching** includes the step of contacting the	The highlighted Claim Terms are addressed in Claim 1			

[1] Raytheon contends that the Court should construe terms for Claims 1-18 of the '678 Patent. The Sony Defendants and Apple contend that the Court should only construe terms for Claims 1, 5-10, 13, and 18. OmniVision contends that the Court should only construe terms for Claims 1 and 9-10. The Samsung Defendants contend that the Court should only construe terms for Claims 1 and 8-10.

Claim Language	Claim Terms	Raytheon's Proposal	Defendants' Proposal	Court's Construction
etchable layer to a liquid etchant that attacks the etchable layer rapidly and the etch-stop layer slowly.				
CLAIM 11[1] A method of fabricating a microelectronic device, comprising the steps of: furnishing a **first substrate** having an **etchable layer**, an **etch-stop layer overlying** the **etchable layer**, and a **wafer overlying** the **etch-stop layer**; forming a **microelectronic circuit element** in the exposed side of the **wafer** of the **first substrate** opposite the side **overlying** the **etch-stop layer**; **attaching** the **wafer** of the **first substrate** to a **second substrate**, the	The highlighted Claim Terms are addressed in Claim 1. This claim has not been asserted against Defendants subject to Raytheon's pending Motion for Leave to Amend P.R. 3-1 Infringement Contentions, which Defendants oppose. Defendants have not undertaken a review of these claims to determine whether they recite other terms that require construction, and therefore object to the inclusion of this claim in the Joint Claim Construction Chart.			

[1] Raytheon contends that the Court should construe terms for Claims 1-18 of the '678 Patent. The Sony Defendants and Apple contend that the Court should only construe terms for Claims 1, 5-10, 13, and 18. OmniVision contends that the Court should only construe terms for Claims 1 and 9-10. The Samsung Defendants contend that the Court should only construe terms for Claims 1 and 8-10.

Claim Language	Claim Terms	Raytheon's Proposal	Defendants' Proposal	Court's Construction
second substrate having a second **microelectronic circuit element therein**; making an electrical contact from the **microelectronic circuit element** in the **wafer** of the **first substrate** to the second **microelectronic circuit element** on the **second substrate**; and **etching** away the **etchable layer** of the **first substrate down to the etch-stop layer**; and forming an electrical connection to the **microelectronic circuit element** in the **wafer** of the **first substrate** through the **etch-stop layer**.				

[1] Raytheon contends that the Court should construe terms for Claims 1-18 of the '678 Patent. The Sony Defendants and Apple contend that the Court should only construe terms for Claims 1, 5-10, 13, and 18. OmniVision contends that the Court should only construe terms for Claims 1 and 9-10. The Samsung Defendants contend that the Court should only construe terms for Claims 1 and 8-10.

Claim Language	Claim Terms	Raytheon's Proposal	Defendants' Proposal	Court's Construction
CLAIM 12[1] The method of claim 11, wherein the **etchable layer** is silicon, the **etch-stop layer** is silicon dioxide, and the **wafer** is single-crystal silicon.	The highlighted Claim Terms are addressed in Claim 1. This claim has not been asserted against Defendants. Defendants have not undertaken a review of these claims to determine whether they recite terms that require construction, and therefore object to the inclusion of this claim in the Joint Claim Construction Chart.			
CLAIM 13[1] A method of fabricating a microelectronic device, comprising the steps of: furnishing a **first substrate** having a silicon **etchable layer**, a silicon dioxide **etch-stop layer overlying** the silicon layer, and a single-crystal silicon **wafer** overlying the **etch-stop layer**, the **wafer** having a front surface not contacting the silicon dioxide layer; forming a	The highlighted Claim Terms are addressed in Claim 1			

[1] Raytheon contends that the Court should construe terms for Claims 1-18 of the '678 Patent. The Sony Defendants and Apple contend that the Court should only construe terms for Claims 1, 5-10, 13, and 18. OmniVision contends that the Court should only construe terms for Claims 1 and 9-10. The Samsung Defendants contend that the Court should only construe terms for Claims 1 and 8-10.

Claim Language	Claim Terms	Raytheon's Proposal	Defendants' Proposal	Court's Construction
microelectronic circuit element in the front surface of the single-crystal silicon **wafer**; **attaching** the front surface of the single-crystal silicon **wafer** to a first side of a **second substrate**; and **etching** away the silicon **etchable layer down to the silicon dioxide etch-stop layer** using an etchant that attacks the silicon layer but not the silicon dioxide layer.				
CLAIM 14[1] The method of claim 13, further including an additional step, after the step of **etching**, of patterning the **etch-stop layer**.	The highlighted Claim Terms are addressed in Claim 1. This claim has not been asserted against Defendants. Defendants have not undertaken a review of these claims to determine whether they recite terms that require construction, and therefore object to the inclusion of this claim in the Joint Claim Construction Chart.			

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Claim Language	Claim Terms	Raytheon's Proposal	Defendants' Proposal	Court's Construction
CLAIM 15[1] The method of claim 14, further including an additional step, after the step of patterning, of forming an electrical connection to the **microelectronic circuit element** through the patterned **etch-stop layer** and through the **wafer**.	The highlighted Claim Terms are addressed in Claim 1. This claim has not been asserted against Defendants. Defendants have not undertaken a review of these claims to determine whether they recite terms that require construction, and therefore object to the inclusion of this claim in the Joint Claim Construction Chart.			
CLAIM 16[1] The method of claim 14, further including an additional step, after the step of patterning, of forming an electrical connection to the **wafer** through the patterned **etch-stop layer**.	The highlighted Claim Terms are addressed in Claim 1. This claim has not been asserted against Defendants. Defendants have not undertaken a review of these claims to determine whether they recite terms that require construction, and therefore object to the inclusion of this claim in the Joint Claim Construction Chart.			

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Claim Language	Claim Terms	Raytheon's Proposal	Defendants' Proposal	Court's Construction
CLAIM 17[1] The method of claim 13, wherein the silicon **etchable layer** of the **first substrate** is about 500 micrometers in thickness, the silicon dioxide **etch-stop layer** of the first substrate is about 1 micrometer in thickness, and the **wafer** of the first substrate is from about 30 nanometers to about micrometers in thickness.	The highlighted Claim Terms are addressed in Claim 1. This claim has not been asserted against Defendants. Defendants have not undertaken a review of these claims to determine whether they recite terms that require construction, and therefore object to the inclusion of this claim in the Joint Claim Construction Chart.			

[1] Raytheon contends that the Court should construe terms for Claims 1-18 of the '678 Patent. The Sony Defendants and Apple contend that the Court should only construe terms for Claims 1, 5-10, 13, and 18. OmniVision contends that the Court should only construe terms for Claims 1 and 9-10. The Samsung Defendants contend that the Court should only construe terms for Claims 1 and 8-10.

Claim Language	Claim Terms	Raytheon's Proposal	Defendants' Proposal	Court's Construction
CLAIM 18[1] The method of claim 13, wherein the step of **attaching** includes the steps of placing a layer of epoxy between the **second substrate** and the front surface of the single-crystal silicon **wafer**, and **degassing and curing the epoxy.**	The highlighted Claim Terms are addressed in Claims 1 and 8			

[1] Raytheon contends that the Court should construe terms for Claims 1-18 of the '678 Patent. The Sony Defendants and Apple contend that the Court should only construe terms for Claims 1, 5-10, 13, and 18. OmniVision contends that the Court should only construe terms for Claims 1 and 9-10. The Samsung Defendants contend that the Court should only construe terms for Claims 1 and 8-10.