# Chemical Mechanical Polish: The Enabling Technology

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**Abstract:** Chemical mechanical polishing (CMP) has traditionally been considered an enabling technology. CMP was first used in the early 1990s for BEOL metallization to re-planarize the wafer substrate thus enabling advanced lithography which was becoming ever more sensitive to wafer surface topography. Subsequent uses of CMP included density scaling via shallow trench isolation and interconnect formation via copper CMP. As silicon devices scale to 45nm and beyond however, a large number of new uses of CMP are considered attractive options to enable new transistor technologies. These new uses will demand improved CMP performance (uniformity, topography, low defects) at lower cost which will in turn require breakthroughs in hardware, software, metrology and materials (slurry, pad, cleaning chemicals).

This paper reviews the module level and integration challenges of applying traditional CMP steps to enable Hi-K metal gate for 45nm technology and to advance Cu metallization from 65nm to 45nm node. These challenges are then considered with respect to new CMP applications considered for 32nm and beyond.

**Introduction:** When CMP was first introduced to IC manufacturing in the early 1990s, common sense insisted that the process was too crude and defect riddled for the modern electron devices. However, rather than the predicted early demise of CMP, use of the technology expanded considerably in the 1990s. Table 1 shows the insertion of new CMP steps into Logic IC technology nodes by year of insertion as well as the technology element enabled by each CMP step. Introduction of these early CMP steps was key to the IC manufacturer's, ability to maintain scaling trends.

**Table 1 - Enabling CMP Technologies**

| Node | Year | CMP | Enabling |
|---|---|---|---|
| 0.8um | 1990 | ILD | Multilevel metallization |
| 0.35um | 1995 | STI<br>PSP<br>W | Compact isolation<br>Poly Si patterning<br>Yield/defect red. |
| 0.18um | 1999 | SiOF ILD | RC scaling |
| 0.13um | 2001 | Cu | RC scaling |
| 90nm | 2003 | SiOC ILD | RC scaling |
| 65nm | 2005 | | |
| 45nm | 2007 | RMG | HiK – Metal Gate |
| < 32nm | 2009+ | ??? | Continued Scaling<br>New Devices<br>New Architecture |

The insertion of new CMP steps slowed during the first part of current decade after the insertion of Cu CMP in the 130nm node. A primary reason for the slow down was concerns raised over CMP's inadequacies. Mainly that CMP was expensive, [illegible] variation that was not consistent with the scaling trends of the IC industry. While the first implementations of CMP were required to enable technology scaling, the original concerns around the crudeness of CMP appeared to prevent further insertion of CMP. During these years, methods were found to scale dimensions and improve transistor performance without adoption of new CMP steps.

With the 45 nm node however, CMP once again is used to enable a critical advancement in silicon technology. CMP is an integral component of the replacement metal gate (RMG) approach for defining metal gate structures required for HiK-metal gate dielectrics [1,2]. Cu CMP is also carried forward from the 65nm node to form Cu interconnects. However, unlike early technologies to utilize CMP, the 45 nm node requires a high degree of thickness precision and maintains a low tolerance to defects. Significant advancements in these two areas are required for CMP to be used successfully in the 45nm technology node.

**Requirements for RMG CMP:** CMP technology is extensively utilized to create metal gate electrodes for the introduction of HiK-metal gates at the 45 nm technology node [1, 2]. Figure 1 shows the RMG process flow utilizing poly opening polish (POP) and metal gate polish steps. Figure 2 shows a TEM micrograph of the resultant HiK-metal gate structure [2]. Because of the small dimensions and consequent small dimensional tolerance of the gate structure, traditional CMP processes are inadequate for these RMG steps. For functional devices and requisite yield, thickness control and defect performance has to be significantly improved over CMP processes used for previous technologies.

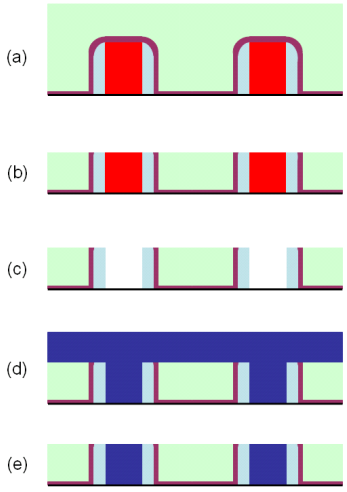


Figure 1. RMG Process flow showing CMP steps: (a) ILD0 deposition post transistor formation, (b) POP CMP to expose the poly-Si gate, (c) poly etch, (d) Metals [illegible] (see [1,2] for details)

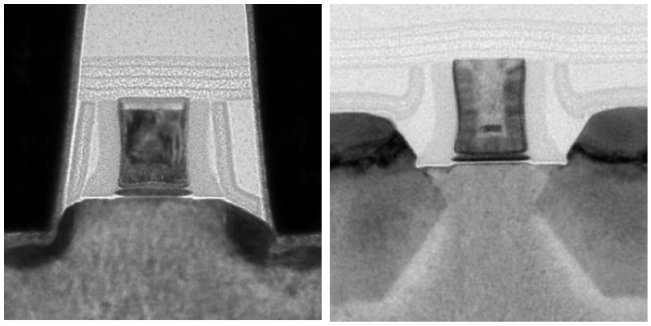

Figure 2 – TEM micrograph of 45 nm HiK-metal gate nmos and pmos logic transistors.[2]

**Table 2 – Integration Issues with RMG CMP**

| Issue | Cause | Impact to device |
|---|---|---|
| Gate Resistance Variation | Poor polish rate control (WIW, WID, WTW) | Parametrics |
| Poor Gate Fill | Thick Poly opening/ large aspect ratio | High gate resistance/defects |
| Unexposed Poly Si Gate | Low polish rate | Vt shift, high gate resistance |
| Residual Material (underpolish) | Non-uniform polish<br>Poor planarization | Shorting/opens<br>Particle generation |
| Raised S/D Exposure | Overpolish<br>Thick Epi S/D | S/D removal during Poly Etch |
| Contact Etch Window | Metal Gate height determines etch depth | Opens/Shorts for under/over etch |
| Bevel edge redistribution of poly/epi | Under/overpolish in bevel region generates defect source | Defects due to redistribution of under exposed gate or overpolished S/D regions |
| Structural Damage to device layer | High CMP shear forces. | Low Yield/Reliability |
| Strain/Stress relaxation | High shear force during CMP | Loss of strain induced carrier mobility |

Table 2 shows integration issues associated with the insertion of the new RMG CMP steps. Many of the integration issues in Table 2 arise from insufficient thickness control – either during CMP or incoming to CMP. Low polish rates at the POP step result in tall gates which are potentially not filled properly with gate metals (due to high aspect ratio). Taller gates also require longer contact etch potentially resulting in under etched contacts (Figure 3). Severe underpolish, such that the poly Si is not exposed, causes poly to remain in the gate, preventing proper metal fill. The resultant poly Si gate transistor will fail due to improper work function (Vt shift) and high gate resistance. Underpolish at the metal CMP step results in incomplete overburden metal removal and hence shorting. Note that the metal gate polish step must have sufficient overpolish to remove any topography evolved during poly opening. Excessive overpolish at either of the RMG CMP steps results in thin gates with high gate resistance and the potential for over etched contacts. Severe overpolished results in the exposure of the adjacent raised S/D regions which are then attacked in the post CMP poly removal etch step (Figure 4). These integration concerns lead to a narrow process window at both CMP steps.

Figure 5 shows the historical improvements of within die (WID) thickness variation obtained for STI/POP CMP processes. Due to thickness control issues listed in Table 2, circuit yield declines precipitously for WID values above the dashed line. Note that the historic 70% scaling from previous

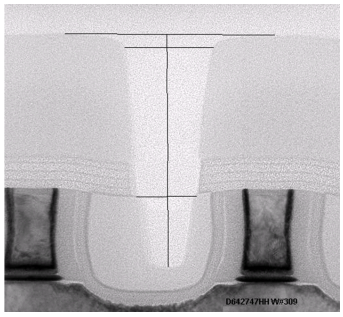

Figure 3. Cross section view of tall gate resulting in under etched contacts.

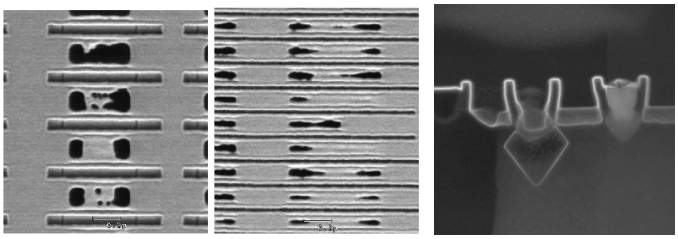

Figure 4. Top down view and cross section view of etched raised S/D exposed during POP CMP step and subsequently attacked during post CMP poly removal.

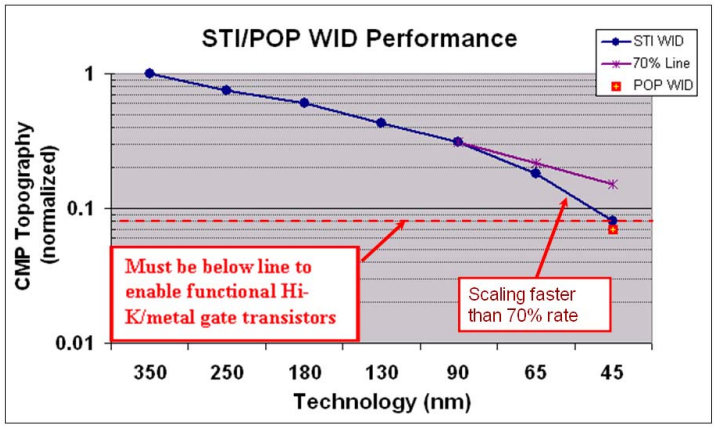


Figure 5 – Improvements in CMP topography by technology node. Traditional 70% scaling of thickness variation from 90 nm node was not sufficient to enable 45 nm HiK-metal gate.

The required thickness control is achieved via several key CMP innovations. First WID/topography control is achieved by selection of high selectivity slurry (HSS) and polish pad as well as the optimization of machine parameters around the selected consumable set. With the HSS, the polish process slows significantly when the ILD0 overburden is cleared and the gate is exposed resulting in an autostop to the process. Figure 6

shows the lowest WID achieved using different consumable combinations evaluated. Next WIW uniformity is optimized by structured experimental designs varying polish pressure, head and pad velocities, pad dressing, and polish head design. Figure 7 shows the optimization of WIW uniformity for various polish head conditions. Note that the most flat condition within the measured 3mm edge exclusion did not provide the best bevel edge performance and thus was not selected. As indicated in table 2, thickness control within standard edge exclusion is not sufficient as poor polish control of the bevel region of the wafer potentially leads to subsequent redistribution of bevel films during poly etch and subsequent wet etch operations.

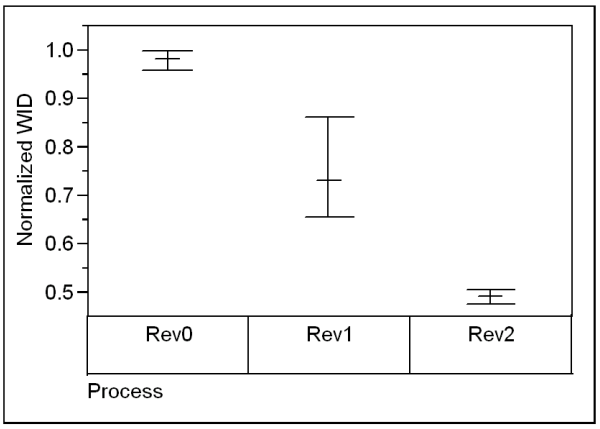


Figure 6. WID performance of several revisions of POP CMP process. WID is driven largely by consumables set (HSS slurry and pad).

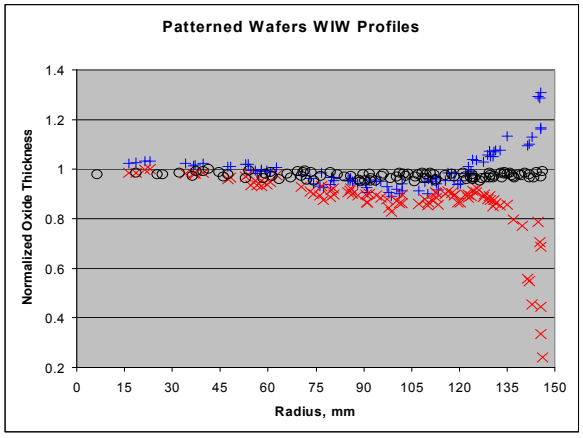


Figure 7. Cross wafer oxide thickness profile post poly opening polish (POP) CMP for three different process conditions. Oxide thickness variation translates directly to gate height variation. Note that polish performance at the bevel of the wafer must also be considered.

Significant CMP defect improvement is also required to enable HiK-metal gate yield. Typical CMP defects are listed in Table 3 - these defect modes were experienced during the development of RMG CMP processes. Because of the narrow dimensions at the gate layer, HiK-metal gate yields are particularly sensitive to CMP defects. Figure 8 shows the reduction in die killed by RMG CMP steps during the development of HiK-metal gate technology. Without significant improvements from the initial levels of RMG CMP defects Hi K-metal gate yield would not have been possible.

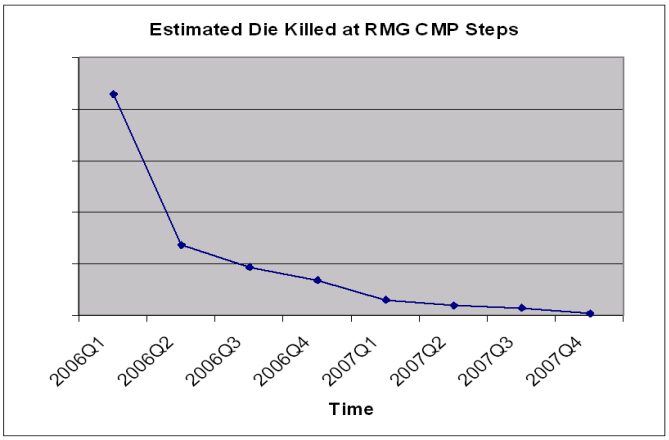


Figure 8. Reduction in die loss due to defect generation during RMG CMP steps.

**Table 3 – CMP Defect Modes**

| Defect mode | Potential causes | Impact to device | Potential solutions |
|---|---|---|---|
| Particles | Slurry/pad residue<br>Polish byproducts | Shorting/opens<br>Pattern distortion | Cleaner tooling<br>Clean Chemistries |
| Macro Scratches | Large/hard foreign particles on polish pad. | Pattern removal over multiple die. | Pad conditioning<br>Pad cleaning<br>Environment |
| Micro Scratches | Slurry agglomeration<br>Pad asperities | Shorting/opens | Slurry filters<br>Pad/Pad conditioning |
| Corrosion (metal CMP) | Slurry chemistry<br>Clean chemistry | Opens<br>Reliability | Passivating films<br>Chemistry optimization |
| Film Delamination | Weak adhesion<br>CMP shear force | Shorting/opens<br>Device parametrics | Improve adhesion<br>Low Pressure CMP |
| Organic Residue | Inadequate cleaning, residual slurry components | Shorting/opens<br>Disturbed pattern-ing of next layer | Cleaner tooling,<br>Slurry optimization,<br>Clean chemistries |

**BE Metallization Requirements:** Scaling of circuit dimensions at the 45 nm node also requires significant improvement to the Cu CMP process. As the metal line width scales, variation in the height of the line results in greater variation in resistance and capacitance of the line. Cu metal loss during CMP (dishing and erosion effects) is a primary cause of interconnect height variation – for the 45nm node, significant reduction in Cu loss is required to insure proper interconnect function. Figure 9 shows the improvement in Cu loss during CMP by technology node since Cu CMP was first used in the 130nm node.

Copper thickness loss is decreased as WIW and WID thickness control is improved. Cu loss is also decreased as improvements in surface topography at a given layer allow the reduction in the amount of oxide removed at subsequent layers. Underlying surface topography requires additional oxide removal to insure that all of the metal overburden is removed from the low lying areas of the surface topography. Hence

required at the lower BE metal layers which in turn translates to less oxide removal required in the upper BE metal layers.

Improvements in the Cu CMP WIW and WID removal rate uniformity at the 45nm node are a result of improvements in slurry selectivity as well as polish pad, pad dressing, and polish machine parameter optimizations. Figure 10 shows the reduction in M1 resistance variation that results from improvements in Cu line dimensional control at the 45 nm node [3].

As with the RMG CMP steps, the defect modes listed in table 3 are a challenge at Cu CMP steps. Because modern IC technologies contain up to 10 layers of metal, even low levels of defect densities in the Cu CMP step can have a significant impact on yield.

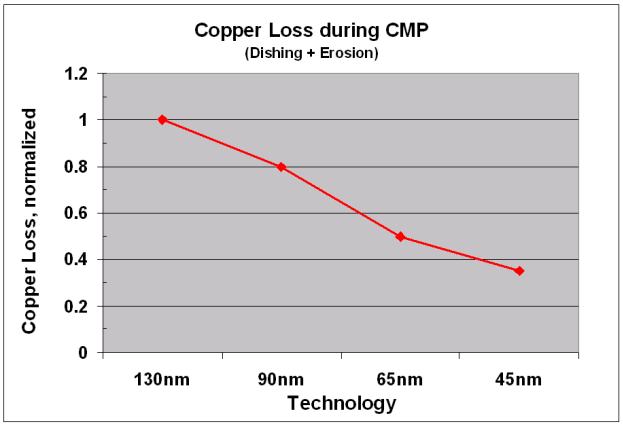


Figure 9. Reduction in copper loss due to CMP topography effects (dishing and erosion) by technology node.

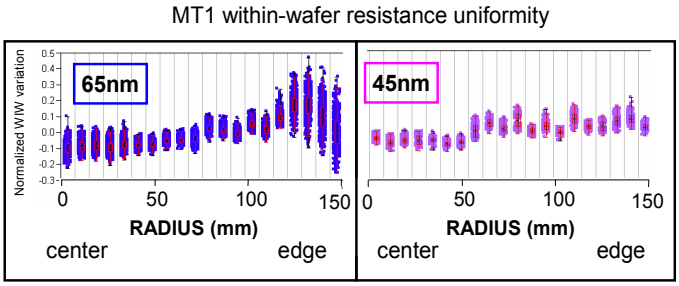


Figure 10. Reduction in M1 resistance variation (WIW, WTW) due to improvements in CMP planarization and trench patterning.

**New uses of CMP:** Recent conference proceedings and journal articles are rich with new potential uses of CMP considered for 32nm and beyond. Table 4 lists some intriguing new uses as well as some of the potential challenges they can be expected to bring. It is evident from the number of articles employing CMP that the technology is still considered a useful tool by process technology architects.

**Table 4 - Potential New CMP Applications**

| Application | CMP Enabling Aspect | Potential Challenges | Reference |
|---|---|---|---|
| FUSI replacement metal gates | CMP used to expose p and n gates independently | Inadvertent exposure of opposing gates. | H.Y. Yu, et al. [4] |
| Novel FUSI metal gates | Enables differential silicidation of poly-Si gate. | Requires CMP of dissimilar metals. | C. Park, et al. [5] |
| FINFET devices | Planarization of Poly Si, reduction of topography caused by fins. | Poly-Si thickness variation resulting in patterning issues. | A. Kaneko et al. [6] |
| FINFET devices | Damascene (inlaid material) approach to FINFET formation | Thickness variation caused by multiple CMP steps. | Y-S Kim, et al. [7] |
| 3D Integration – chip stacking | Oxide CMP post Cu CMP to recess oxide and promote Cu bonding | Smearing of Cu bumps | K.N. Chen et al.[8] |
| 3D stacked NAND Flash devices (2 papers) | 3D integration | Ultra-flat topography required for building multiple layers of devices. | S.M. Jung, et al.[9] E.K. Lai et al, [10] |
| Novel memory – Ferroelectric media | CMP eliminates roughness typical of ferroelectric material. | Device layer thickness control | D.C. Yoo, et al. [11] |
| Phase Change Memory | Planarize and expose phase change element | Thickness control of small device region | T. Nirschl, et al., [12] |

The multitude of new CMP uses under consideration is good news to the CMP technologist and CMP industry who have a vested interest in the expanded use of CMP. However, the difficulties experienced in introducing RMG steps at the 45nm node demonstrate that new CMP steps introduced into the front end of the line will require exceedingly tight thickness and defect control. Without such control, the new RMG CMP steps would not have successfully advanced from R&D to high volume manufacturing. The new CMP steps listed in table 4 can be expected to demand even greater control of thickness and defects - as will shrinking to dimensions to 32nm, 22nm, and beyond. Hence, new innovations in CMP will be required to successfully introduce these new technologies and to move them from R&D to HVM.

**Conclusion:** CMP has been shown to enable Si IC technology scaling since its inception in the early 1990s – most recently at the 45nm node. However, for CMP to be a useful tool in the integration of new technologies, significant advances must be made in the areas of defect reduction and film thickness variation. Reduction in defects and film thickness variation were critical to the successful use of CMP in the 45 nm technology node. To continue growth of CMP, the CMP industry must find processing conditions (slurry, pad, tooling) that improve performance in these critical areas.

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