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### United States Patent 1191

van Phuoc et al.

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### [54] BATTERY PACK HAVING A PROCESSOR CONTROLLED BATTERY OPERATING **SYSTEM**

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### Related U.S. Application Data

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[51]	Int. Cl. <sup>6</sup> H01M 10/44; H02J 7/00
[52]	<b>U.S. Cl.</b> 320/30; 320/48
[58]	Field of Search 320/5, 19, 20
	320/22, 30, 35, 48; 324/426; 361/96, 106
	364/483, 350, 550

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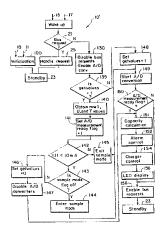
#### ABSTRACT [57]

A smart battery device which provides electrical power and which reports predefined battery parameters to an external device having a power management system, includes: at least one rechargeable cell connected to a pair of terminals to provide electrical power to an external device during a discharge mode and to receive electrical power during a charge mode, as provided or determined by the remote device; a data bus for reporting predefined battery identification and charge parameters to the external device; analog devices for generating analog signals representative of battery voltage and current at said terminals, and an analog signal representative of battery temperature at said cell; a hybrid integrated circuit (IC) having a microprocessor for receiving the analog signals and converting them to digital signals representative of battery voltage, current and temperature, and calculating actual charge parameters over time from the digital signals, the calculations including one calculation according to the following algorithm;

$$CAP_{rem} = CAP_{FC} - \Sigma I_c \Delta t_d - \Sigma I_s \Delta t + \Sigma \epsilon_c I_c \Delta t_c$$

wherein  $\epsilon_c$  is a function of battery current and temperature; and I, is a function of battery temperature and CAPFC. Superimposed on this equation is reset logic, that self corrects the value of  $CAP_{FC}$  with a capacity calculation at each full charge (EOC) and each end of full discharge.

### 32 Claims, 31 Drawing Sheets

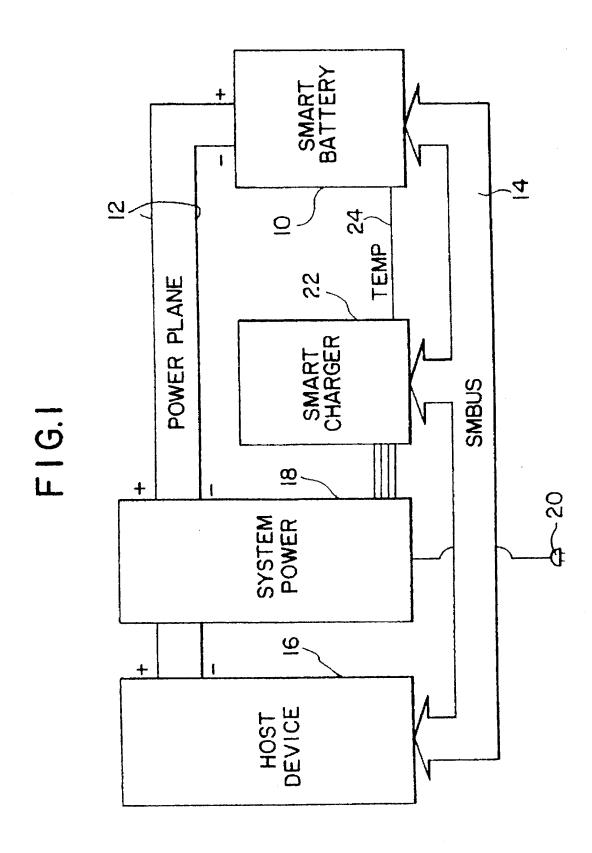




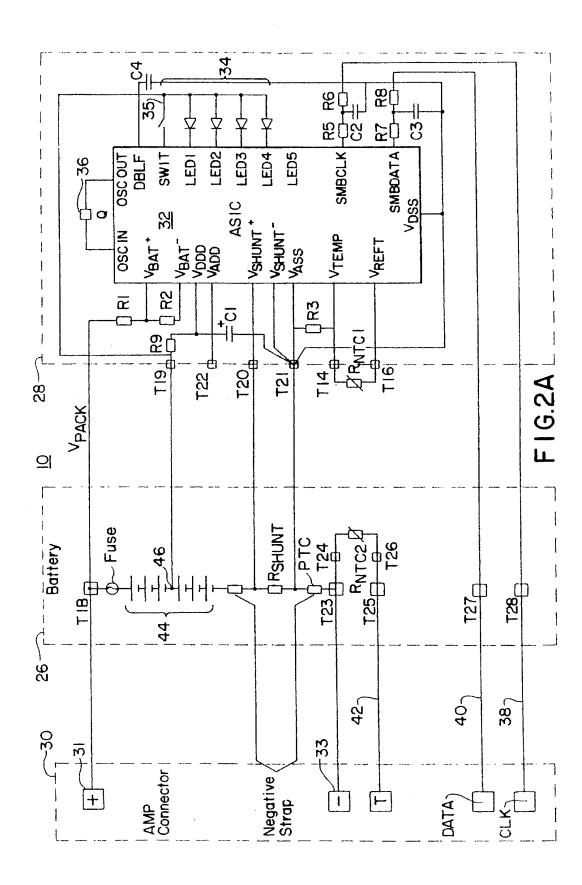
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SMBCLK 38 53 internal 8 bit bus program ROM 72 driver Interface ED. **SMBUS** 35 **20** 65 85 65a F16.2B POWER RESET 8 bit RAM 80 wake-up comparator circuit 67 on-chip 455kHz <u></u> register 55 **₩** extern 9 55



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