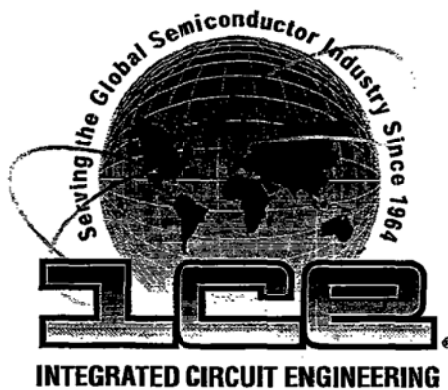


EXHIBIT B

Construction Analysis

Lattice ispLSI2032-180L CPLD

Report Number: SCA 9712-573



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INTRODUCTION

This report describes a construction analysis of the Lattice ispLSI 2032-180L Complex Programmable Logic Device (CPLD). One device packaged in a 44-pin Thin Quad-Flat-Pack (TQFP) was received for the analysis.

MAJOR FINDINGS

Questionable Items:¹

- Excessive metal 2 and metal 1 aluminum thinning.

Special Features:

- Three types of EEPROM cells were used.
- Mature technology using thin tunnel-oxide windows.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

TECHNOLOGY DESCRIPTION

Die Process and Design:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in an N substrate. No epi was used.
- Final passivation: A layer of nitride over a layer of glass (no die coat was present).
- Metallization: Two levels of metal interconnect were used. Both metal 2 and metal 1 consisted of aluminum with a thin titanium-nitride (TiN) cap and barrier. Standard vias and contacts were employed (no plugs).
- Interlevel dielectric: Interlevel dielectric (between M2 and M1) consisted of two layers of glass, with a spin-on-glass (SOG) between to provide planarization.
- Pre-metal dielectric: Consisted of a single layer of reflow glass (probably BPSG) over various densified oxides.
- Polysilicon: A single layer of dry-etched polycide (poly and tungsten silicide) was used. This layer formed all gates on the die, and in the cell array it formed the capacitors, word lines, and tunnel oxide device. Oxide sidewall spacers were used on all gates, and left in place.
- Diffusion: Standard implanted N+ and P+ diffusions formed the sources/drains of the MOS transistors.
- Wells: Twin-wells in an N substrate. A shallow N-well was located under the P-channel devices. N-channel devices were located within the P-wells. A step was noted in the local oxide at the edges of the well boundaries.

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