Handbook of
THIN FILM
DEPOSITION

Processes and Technologies

SECOND EDITION

O InAs$_{1-x}$ P$_x$ at 600°C (a)
△ GaAs$_{1-x}$ P$_x$ at 750°C (b)
◆ GaAs$_{1-x}$ P$_x$ at 550°C (c)
□ GaAs$_{1-x}$ P$_x$ at 700°C (d)
▼ GaAs$_{1-x}$ P$_x$ at 750°C (e)
▲ GaAs$_{1-x}$ P$_x$ at 600°C (f)
● GaAs$_{1-x}$ P$_x$ at 850°C (g)
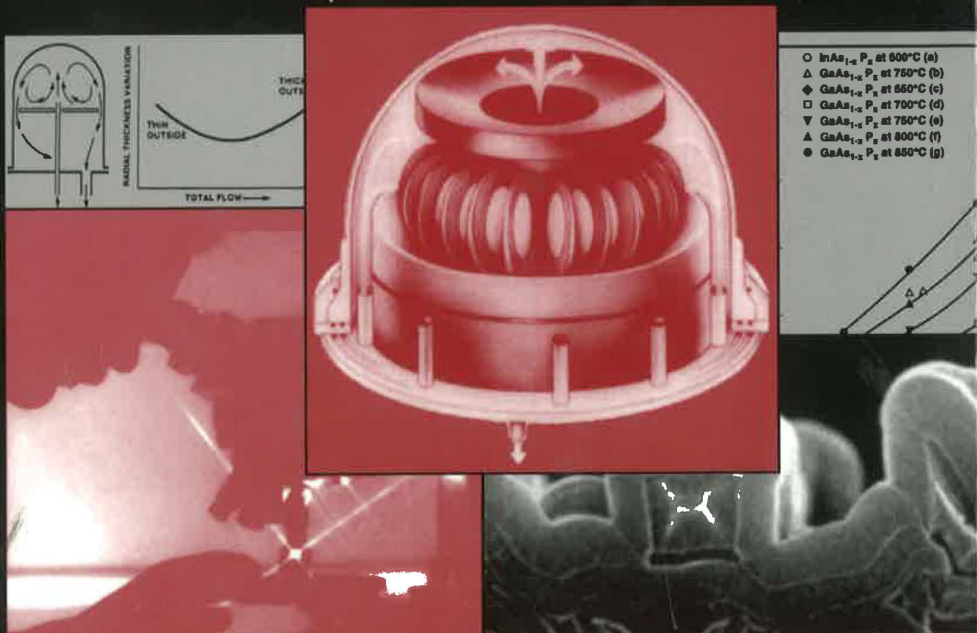
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Chemical Vapor Deposition of Silicon Dioxide Films

John Foggiato

1.0   INTRODUCTION

The use of chemical vapor deposition for various insulator films is paramount in the fabrication of semiconductor devices. The initial use of such films for passivation led to the development of low temperature techniques for film deposition. With the availability of silane, the pyrolysis of silane in the presence of oxygen at atmospheric pressure provided the deposition mechanism. Further enhancements in film characteristics through the use of phosphorus as a dopant within the film allowed the film to provide gettering of impurities during wafer fabrication. This led to the need for "smoothing" the films, now known as *reflow*, to minimize the sharp corners that metal lines had to cover. Reflow was further enhanced by the addition of boron as the dopant. This technology continues to be used today with better implementation of the reflow processes.

With the addition of more than a single metal layer, dielectric films were needed for electrical isolation. These dielectrics had to be deposited at less than 400°C to prevent affecting the underlying metal layer. Initially, using silane at atmospheric pressure, suitable films could be formed. The

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advent of plasma enhanced film deposition enabled or improved dense film deposition. Low frequency power during deposition improved both the film deposition process and the film properties. Both atmospheric and plasma enhanced films are extensively used today.

More recently, other reactants in the form of liquid precursors have been developed to provide other film properties, generally focused toward better step coverage. Although initially used at high deposition temperatures (>650°C), today TEOS (tetraethylorthosilicate) is used as a precursor in plasma enhanced deposition and for atmospheric pressure deposition with ozone. New precursors are being developed to deposit interlevel and intermetal dielectrics. As the technology drives towards 0.10 μm linewidths and gaps, better gap filling capabilities are needed and, as much as possible, dielectric films need an in-situ flow characteristic.

This chapter focuses on the deposition of dielectric films suitable for interlevel and intermetal dielectrics. A brief review of future directions of dielectrics for DRAM memory cells is given. Starting with atmospheric deposition of films, the first portion of the chapter covers the history of this technology. Plasma enhanced CVD follows with a short overview of new techniques, including HDP (High Density Plasma), ECR (Electron Cyclotron Resonance) and photo enhanced deposition.

After reviewing the basis for deposition for each of the technologies within their respective sections, current deposition methods are reviewed. The reaction mechanisms and the film characteristics that are obtained are given along with the basis by which the film properties are achieved.

An important advancement in achieving the ability to reflow deposited films came as a result of incorporating phosphorus as a dopant. Later optimizations included adding boron to form boron phosphorus silicon glass (BPSG). A review of the dopant incorporation mechanisms is given for this important step in enhancing integrated circuit reliability and manufacturability of smaller device geometries.

In summarizing the chapter, film properties from the different technologies are compared, especially the film properties required for applications in integrated circuit manufacturing.

2.0 OVERVIEW OF ATMOSPHERIC PRESSURE CVD

The initial techniques for depositing films of SiO_2 employed atmospheric pressure reactors (APCVD). Operating at atmospheric pressure,

the reactor designs were simple, yet provided high deposition rates. By using silane (SiH_4) and oxygen, injected as separate gases, the surface reaction on the heated wafer, typically at 400°C, grew films in the 2000 to 3000 Å/min range. The resultant films had suitable electrical characteristics, however, due to gas phase reactions, the step coverage was poor. Examples of such coverage are shown in Figs. 1(a) to 1(c) with the notation that a "bread-loafing" effect appears as the film becomes thicker. Figure 1a illustrates the conformal deposition initially achieved, however with additional deposition (Fig. 1b), the formation of the "bread-loafing" effect can be seen. With typical film thicknesses of 0.5 to 1.0 µm, narrow gaps will fill with a void (empty hole) forming as shown in Fig. 1(c). With a better understanding of the reaction mechanisms and the injection of reactants, some of these step coverage problems could be minimized. Various new reactors have been built around these enhancements and are used today.

(a)

(b)

(c)
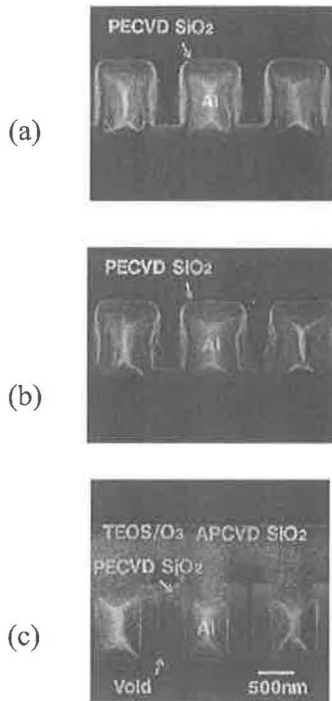
Figure 1. Step coverage comparison of dielectric films deposited at atmospheric pressure. (*a*) Initial deposition. (*b*) Further deposition shows "bread-loafing" effect. (*c*) Closure of gap with void formation.

Another approach to overcome APCVD limitations is to find new chemistries that can overcome the gas phase nucleation of the SiH_4 processes. TEOS was readily used in low pressure CVD systems at high temperature to decompose in the presence of oxygen and deposit high quality SiO_2 films. However, at atmospheric pressure, the decomposition was very slow due to minimal presence of reactive oxygen. During the mid 1980s, various researchers (i.e., K. Maeda[1]) proposed mixing TEOS with ozone in the presence of moderate temperatures. This resulted in growth of good oxide films at 400°C with growth rates of 0.1 μm/min or more. The advantages provided by the TEOS/ozone based films are excellent step coverage and in-situ flow resulting from the surface mobility of the reactants prior to formation of SiO_2. Other chemicals, to be discussed later, can serve as reactants and are being evaluated to further enhance film properties.

With atmospheric systems where the reactions take place in a "mass transport limited" regime, careful design of the reactant supply system is required to prevent reactions from taking place within the gas dispersion plumbing. Deposition uniformity is sensitive to the uniform availability of reactants and the exhaust of resulting by-products. Two gas dispersion architectures are in use today, one employing gas injectors with separated reactants evolving from each injector, and the other employing an areal injector. With the gas injector type, high velocity reactants are presented in a narrow line over the heated wafer, referred to as a "knife edge," while the wafer is moved horizontally under the injector. The reactant mixing takes place on the wafer surface. With the areal injector, also referred to as a *dispersion head,* the reactants are premixed prior to reaching the "reaction zone" and the hot wafer surface. This reactant supply technique enhances film thickness uniformity. One drawback of atmospheric reactors is the large amount of SiO_2 powder formed which has to be removed from the wafer area. This requires very good design of the by-product exhaust systems and good control of the reactant injector temperature.

In one APCVD reactor system, shown in Fig. 2a,[2] the wafers are held facing downward which minimizes the number of particles which stick to the wafer surface. In this case, reactants are brought through an areal dispersion head and reach the heated wafer by traversing a 6 mm air gap. By-products and unused reactants are exhausted around the areal dispersion head. In the knife-edge injector system (Fig. 2b),[3] exhaust is provided adjacent to the injectors and through a plenum around the reaction zone. For both types of reactors, the injector temperature must be

low (<100°C) to prevent premature reaction and minimize film deposition in the injectors.

Overall, APCVD technology continues to be used today for both logic and DRAM device fabrication. The SiH_4 based films with their low moisture content still dominate the logic market. With the in-situ planarization offered by TEOS/ozone based films, DRAM's use these films extensively in production.
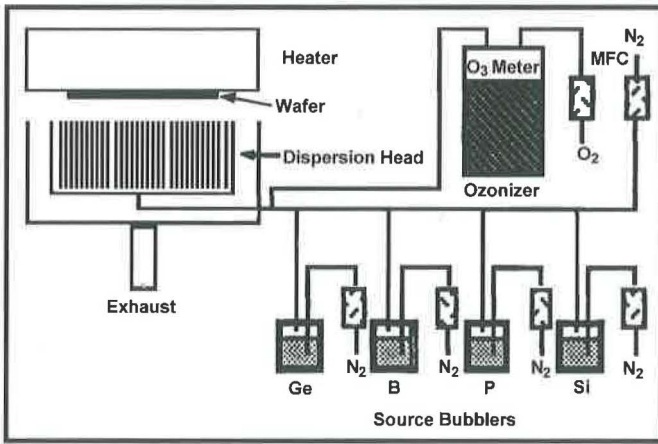
(a)
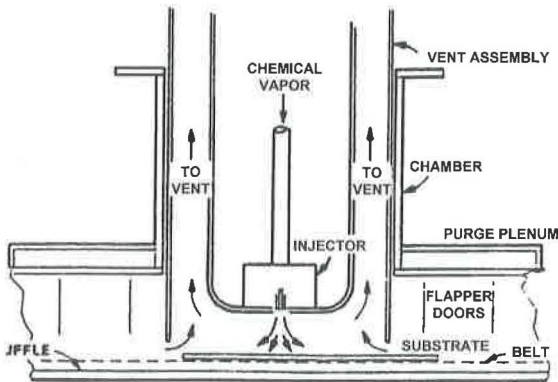
(b)

Figure 2. Comparison of APCVD reactor types. (*a*) Areal injector-dispersion head. (*b*) Linear injector.

2.1   Basis of Atmospheric Deposition

This section gives a basic overview of film depositions which take place at atmospheric pressure. Its purpose is to familiarize the reader with reaction dynamics which affect the resultant film properties. Extensive coverage of the reactions and their chemical representations is given in Refs. 4 and 5.

The chemical, SiH_4, is pyrophoric; the formation of SiO_2 takes place just through its exposure to oxygen. The fundamental reaction is given by:

Eq. (1) $$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2 \uparrow$$
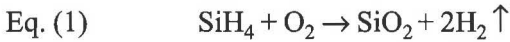
With the wafer at 400°C, an amorphous film of SiO_2 is formed which is used as the interlayer dielectric. In these reactions, it is important to minimize the residual H_2 in the film and to provide a film with suitable electrical properties. The film will undergo additional processing, primarily etching or in some cases densification, so it is necessary to have film thickness uniformity of better than 5%. A theoretical study of the reaction mechanisms and kinetics was given by Cobianu[6] with an emphasis on low temperature deposition.

In a similar manner, phosphorus, for subsequent reflow of the film, is added through the decomposition of phosphine: '

Eq. (2) $$4PH_3 + 5O_2 \rightarrow 2P_2O_5 + 6H_2 \uparrow$$
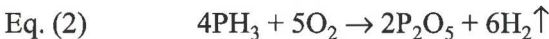
Through the incorporation of the phosphorus pentoxide (P_2O_5), generally in the range of 4 to 7 weight percent, the films will reflow at temperatures of 900°C.

In the reaction noted above, the hydrogen release is dictated by the mechanisms driving the reaction, one being deposition temperature. As hydrogen can introduce "hot electron" failures in integrated circuit devices, the amount left in the film must be minimized. These failures are due to hydrogen presence in the transistor gate, thus lowering the transistor transconductance. If allowable, a densification step, at up to 700°C, can be used to outgas the hydrogen. Film deposition uniformity is sensitive to wafer temperature, which must be kept to tolerances of less than 2°C across the wafer surface.

With TEOS, the reaction is one of oxidizing the reactants on the hot wafer surface. In this case the reaction is:

Eq. (3) $Si(OC_2H_5)_4 + 6O_2 \rightarrow SiO_2 + 10H_2O + 8CO_2$

$+$ by-product mixtures
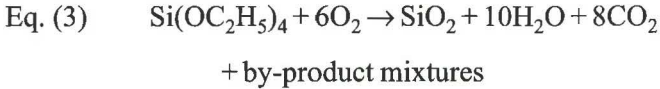
Note that in this case, water, also an undesirable residue within the film, is formed as one of the by-products. Unfortunately, this water with its hydrogen cannot be removed unless heated to the 500°C range. For oxides which are reflowed or densified at higher temperatures, the moisture may be eliminated. The TEOS/ozone deposition generates silanol (Si-OH) which also can be found in the film, however, these silanol groups can be eliminated by high temperature annealing.

In the case of TEOS, initial deposition is performed in a low pressure CVD (LPCVD) system employing the TEOS in vapor form with oxygen. The reactions are exemplified by the conditions given in the Arrhenius plot shown in Fig. 3.[1] At high temperatures, exceeding 750°C, moderate deposition rates are achievable through pyrolysis. With the addition of oxygen, the deposition can be significantly increased or the temperature may be lowered. However, for applications where low temperatures, <500°C are required, a new reaction system is needed employing ozone for the oxidizing agent. As noted, deposition rates greater that 1000 Å/min are achievable at 400°C. A theoretical model describing the kinetics is given in Ref. 7.

Deposition Rate of TEOS
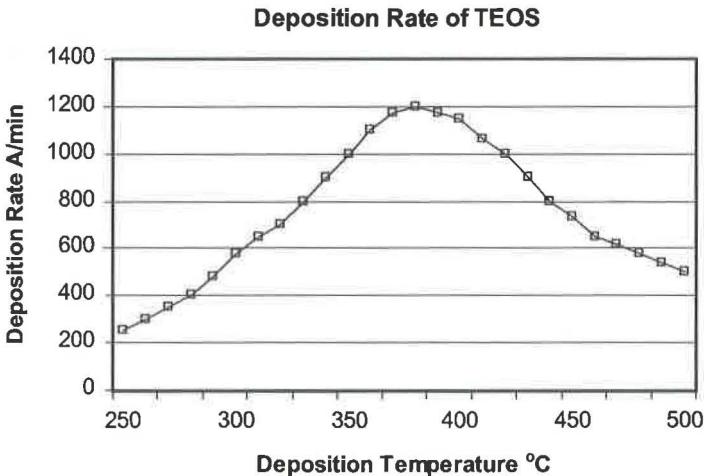
Figure 3. Arrhenius plot of CVD SiO_2 film formation using TEOS.

Both SiH_4 and TEOS based films are doped with phosphorus and boron to lower the films' melting points allowing reflow or planarization of the film. For SiH_4, the dopants are phosphine (PH_3) and diborane (B_2H_6), which are oxidized to form their respective oxides P_2O_5 and B_2O_3. For phosphorus oxide, an intermediate state can be formed, P_2O_3 which is unstable and must be converted to P_2O_5 for stabilization. This generally is done through the reflow cycle which takes place at 800°C to 950°C. At the lower temperature, little reflow takes place, however, the film is densified and stabilized. Above 850°C, the reflow process results in a better planar surface.

For TEOS based chemistries, the compatible dopants are also liquids, with a variety being available. To dope with boron, TEB (triethylborate) and TMB (trimethylborate) are used, the latter being developed more recently. Phosphorus doping is obtained with TMPO (trimethylphosphate) or TMPI (trimethylphosphite), the latter having less oxygen in the molecule, thus being more active.

The liquid chemical TEOS (tetraethylorthosilicate or the equivalent tetraethoxysilane) is a safer alternative to the gases silane and dichlorosilane. TEOS and its companion dopants, TEB and TMB for boron, and TMPO and TMPI for phosphorus, slowly hydrolyze into their respective oxides through the decomposition, for example, of the TEOS molecular structure shown here.
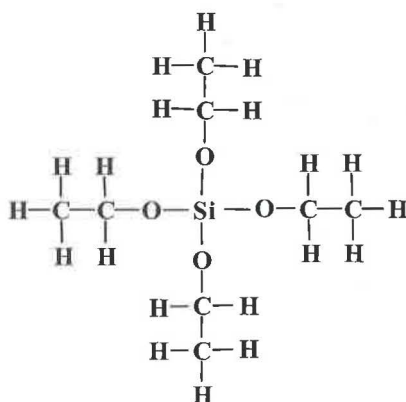
It is to be noted that the TEOS molecule already is oxidized and the conversion of TEOS to silicon dioxide is essentially a rearrangement of the molecular structure. The reaction for deposition requires removing two oxygen atoms. At high temperatures, 650 to 850°C, TEOS chemisorbs onto silanol (Si-OH) groups at the surface of the molecule, releasing the ethane molecule. Further desorption takes place and forms Si-O-Si bridges with neighboring molecules.

In a similar manner, the dopants TEB and TMB decompose to their oxide, B_2O_3, which becomes the dopant. In the case of phosphorus, TMPO and TMPI decompose to P_2O_3 initially, and with additional reaction and high temperature processing, convert to P_2O_5. These dopants are incorporated to allow the films to "flow" during subsequent high temperature annealing. This planarization facilitates subsequent lithography and improves reliability.

Other dopants, both gaseous and liquid are becoming available with germanium being the most practical. Germanium oxide, when combined with SiO_2 can further lower the melting point of the resulting film. Although still in the development phase, the four component system of Ge oxide, B and P oxides and silicate glass, resulting in GeBPSG, has shown good reflows at temperatures of 750°C or less. Although very porous resulting in moisture absorption, through multiple film structures, the dielectric has suitable electrical properties.[8] One application results from the higher refractive index of the Ge BPSG allowing optical waveguides to be formed on silicon wafers.

An application demonstrating the use of Ge as the dopant in BPSG films is described in Ref. 8. A range of doping levels were tried with RTP (Rapid Thermal Processing) being used for reflow. Overall, lower reflow temperatures were possible for film planarization. Additional characteristics using furnace flow process were reported in Ref. 9, with complete planarization at a temperature of 800°C.

In summarizing the chemical reactions and resulting films, Table 1 provides the basic parameters. With the development of organic silicon sources and their corresponding dopants, the safety problems associated with SiH_4 are minimized and new resultant film properties can be achieved.

Table 1. Temperatures and Reactants for Forming Silicon Dioxide Films at Atmospheric Pressure

| Film Formed | Base Si Source | Reactants | | Base Gas | Reaction Temp. Range |
		Phosphorus Dopant	Boron Dopant		
SiO_2	SiH_4			O_2	300–500°C
PSG	SiH_4	PH_3		O_2	300–500°C
BSG	SiH_4		B_2H_6	O_2	300–500°C
BPSG	SiH_4	PH_3	B_2H_6	O_2	300–500°C
SiO_2	TEOS			O_3	300–450°C
PSG	TEOS	TMPO		O_3	300–450°C
PSG	TEOS	TMPI		O_3	300–450°C
BSG	TEOS		TEB	O_3	300–450°C
BSG			TMB	O_3	300–450°C
BPSG	TEOS	TMPO	TEB	O_3	300–450°C
BPSG	TEOS	TMPI	TEB	O_3	300–450°C
BPSG	TEOS	TMPO	TMB	O_3	300–450°C

2.2   Parameters Affecting Chemical Reactions

As previously noted, the reaction sensitivity of atmospheric deposition focuses on the control of a mass-transport dominated reaction. With the reaction taking place at atmospheric pressure, the only control is the exhaust pressure for removal of unused reactants and reaction by-products. The gas injection to the reaction zone depends on the type of injector and conditions of gas mixing, so the resultant film composition and deposition rates vary. Varying the deposition temperature provides some variation in growth rates

and resultant film quality. We first discuss the parameters affecting SiH_4 based films followed by TEOS/ozone films.

The effects of exhaust on the deposition characteristics of a system are highly dependent on the reactor design, and a number of practical guidelines can be drawn from currently operating systems. In general, the exhaust and its control affect deposition uniformity and particles which may remain on the wafer. As these reactions are mass-transport driven, the exhaust affects the gas flows across the wafer surface which results in a nonuniform film deposition. Many particles are formed as part of the reaction, so the particle density within the reaction zone is also affected by system exhaust. Systems have evolved where exhaust sensitivity is being decreased, but the factors affecting exhaust must be carefully monitored including periodic cleaning of the system.

Temperature is a major factor in growth rate control, requiring careful control of not only the base wafer temperature, but its distribution across the wafer. Various means have been employed with multiple zone control and/or wafer susceptors with suitable thermal conductivity to achieve uniform wafer temperature. The temperature sensitivity for SiH_4 and TEOS are shown in Fig. 4 where for SiH_4, increasing the temperature increases the film deposition rate. In the case of TEOS, at low temperature deposition, a maximum growth rate is achieved at 380°C while growth decreases at lower and higher temperatures. To achieve excellent film thickness uniformity of better than ±2%, the temperature distribution across the wafer must be very uniform. Temperature variation of less than ±1°C across a 200 mm diameter wafer is required for the film thickness nonuniformity to be less than ±2%. The optimum deposition temperature is chosen on the basis of film growth rate. In the case of TEOS based films, temperature can also affect the film's ability to fill narrow gaps, so a compromise must be chosen between growth rate and gap-fill capability.

For the case of silane based films, the deposition rate at lower temperatures, ranging from 300 to 500°C, is linear with an activation energy of 10 eV.[6] In the case of TEOS, at lower temperatures, insufficient energy is available to achieve a high growth rate. As temperature is increased to 380°C, a maximum growth rate is achieved, typically 1000 Å/min for undoped oxide films. Further increasing the temperature causes the reactant ozone to decrease in concentration thus decreasing the TEOS/ozone reaction rate resulting in lower film growth rate.
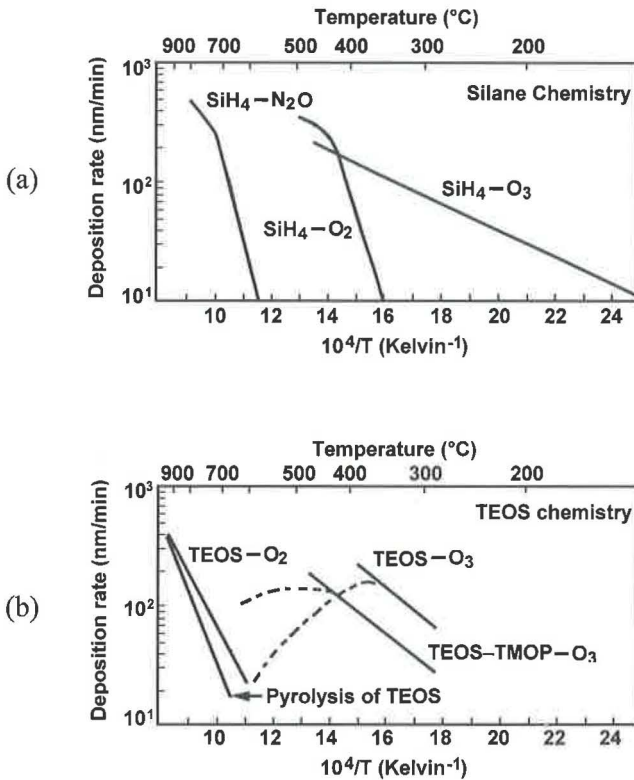
Figure 4. Comparison of deposition rate sensitivity with temperature for SiH_4 and TEOS.

With mass-transport reactions, the availability of reactants affects growth rate. Within the constraints of the reactor, namely exhaust and reactant transport, increasing the reactant flow rate increases deposition rate. In the deposition of doped films, there is an interaction between the phosphorus and boron reactants which can affect both growth rate and the level to which the dopants can be incorporated into the film. As reactant supply is increased, one must also adjust process exhaust to optimize film thickness uniformity.

In the case of TEOS/ozone chemistry, the reactants are derived from vaporization of the liquid chemicals. The vapor pressure, as depicted in Fig. 5, is sensitive to temperature requiring the chemical containers' temperatures to be precisely controlled. Generally the chemicals are kept

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at temperatures providing vapor pressures of 20 mm Hg. Systems now are being developed to directly inject the liquids through a vaporization system to more precisely control reactant flows.

With the variations described above, one can note the process parameters which can be varied to obtain optimal film characteristics. The principle parameters are listed in Table 2 indicating trends with deposition conditions.
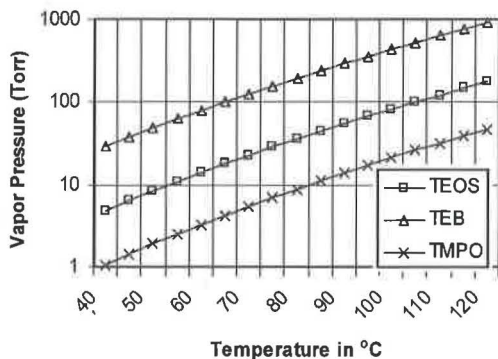
Figure 5. Vapor pressure of TEOS and dopants TEB and TMPO.

Table 2. Film Parameter Variations with Increasing Process Parameters

Process Parameters	Increasing Deposition Temperature	Increasing Reactant Temperature	Increasing Reactant Flow	Increasing Exhaust
SiH$_4$ Based				
Deposition Rate	Increases	Slight change	Increases	Slight change
Film Thickness Uniformity	Decreases at higher temperature	Slight variation	Decreases with higher flow	Very sensitive
TEOS/Ozone				
Deposition Rate	Increases to 380°C Decreases beyond 400°C	Increases with with increasing temperature	Increases with reactant flow	Slight changes
Film Thickness Uniformity	Decreases at higher temperature	Slight variation	Needs balance with exhaust	Very sensitive

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2.3   Reaction Chamber Designs

A variety of reactors have been developed for atmospheric film deposition. Original designs employed a pancake configuration with wafers subjected to a gas stream from injectors dispersed around the reactor. With continual adjustments of the injectors and methodical placement of the wafers, reasonable uniformities were achieved on wafers up to 100 mm diameter: The introduction of the Applied Materials 2100 launched a new concept that had fixed areal type injectors and moved the wafers under the injector. Wafers were heated through the moving chain, with wafers placed on plates. This reactor led to the reactors available today.

Reactors of the moving belt type have a linear injector that covers the belt width plus some overlap.[11] As depicted in Fig. 6, the reactant gases are injected from separate nozzles and allowed to mix over the hot wafer. The resultant film deposition takes place with the peripheral exhaust controlling the expenditure of unused reactants and by-products. Nitrogen curtains are used to control gas flows and dispersion. Today's reactors have three or four injectors resulting in an equivalent deposition rate of 2000 Å/min.
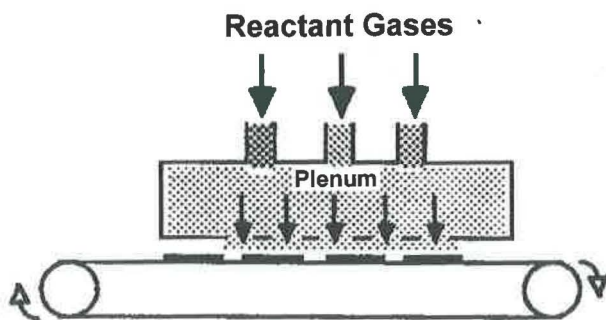
Figure 6. Reactor schematic showing wafer moving under injectors.

An areal type reactor utilizes a wider area injector, achieving more control over film thickness uniformity by depositing over the entire wafer. Further expanding the use of an areal injector, a system with multiple reactors for deposition has been developed. Utilizing up to five single wafer reactors, the entire film thickness is deposited within the reactor

with good throughput and film thickness uniformity.[12] Taking advantage of the averaging effects when depositing a portion of the film across multiple reactors, the system concept shown in Fig. 7 was developed. With five reactors, 20% of the film is deposited at each reactor resulting in a high number of wafers processed (high throughput) through the system.

In all the reactors, the mechanical designs have been optimized to minimize the formation of particles and achieve high deposition rates. As deposition is very dependent on the injector-to-wafer distance, the flow dynamics of reactants is controlled by process exhaust. Injector cooling is important to reduce deposition on the injector while still allowing what is deposited to adhere to the injector to prevent particles on the wafer surface.
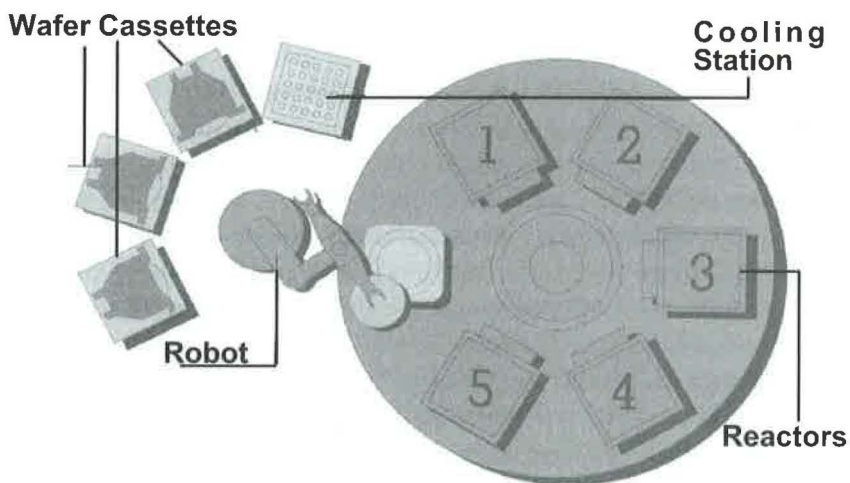
Figure 7. Dispersion head type reactor with five reaction chambers. *(Courtesy of Quester Technology.)*

2.4   Process Exhaust and Particle Containment

As previously mentioned, the process exhaust controls the deposition characteristics of the injector with film thickness uniformity depending on the mechanical configuration and the resultant exhaust. The reactant lifetime and its reaction on the surface control the deposition rate, so the process exhaust can also affect the resultant deposition rate. This applies to both the linear and areal injector types.

Another effect of the exhaust is particle control. In these deposition processes, the resultant by-products are in the form of particles and must be removed prior to reaching the wafer surface. Exhaust control is used to maintain laminar flows and levels to assure minimal particle formation. In the areal reactor shown in Fig. 7, the wafer is held facing downward with reactants injected upward toward the hot wafer.

Another aspect of particle containment relates to particles on the wafer's backside. With the belt system, an in-situ cleaning of the belt is performed during operation. With the areal deposition system, the wafer is held to a susceptor by vacuum. Sealing of the wafer edge to the susceptor is important in minimizing backside particles.

Atmospheric pressure deposition systems continue to provide films suitable for high-density, small-geometry semiconductor devices. Whereas the emphasis is toward the use of TEOS/ozone due to the film's planarization capability, continued system optimization and new chemistries will further extend the use of APCVD. We now review another technology for depositing films that uses plasmas to initiate and sustain the chemical reactions.

As wafers are processed in a reactor, the uniformity of the film deposition is dependent on the uniformity of the gas distribution, the wafer temperature and the reactor exhaust characteristics. To optimize the film thickness uniformity, it is advantageous to deposit portions of the film in multiple reactors, thus through averaging of the non-uniformities, a better uniformity is achieved. This was initially demonstrated for sputtering of metal films and then implemented in a number of ways for CVD. The Novellus system utilizes multiple deposition sites within a single vacuum chamber for PECVD deposition of films. The Quester system employs multiple reactors in a circular configuration at atmospheric pressure. The reactor of Fig. 6 uses multiple reaction sites in a linear configuration. Experimental data on the Quester system[13] has shown that a single reactor uniformity of 2.5% can be reduced to less than 1% through averaging and balancing reactor operation.

3.0 PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION

The previous discussion focused on atmospheric deposition of silicon dioxide with good deposition rates and resultant film characteristics, however, improved deposition rates and denser films are obtained by using plasma for promoting deposition reactions. With the ability to vary the input energy to the reactor via the RF used to generate the plasma, the

deposition rates, and to some extent, the film properties can be optimized. The stress in most films deposited at atmospheric pressure is tensile. The addition of secondary low frequency RF power provides a mechanism for varying the resultant deposited film stress, making it compressive.

3.1   Deposition Rates

As noted in Fig. 8, the film parameters for plasma enhanced CVD (PECVD) films can be controlled through varying the plasma-sustaining RF power as well as varying the flow rates of reactants.[13] In addition, working in a vacuum provides a longer mean free path, hence time for the reactants to react and form a film. This results in a higher usage efficiency of the reactants, although at the expense of a more complex system. A comparison of atmospheric and PECVD in Table 3 indicates the characteristics of PECVD systems.

With PECVD technology, other process variables are available to control film characteristics; this flexibility leads to the adoption of PECVD for dielectric film deposition. A plasma process requires control and optimization of several deposition parameters. Within the reaction zone, primarily the wafer temperature must be controlled to achieve good film uniformity. Other parameters providing the reactant decomposition energy include RF power density, frequency and possible duty cycles. The deposition process is dependent in a very complex and interdependent way on these parameters, and the gas composition, flow rates, temperature and pressure must also be considered.

A review of the process parameters as they affect the film characteristics shows the trends for different film parameters. PECVD TEOS films will absorb moisture when exposed to ambient as demonstrated by an increase in dielectric constant. Depositing at higher temperature provides a denser film with lower moisture absorption. Through the use of a lower frequency (about 400 kHz) in conjunction with the RF used for chemical disassociation during deposition, the film is densified which also reduces the moisture absorption. Increasing the deposition rate through higher reactant flow increases the hydrogen content within the film. The hydrogen is found in the form of -OH and water, both of which can be changed by varying reactor operating parameters. To optimize the moisture resistance of these films, both low and high frequency power are used resulting in a film with compressive stress. Also, the deposition parameters are optimized through the deposition rate and by depositing at the highest temperature possible.
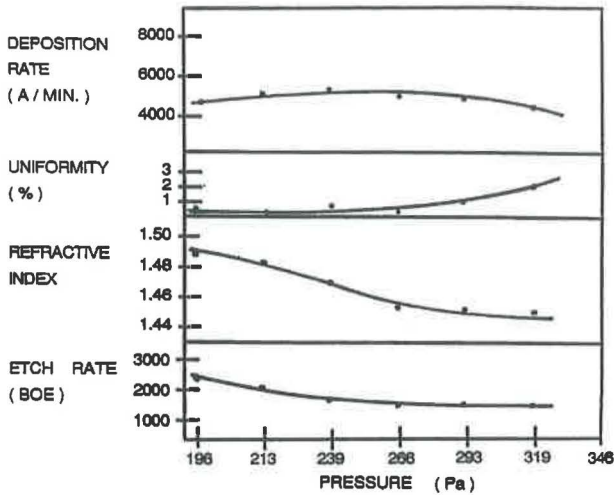
Figure 8. Film characteristic variation by varying reactor power.

Table 3. Comparison of APCVD and PECVD Systems

Comparative Parameter	APCVD	PECVD
Deposition Rate		
SiH_4 based	1000 to 3000 Å/min	5000 to 6000 Å/min
TEOS based	1000 to 2000 Å/min	5000 to 7000 Å/min
Film Stress	Tensile	Tensile→compressive
Dual frequency		Compressive
Film H_2 Content	9 to 12 at %	3 to 5 at %
	as Si-OH and H_2O	as Si-OH
System Complexity		
# of reactors	1 to 5	1 to 4, clustered
	4 linear reactors,	Single with up to
	5 areal reactors	7 deposition sites
Wafer Load/Unload	Robot at atmospheric	Vacuum load locks,
	pressure	robots
Vacuum System	None	Multiple stages

Three types of PECVD systems are in use today: 1) single wafer, 2) multiple wafer, clustered tools, and 3) systems employing a single chamber with multiple deposition sites to achieve better film thickness uniformity. Other features being implemented include a dc or RF bias (dc: 400 kHz) for modifying the film stress. Examples of these are shown in Fig. 9. In Fig. 9a, a single chamber reactor is shown with associated plasma confinement shields. These assist in minimizing deposition outside the area of the wafer and thus particles which may be generated within the system. RF power is applied through the "showerhead" electrode which injects reactants into the process chamber. A second bias, either dc or more recently, low frequency RF, can be applied to the lower electrode. This bias controls ion species bombardment of the deposited film, especially during deposition, leading to an ability to control film stress from a low compressive to a high compressive value.

To attain higher productivity, multiple reactors may be clustered as shown in Fig. 9b. Each of the reactors is independently controlled allowing deposition of films with varying process conditions during deposition. This provides the capability of depositing "sandwiched" layer films to address varying film deposition requirements.

Additional productivity can be obtained by multiple reaction locations within a large single process chamber as shown in Fig. 9c. Although less flexible in terms of process variables, the concept provides high throughput and better film uniformity through the "averaging" effect as discussed in Sec. 2.4.

The important parameters affecting PECVD film during deposition encompass the reactant flow rates, wafer temperature, and rf power used to sustain the plasma. Secondary effects to change film properties include the bias, generally applied to the wafer holder, and plasma confinement to minimize particles. To clean the systems, the convenience of changing process gas and using the plasma to generate reactive species is very convenient. A listing of these parameters as related to film properties is given in Table 4.

Various techniques are being employed to further enhance PECVD films with the incorporation of high plasma density sources. These new directions for depositing high density, good gap-fill films will be described later. We will review some of the chemistries being explored to enhance films characteristics.
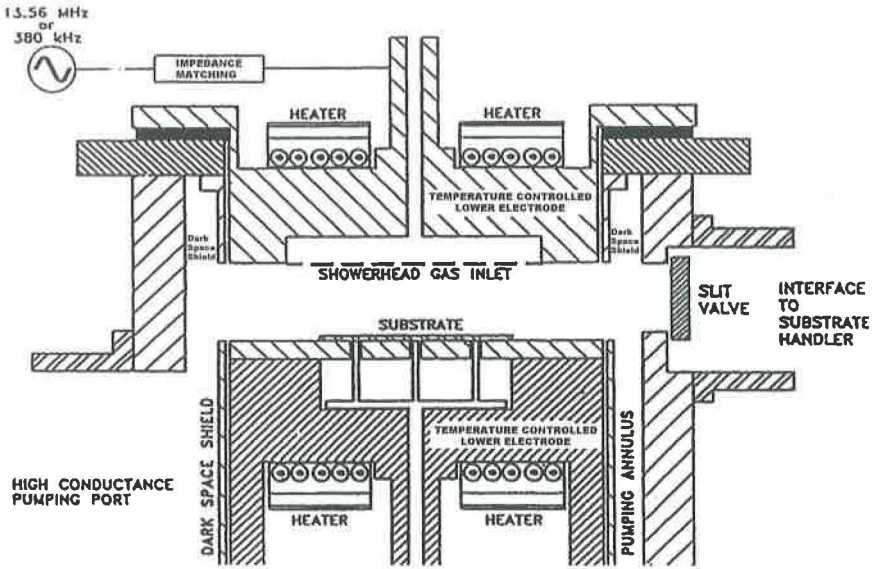
(a)
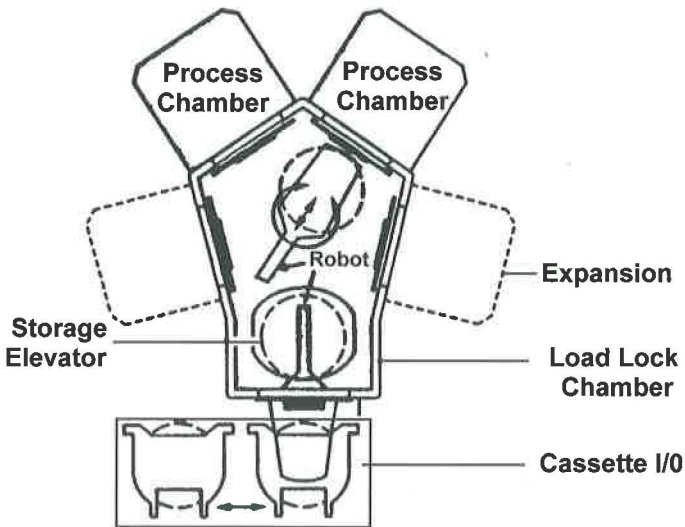
(b)

Figure 9. Various PECVD reactor configurations. (*a*) Single reactor with plasma confinement shields *(courtesy STS Corporation)*. (*b*) Multiple reactor system in cluster tool configuration. (*c*) Multiple deposition sites within single chamber.
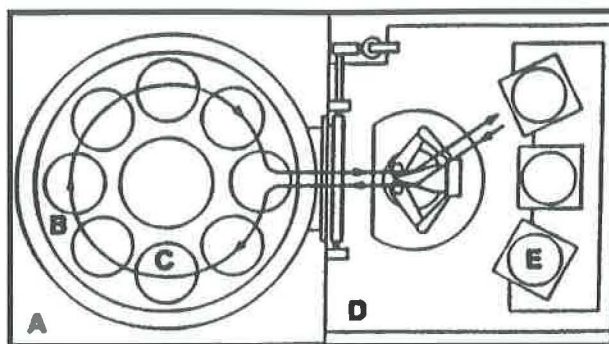
A = Process Chamber
B = RF Powered Al Susceptor
C = Deposition Stations
D = Vacuum Loadlock
E = Cassettes (3)

(c)

Figure 9. *(Cont'd.)*

Table 4. PECVD Process Parameters as Related to Deposited Film

Deposited Film Parameter	PECVD Design and Process Control Parameters
Deposition Rate	Electrode/Showerhead Proximity Reactant Flow, RF Power
Thickness Uniformity	Electrode/Showerhead Parallelism Reactor Chamber Vacuum Exhaust
Stress	Dual Frequency (Bias) RF Deposition Rate
Hydrogen Content	Operating Vacuum Levels Reactants Used Deposition Rate
Density	Bias Level (RF/Bias Power Ratio) Operating Vacuum Levels

3.2 Film Characteristics for Different Chemistries

With the reactivity control attainable with PECVD, a variety of chemistries have been developed for depositing silicon dioxide and silicon nitride films. A comparison of these is given here to address different applications.

As a follow-on to APCVD, the initial chemistry used silane and oxygen. The reaction given by:

Eq. (4) $$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2 \uparrow$$
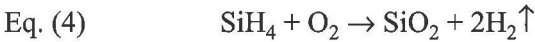
which indicates the possible inclusion of hydrogen in the film. As previously mentioned for the case of APCVD, hydrogen can induce "hot electron" effects which can lead to circuit reliability problems. With the additional available energy to disassociate molecules, N_2O was introduced as the oxidant for SiH_4. The PECVD oxides contain hydrogen in various forms, Si-H, Si-O-H and H-O-H, thus a low level of nitrogen is incorporated in the film leading to decreased diffusivity of hydrogen.

Takasaki[15] describes the use of N_2O as the oxidizing reactant with the resultant film properties. Through the use of N_2O, the "critical" amount of oxygen is generated for film deposition, however the removal of hydrogen may be decreased leading to a higher level of hydrogen in the deposited film.

Another important parameter comprises the film's ability to fill narrow-high aspect ratio gaps. This is becoming more important as films are subjected to CMP (Chemical Mechanical Polishing) after deposition; the films must be free of voids. A number of mechanisms have been proposed as the means to achieve excellent gap-fill. Fujino, et al.[12] have proposed a mechanism for APCVD deposited films. The formation of oligmers in various steps as the reactants reach the wafer surface provides a means of moving across the patterned wafer surface. This molecular mobility allows the oligmers to flow thus providing void-free gap filling. In a similar manner, the same mechanisms have been proposed in PECVD deposition.[15] With the added low frequency bias used in PECVD, it is proposed the formed ions are accelerated into film formation, thus enhancing gap fill compared to operating with a single frequency.

The use of TEOS as the silicon-supplying reactant provides a more conformal film than obtainable with SiH_4 chemistry. With SiH_4, there is a slow surface migration leading to a reentrant angle as shown in Fig. 10(a).

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Experience gained with TEOS in APCVD reactors has enabled rapid surface migration resulting in a conformal step coverage regardless of topography. With a similar process environment and low pressure, the TEOS films deposited by PECVD show the same conformal characteristics as shown in Fig. 10(b).

Use of PECVD oxide films for various applications depends on the allowable hydrogen content, the film step coverage, and resultant stresses. Table 5 lists the various films with possible applications.

(a)

(b)

(c)
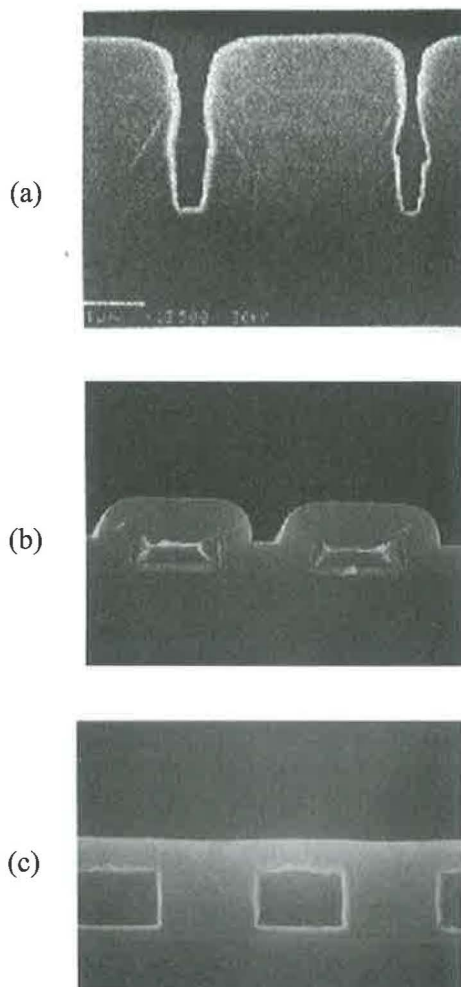
Figure 10. Film deposition characteristics: (*a*) SiH$_4$ based films, (*b*) TEOS in APCVD or PECVD, and (*c*) after reflow.

Table 5. PECVD Oxide Films and Their Applications

Film	Chemistry	Application
SiO_2	SiH_4, O_2	Interlevel (ILD), Intermetal (IMD) Dielectric
SiO_2	SiH_4, N_2O	ILD, IMD, Hydrogen Sensitive ICs
SiO_2	SiH_4, N_2O	Spacer Oxide, LDD Structure
PSG	SiH_4, PH_3, O_2 or N_2O	ILD, IMD
BSG	SiH_4, B_2H_6, O_2 or N_2O	Special Applications
BPSG	SiH_4, PH_3, B_2H_6, O_2	ILD
SiO_2	TEOS, O_2	ILD, IMD
SiO_2	TEOS, N_2O	ILD, IMD

Similar to APCVD, one important aspect of the dielectric films encompasses use of boron and phosphorus doping to lower the films' melting points. With the conformality of the deposition, films are heated and "reflowed" to obtain a "smoother" film for subsequent processing. Figure 10(b) shows films at deposition with excellent conformality as deposited. Heating to 700°C leads to film densification, and some depletion of incorporated unreacted species, i.e., Si-H, Si-O-H, H-O-H, however, the film topography is nearly the same as deposited. Heating to 850°C, typically for 30 minutes in nitrogen, causes the film to soften and reflow, thus providing a smoother topography. To achieve this reflow, boron and phosphorus are incorporated at levels of 3.5 weight percent (wt %) and 5 wt % respectively. Figure 10c shows such films reflowed at 900°C where nearly true planarity is achieved. Higher concentrations of boron and phosphorus allow lower temperatures and shorter times to be used, however, the films tend to readily absorb moisture from the environment.

With PECVD and SiH_4 based chemistry, the dopants diborane (B_2H_6) and phosphine (PH_3) are utilized. When TEOS is used, compatible chemistries, reactants in liquid form, are available; TEB and TMB for boron, TMPO and TMPI for phosphorus. In both applications, the doping reactants are delivered in a manner similar to the silicon supply, just requiring additional control hardware and software.

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With the higher energy required to form Si_3N_4 from SiH_4 and N_2, the PECVD technology allowed deposition of these films at low temperatures. Used primarily as a passivation layer, the Si_3N_4 film deposition temperature cannot exceed 380°C. As a passivation layer, it behaves as nearly an impervious diffusion barrier, with a low compressive stress, and its coverage of underlying layers, especially metal, is conformal. With PECVD, the stress can be varied, generally to achieve a low compressive level, and with uniform deposition, a pinhole free film can be obtained.

With PECVD, the film is nonstoichiometric and contains hydrogen. Ammonia has been also used as the nitrogen source; the NH_3 molecule disassociates at lower energy than N_2. Table 6 provides a comparison of the nitride films in use today and their applications.

Table 6. Silicon Nitride Film Properties and Applications

Property	Deposition Method	
	LPCVD	PECVD
Composition	Si_3N_4	$Si_xN_yH_z$
Si/N ratio	0.75	0.8–1.0
Density	2.8–3.1 g/cm^3	2.5–2.8 g/cm^3
Refractive Index	2.0–2.1	2.0–2.1
Dielectric Constant	6–7	6–9
Dielectric Strength	1×10^7 V/cm	6×10^6 V/cm
Stress at 25°C on Si	1.2–1.8×10^9 dyne/cm^2 Tensile	1–8×10^9 dyne/cm^2 Compressive
Step Coverage	Fair	Conformal
H_2O Permeability	Zero	Low–None
Na Penetration	<100 Å	<100 Å
Application	Selective Oxidation Gate Dielectric	Passivation

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4.0   PROPERTIES OF DIELECTRIC FILMS

There are secondary film properties which are becoming very important for high density, small geometry integrated circuit applications. These are summarized here with some explanation of their effects on circuit performance.

With smaller geometry metal lines, the stresses introduced by the dielectric films can affect reliability. The APCVD films comprised of TEOS/ozone are tensile thus affecting the electromigration of underlying metal lines. A slightly compressive film is desired to counter the tensile stress within the metal films. PECVD films are compressive and their level of compressiveness can be controlled by utilizing a low frequency bias during deposition.

Film thickness uniformity becomes important in subsequent processing steps which involve etching small via holes for intermetal level connection. The etch process can be continued for a short time beyond the nominal endpoint to assure via holes are completely etched, but not too long, otherwise regions where an endpoint is reached initially will have oversize vias. As smaller geometries and larger wafers are being used, the thickness uniformity becomes very important.

Particles introduce point defects which translate to a number of circuit defects, depending on the particle composition and its position. The particles contributed by the CVD processes generally are SiO_2 in various forms, from "dust" to pieces which come from depositions within the reactor. With the continuing focus on this problem, today's CVD reactors have become quite clean with maintenance playing a major role in keeping particle counts to a minimum.

Although not heavily emphasized, the refractive index indicates the films' optical properties but also gives an indication of density and dielectric constant. With the SiO_2 films, the refractive index provides an indication of the hydrogen content in the form of Si-OH or water. The content can be kept at a minimum by monitoring the deposition process operation through the refractive index measurement.

Film density is measured in a number of ways, the easiest being etch rate in a fixed diluted HF solution, typically 100:1 water:HF. The importance of this parameter is in subsequent etching processes to provide repeatability of the etch process. The etch rate also indicates the films' composition, with higher content of SiO_2 giving a lower etch rate.

Reactants for film deposition have achieved remarkable cleanliness through the distillation processes for liquids and their handling and transport. The resultant impurity levels are near or below the detection levels of SIMS and other analytical techniques.

Electrical properties constitute dielectric constant and strength. With the concerns of circuit performance degradation, a lower dielectric constant is desired, however, the basic deposited oxide dielectric constant still remains higher than thermal oxide. Some oxide films have moisture, or are Si or N rich, and the dielectric constant is above that of thermal oxide. Dielectric strength is adequate, greater than 5 MV/cm, for the majority of applications. In high voltage applications, the impurities or unreacted species may introduce premature dielectric background.

Step coverage capability of the films is very important for achieving high yield and high reliability. Substrates typically have different interconnect layers crossing over multiple steps of various heights, and the films' coverage determines circuit isolation. Going to smaller geometries further requires better step coverage as films will need to be thinner for acceptable via hole definition.

As a contradiction to step coverage, there is the need for planarization of the film surface. Ideally, the film can be planarized as part of the deposition process, however, such is not the case today. The APCVD TEOS/ozone process provides a degree of planarization especially for small gaps. The rapid molecular migration during deposition provides some planarization along with good filling of gaps between metal or polysilicon lines.

In Table 7, the properties of films are compared to determine suitability for an application.

5.0   NEW DEPOSITION TECHNOLOGIES

With smaller geometries for high performance/high density semiconductor technologies, dielectric films need the capability to fill gaps between polysilicon and metal lines. The typical structure shown in Fig. 11 requires a dielectric film to completely fill the gap without voids as shown in Fig. 11a. The ideal structure shown in Fig. 11b provides the desired filling of metal lines assuring no voids are present. As may be surmised, the voids can accumulate impurities during subsequent processing along with making it difficult to lithographically define contact vias.

Table 7. Comparison of Deposited Film Properties

Type of Film	SiO_2					Si_3N_4
Deposition	APCVD	PECVD	PECVD	Dual Freq. PECVD	Dual Freq. PECVD	PECVD
Chemistry	SiH_4	SiH_4	TEOS	SiH_4	TEOS	SiH_4
Primary Reactant	O_2, O_3	O_2, N_2O	O_2	O_2, N_2O	O_2	NH_3
Dopants: Boron	TEB, TMB	B_2H_6	TEB, TMB	B_2H_6	TEB, TMB	
Phosphorus	TMPO, TMPI	PH_3	TMPO, TMPI	PH_3	TMPO, TMPI	
Stress Type	Tensile	Tensile to Compressive	Tensile to Compressive	Tensile to Compressive	Tensile to Compressive	Compressive
Stress Level 10^9 dynes/cm²	1.5 to 2.0	<1.5	<1.5	<1.0	<1.0	1.0
Hydrogen Content Level	10%	1–2%	3%	1%	3%	15%
Form	H_2O Si-OH	Si-H	H_2O Si-OH	Si-H	H_2O Si-OH	Si-H
Deposition Rate Å/min	1000–2000	5000–6000	3000–4000	5000–6000	3000–4000	1800
Uniformity (1,000 to 10,000 Å)	<3%	<3%	<3%	<3%	<3%	<3%
Refractive Index	1.44	1.45–1.46	1.45–1.47	1.45–1.46	1.45–1.47	2.0–2.1
Dielectric Constant	4.3	4.1	4.2	4.1	4.2	6–9
Dielectric Strength MV/cm	6–7	6–7	6–7	6–7	6–7	>7
Step Coverage	Gap-fill	Conformal	Gap-fill	Conformal	Gap-fill	Conformal
Mechanical Properties Hardness, GPa	3.18		8.24			25.2
Young's Modules, GPa	91		101			170
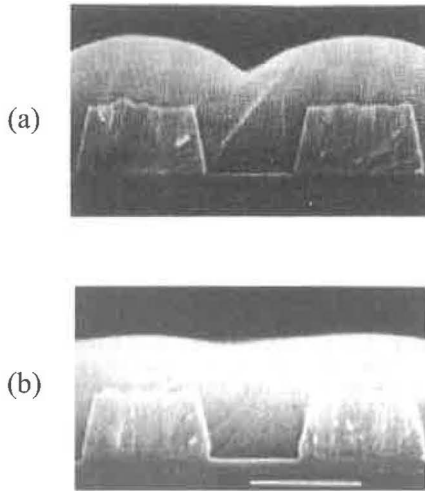
Figure 11. Deposited films (*a*) after deposition and (*b*) after reflow at 900°C. *(Courtesy of Quester Technology.)*

In the deposition of the dielectric films, the previously mentioned "bread-loafing" effect causes closure of the gap at the top thus preventing good gap fill. Initial attempts to overcome this problem entailed partial deposition of the dielectric film, then etching back the upper corners of the film as depicted in Fig. 12.[16] Further film deposition followed with repetition of the etching process if needed. Unfortunately the concept was demonstrated, but much too expensive for use in production. Why not develop an environment where deposition and etching could be sequentially done in the same system? This led to the development of ECR technology for deposition where both deposition and to some extent directed etching could take place.

As illustrated in Fig. 12b, the initial film deposition was conformal with eventual closing at the top of the gap. By switching into a directed etching mode, the top could be etched back at a typical 45° angle. Subsequent deposition filled the gap leaving the structure as shown in the actual structure (Fig. 12a).

(a)   (b)
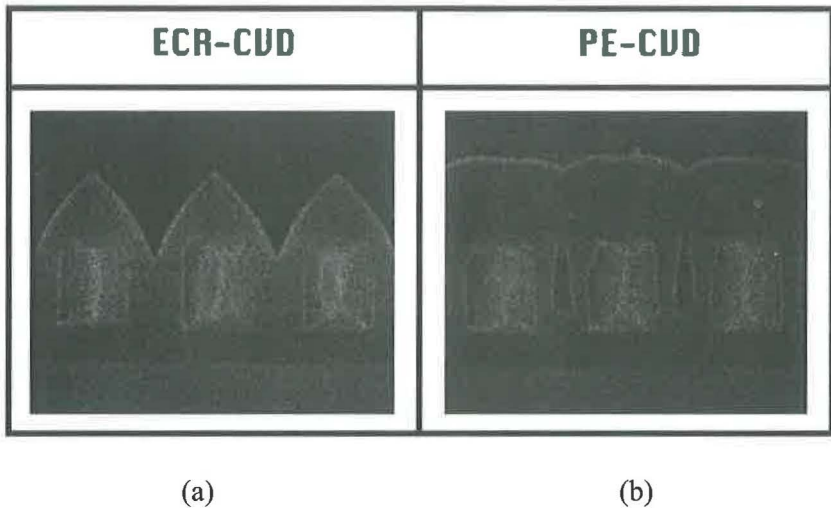
Figure 12. Depiction of gap fill with partial etch back. Notice the voids in (*b*) the PE-CVD photo. (*a*) The ER-CVD films don't have voids between the lines.

Film properties for the ECR deposited films are given in Table 8 with some notation of the deposition conditions for the ECR system shown in Fig. 13. The deposition plasma is generated above the deposition chamber and directed downward by a magnetic field bias. With injection of reactants, deposition takes place on the wafer which is held down with an electrostatic chuck. The plasma densities are high, so the wafer is cooled with helium dispersed underneath the wafer. Considerable effort has gone into making the ECR technology commercially viable, but problems associated with particle generation, uniformity control, and cost have led to alternative high-density plasma sources for CVD applications.

During the development of ECR, other plasma sources were developed to provide high density plasmas suitable for both deposition and etching of dielectric films. The objective was to develop a directed plasma which would direct reactants into the gaps, provide a means for periodically etching the deposition at the top of the gap, and achieve good electrical characteristics. Further improvements lead to the simultaneous ion bombardment (sputtering) of the top of the gap during deposition.

Equipment manufacturers initially extended the sources developed for film deposition into the "high density" plasma regime. This led to plasma damage of active device regions and numerous limitations in film deposition.

One development was the MORI™ source previously supplied by Trikon.[14] A cross section shown in Fig. 14 notes that the plasma is formed above the biasing magnets. The resulting plasma reaching the wafer can be confined to desirable species with high energy ions kept from the wafer. Developments are continuing in the use of these sources for deposition, however, less complex sources are currently being used..

Transformer-coupled plasma sources have been used extensively for etching and are now migrating towards use for deposition.

Inductively coupled sources have also been developed for deposition; they were some of the earliest sources of high density plasma. All these have certain attributes and require careful design of the reactant injection systems within the confines of a high vacuum plasma environment.

Table 8. Film Properties of ECR Deposited Films

Film Parameter	SiO_2	Si_3N_4
Thickness Nonuniformity	<3%	<4%
Deposition Rate (Å/min)	3000 to 4000	200 to 500
Etch Rate	30%	
Net Deposition Rate (Å/min)	2100 to 2800	
Refractive Index	1.46	1.98 to 2.10
Dielectric Constant	4.1	8
Stress (10^9 dynes/cm^2)	2.0 to 2.5	0.6 to 1.4
H Content (at %)	2 to 3	8
RF Power (watts)	400 to 1000	500 to 2000
Deposition Temperature (°C)	300	350
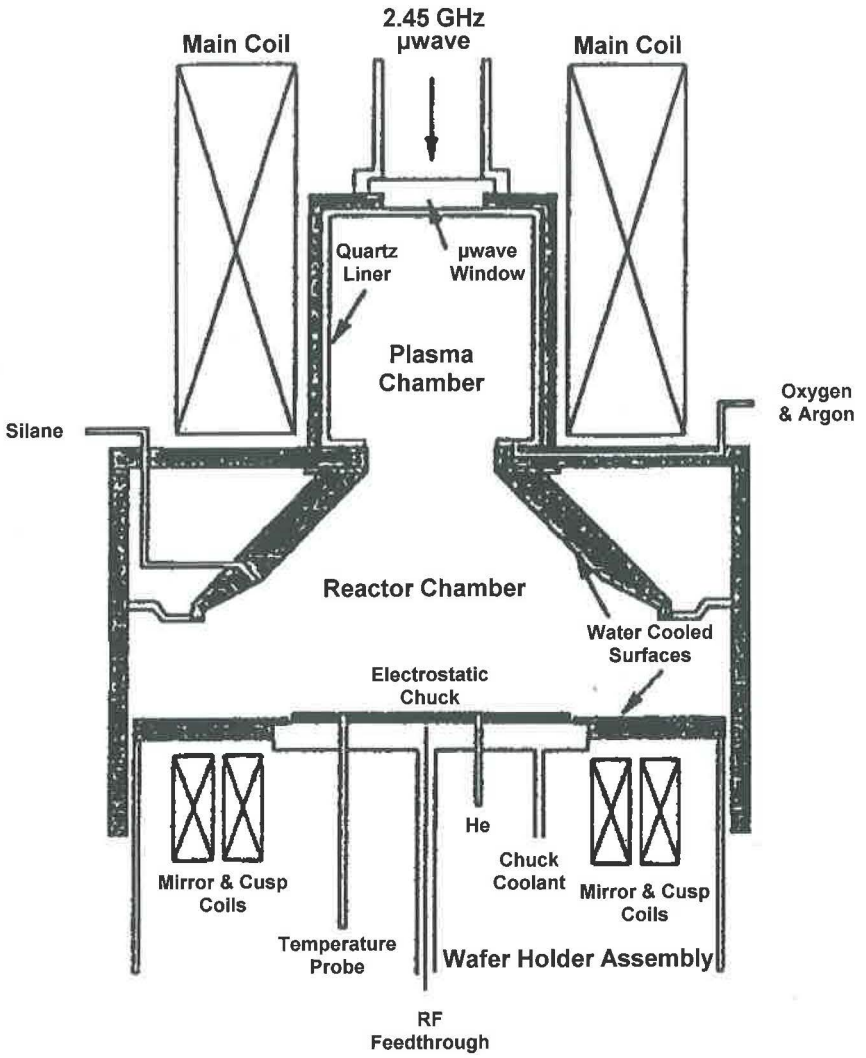
Figure 13. ECR system schematic.
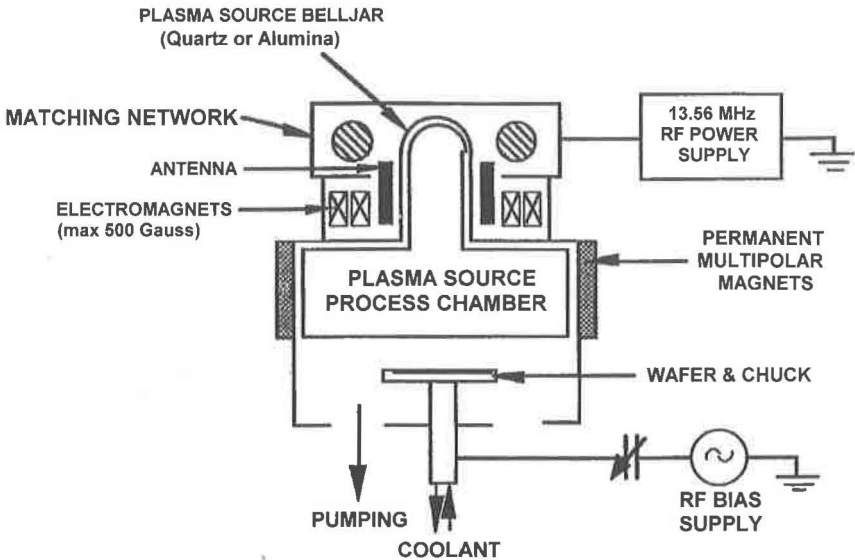
Figure 14. Mori source schematic.

5.1 Trends for CVD of Dielectric Films

For dielectrics used as capacitors in memory cells, the trends are toward use of higher dielectric materials. These consist of Ta_2O_5, Al_2O_3, and, more recently, ZrO_2 and HfO_2, all having the capability for deposition by CVD techniques. The Ta_2O_5 materials have made the most progress in possible use for future memory circuits, however, the higher dielectrics constant BZT has received considerable attention.

The higher dielectric materials utilize various precursors for deposition in reactors similar to those used for TEOS. The listing in Table 9 provides available properties of the films, but all the films still need refinement to grow thin layers which are defect free. Along with deposition, the technologies for etching the films also need development.

For interlevel and intermetal dielectrics, the emphasis is toward excellent gap-fill and planarization capabilities. The current technologies, with some refinement, will provide these capabilities as illustrated in Fig.

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15. The films consist of a PECVD oxide over metal lines at the gap bottom with typical thickness of 1000 to 2000 Å. A TEOS/ozone overlying layer provides the gap-fill. A third layer, typically 1.5 micron thick PECVD TEOS is then subjected to Chemical Mechanical Polishing (CMP) to provide the planarization shown. Work is currently in progress to CMP the TEOS/ozone films directly.

Table 9. Properties of Various Hi-K Dielectrics

Film Type	Thermal SiO_2	Al_2O_3	Ta_2O_5	ZrO_2	HfO_2
Dielectric Constant	3.95	9	26	25	25–40
Bandgap (eV)	8.9	8.7	4.5	7.8	5.7
Barrier Height to Silicon	3.2	2.8	1–1.5	1.4	1.5
Deposition Technique	Thermal Growth	CVD	CVD	CVD	CVD
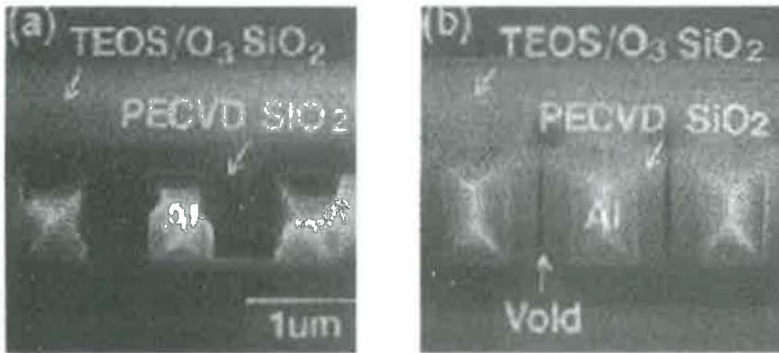
Figure 15. Dual layer film stack employing PECVD and TEOS/O_3 based SiO_2.[19]

Additional progress with plasma deposited films for excellent gap-fill is being made at the same time lowering the dielectric constant. By adding fluorine to the SiO_2 film, the interaction during deposition shows an improvement of the gap fill. This work has also led to lowering the dielectric constant of the deposited films. Dielectric constants in the range of 3.5 to 3.8 have been measured with recently reported film characteristics given in Table 10. Lowering of the dielectric constant is the next direction for the ILD and IMD films. As has been well published, lower dielectric constants enhance circuit performance as will be required for future generation microprocessors and memory circuits.

The most prevalent approach for lower dielectric constant of SiO_2 based films is to add fluorine to the film. Although leading to film instabilities, absorption of moisture, and formation of hydrofluoric acid, the films after annealing can be stabilized. Other approaches include use of boron-doped glasses and inclusion of boron nitride in the films. With all these films, the lower dielectric constant can be achieved, however, the technologies of subsequent processing steps have to be developed.

Extensive work has been performed using organic films for dielectrics with the development of MCM's (Multi Chip Modules) and to some extent with forays toward wafer scale integration. Various polymers are being investigated with parylene being the most developed. Whereas these films were suitable for the larger geometry technology in MCM's, they are a challenge to use for submicron technology. Examples and properties of such films are given in Table 11.

Table 10. Properties of Fluorine Doped SiO_2 Films

Film Type	SiOF	SiOF	a-C:F
Reported in Reference	[22]	[23]	[25]
Dielectric Constant	≈3.5	2.7 to 3.2	2.5 to 2.8
Deposition Technique	Room Temperature Flow CVD	PECVD and HDP CVD	HDP CVD
Source	FTES (fluoro-triethoxysilane)	TEOS	CH_4
F Source	Included	C_2F_6	C_4F_8

To overcome the limitations of spin-on coating of the organic films, CVD methods are being developed.

Various reactors are being used to derive such films using CVD methods, with a typical example shown in Fig. 16. A reactor consisting of a reaction (deposition) chamber has the reactants delivered through two reactant "cracking" chambers. A detailed description is given in Ref. 26 with some results. Still limiting this technology are the problems associated with surface nucleation on the wafer and defect formation by the large molecular structure of the parylene.

Table 11. Properties of Organic Dielectrics

| Film Type	Parylene	BCB	PTFE
Film Parameters			
Dielectric Constant	2.6	2.7	1.9
Deposition Technique	CVD	Spin-on	Spin-on
Reactants	Poly-p-xylylene	Divinyl-benzo siloxane and Bis-cyclo-butene	Polyfluoroteton-ethylene
Temperature Limit °C	300	350	400
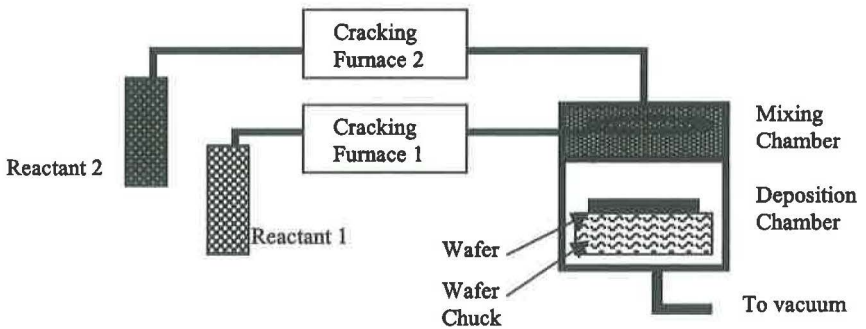
Figure 16. Low-K polymer based CVD reactor schematic.

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6.0   FUTURE DIRECTIONS FOR CVD OF DIELECTRIC FILMS

As we peer into the next centuries' requirements for the films, the challenges for CVD deposition are definitely there. Whereas the focus has been toward production of films suitable for semiconductor devices, the areas of flat panel displays present some formidable challenges. Not only are the deposition areas becoming larger, the perfection requirements for the film are becoming extremely tight. There is much to do to overcome some of the limitations.

With respect to achieving film uniformity and understanding deposition over patterned wafer surfaces, the modeling efforts are giving insight into the reactions that are taking place. Insight into the parameters that affect uniform deposition and its reactions can be derived. However, as surfaces become more demanding, i.e., smaller geometry patterns, further model refinements have to be made.

More difficult is the controllability of particle generation as so many interacting phenomena can result in formation of particles. Various mechanical enhancements to exhaust by-products and unused reactants provide some means of minimizing particles. Through optical observations of reactions plus laser-based particle monitors, particle generation phenomena within reaction zones may be determined. Continued progress in reactor cleaning technology, both the methods and chemistries used, will lead to minimization of particles.

With the need to alter film properties in-situ the deposition reactor, pre- and post-deposition processing will be implemented. Use of electron-beam radiation on SOG films has demonstrated an altered film with more suitable properties.[24] To achieve an in-situ reflow, the BPSG films can be deposited at higher temperatures, currently being performed in Model 9900 systems by LAM Research, Inc.

Continued need for providing tolerable depth-of-focus (DOF) for lithography places emphasis on global planarization of the films. Whereas currently attained through CMP technology, and to some extent by spin-on-glass, it is desirable to find ways for global planarization while depositing the film. Of course, this would lead to a selective deposition as is possible with some metal films. The prospect of a pre-deposition treatment of the wafer surface to achieve selective deposition would be a major breakthrough.

New chemistries are being explored to provide more suitable films within the confines of currently available reactors.[25] An example is the

recently reported use of TMS, within a dual frequency PECVD system, to achieve enhanced film deposition conformity on patterned wafers.

Lower dielectric constant materials, both in the form of organics and inorganics, will be derived from new chemistries. As noted in Table 12, a variety are under development, all focused toward extending current reactor technologies.

7.0   SUMMARY

An overview of CVD technologies for dielectric films has provided some insight on film deposition techniques along with film properties. Detailed descriptions of many factors associated with the depositions are given in the cited references. With the continued importance of these films in semiconductor manufacturing and for flat panel displays, a continued, concerted effort will be made to provide the nearly perfect films required for future technologies. Technological progress in theoretical understanding and practical deposition designs will provide films for 300 mm wafers and large area flat panel displays.

Table 12. Chemistries for Low-K Materials Deposited by CVD

Material	K Value	Glass Transition Temperature, °C	Reference
Fluorinated Silicate Glass (FSG or SiOF)	3.2–3.6	>800	[29]
Methylated Silica from Tetramethyl Silane	2.7	375	[29]
Parylenes (including copolymers)	2.2–2.6	375	[29]
Fluorinated Amorphous Carbon (a-C:F)	2.1–2.5	350	[29]
Poly(p-xylylene)	2.3	450	[30]
Carbon-doped SiO_2	2.6–3.2	500	[31]

REFERENCES

1. Fujino, K., Tokumasu, N., and Maeda, K., Doped Silicon Oxide Deposition by Atmospheric Pressure and Low Temperature Chemical Vapor Deposition Using Tetraethoxysilane and Ozone, *J. Electrochem. Soc.*, 138:2883 (Oct. 1991)

2. Fisher, S., Chino, H., Maeda, K., and Nishimoto, Y., Characterizing B-, P-, and Ge-Doped Silicon Oxide Films for Interlevel Dielectrics, *Solid State Tech.*, p. 55 (Sept. 1993)

3. Korczynski, E. J., and Shih, A. H., Improved Sub-Micron Inter-Metal Dielectric Gap-Filling Using TEOS/Ozone APCVD, *Microelectronics Manufacturing Technology* (Jan. 1992)

4. Ban, V. S., and Gilbert, S. L., *J. Electrochem. Soc.*, 122(10):1382 (1975)

5. Sirtl, E., Hunt, I. P., and Sawyer, D. H., *J. Electrochem. Soc.*, 122:919 (1974)

6. Cobianu, C., and Pavelescu, C., *J. Electrochem Soc.*, 130:1888 (1983)

7. Kim, E. J., and Gill, W. N., *J. Crystal Growth*, 140:315–326 (1994)

8. Thakur, R., and Iyer, R., et al., *VMIC*, p. 117 (1994)

9. Tokumasu, N., and Maeda, K., et al., VMIC, p. 123 (1994)

10. Schwartz, G., *VMIC Seminar*, p. 107 (1992)

11. Smith, D. L., Alimonda, A. S., et al., *Mat. Res. Soc. Symp. Proc.*, 204:475 (1991)

12. Fujino, K., Nishimoto, Y., et al., *J. Electrochem. Soc.*, 550:1382 (1991), and private communications.

13. Kubo, A., Hirose, K., et al., *VMIC*, p. 94 (1994)

14. Singer, P., Meeting Oxide, Poly and Metal Etch Requirements, *Semiconductor Int'l.*, p. 50 (April 1993)

15. Takasaki, K., et al., *Electrochem. Soc. Ext. Abs.*, 80-2:260 (1980)

16. Ishikawa, H., and Murao, Y., *VLSI Multilevel Interconnection Conference*, p. 67, VMIC (1994)

17. Verma, A., Guo, T., et al., Process Integration of Low Dielectric Constant Fluorine Doped PECVD Silicon Oxide Thin Films With Interconnect Metallization, *VMIC Conference*, p. 141 (1995)

18. Kim, K., Park, S., and Lee, G. S., Improvement of Moisture Resistance in Fluorinated Silicon Oxide Films by Adding Ar., *J. Elec. Chem. Soc.*, 146:3799 (1999)

19. Kubo, A., et al., *VLSI Multilevel Interconnection Conference*, p. 94, VMIC (1994)

20. Banerjee, I., and Harket, M., et al., Characterization of Chemical Vapor Deposited Amorphous Fluorocarbons for Low Dielectric Constant Interlayer Dielectrics, *J. Elec. Chem. Soc.*, 146:2219 (1999)

21. Han, S. S., Kim, H. R., and Bae, B. S., Deposition of Fluorinated Amorphous Carbon Tin Films as a Low Dielectric Constant Material, *J. Elec. Chem. Soc.*, 146:3383 (1999)

22. Lim, S. W., Shimogaki, Y., et al., *J. Elec. Chem. Soc.*, 146:4196 (1999)

23. Robles, S., Ping, X., et al., Ultra Low K Dielectric PECVD α–FC Films for Damascene Applications, *Advanced Metallization and Interconnect Systems for ULSI Applications in 1997*, p. 373, Mat. Res. Soc. (1998)

24. Yang, J. J., Wang, S. Q., et al., Integration of Spin-On Low K Dielectrics Using E-Beam Curing for ULSI Mutilevel Interconnects, *Advanced Metallization and Interconnect Systems for ULSI Applications in 1997*, p. 359, Mat. Res. Soc. (1998)

25. Suzuki, S., Tokumasu, N., and Maeda, K., High Quality SiO_2 Films Prepared by Dual Frequency Exciting PECVD with New Organic Si Source, *VLSI Symp.*, Japan (1998)

26. Wary, J., Olson, R., and Beach, W., Polymer Developed to be Interlayer Dielectric, *Semiconductor Int'l.*, p. 211 (June 1996)

27. Kwon, K. W., et al., *Mater. Res. Soc. Symp. Proc.*, 284:505 (1993)

28. Singer, P., Low K Dielectrics: The Search Continues, *Semiconductor Int'l.*, 88 (May 1999)

29. Ryan, T., and Fox, R. J., Low-K Dielectric Materials, *Future Fab International*, Edition 8

30. Pye, T and Rose, P., Low-Dielectric Constant Materials for Back-end-of-line Applications, *Semiconductor Fabtech*, 8th Edition, p. 203

31. Sermon, et al., Low-K Dielectrics for Future IC Fabrication, *Semiconductor Fabtech*, 11th Edition, p. 245