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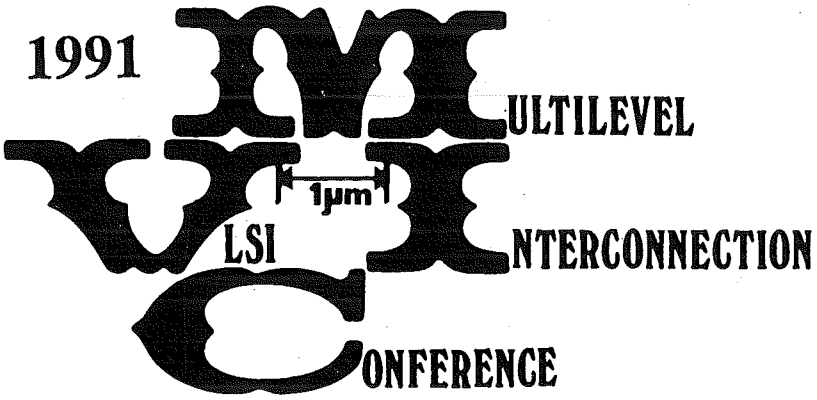

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A FOUR-LEVEL-METAL FULLY PLANARIZED INTERCONNECT TECHNOLOGY FOR DENSE HIGH PERFORMANCE LOGIC AND SRAM APPLICATIONS

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ABSTRACT

This paper describes a four-level-metal (4LM) interconnect technology used to wire high-density, high-performance logic and SRAM chip designs. Process features include oxide planarization under all metal levels, tungsten studs for contacts and interlevel vias, layered titanium and aluminum-0.5% copper metal lines patterned by reactive ion etch (RIE), and fusible metal links for redundancy applications. Functional 300K circuit ASIC logic test sites (4LM) and 256K SRAMs (3LM) have been fabricated in both 125-mm and 200-mm wafer sizes. Process details are described along with the results of standard electrical tests and reliability stresses.

INTRODUCTION

The continuing drive to achieve greater density and performance in CMOS logic and SRAM applications is placing ever-increasing demands on multilevel interconnection technology. Indeed, present ASIC offerings with high circuit counts and large chip sizes are usually wiring-limited; it is not unusual to have less than 60% of the available circuits wired on these chips. Current-generation designs require up to five levels of metal to satisfy all of the wiring needs. Maximum layout efficiency requires the ability to make vertical connections between any of these metal levels in a minimum space. The interconnect technology chosen to accomplish this task must also meet the performance and reliability targets of the designs and be manufacturable.

The interconnect process described in this paper was developed and piloted in a 125-mm logic manufacturing line and has been installed in a 200-mm manufacturing line which it shares with 4-Mbit DRAM production at IBM's Essex Junction, Vermont, facility. In fact, this logic interconnect process was developed using the DRAM process as a base [1], and then modified in several areas to meet the needs of logic. Various process modules from IBM's East Fishkill [2], Yorktown [3] and Essex Junction development areas are included in the final integrated process.

TECHNOLOGY FEATURES

This advanced interconnect technology provides logic and SRAM designers with the wireability features required to manufacture high-density, high-performance logic and SRAM products. The wiring features include a local interconnect level and up to four levels of reactive-ion-etched (RIE) layered titanium and aluminum-0.5% copper wiring; each metal level is fabricated on top of a planarized insulator.

The metal pitch and thickness for each of the interconnect levels are listed in Table 1.

Vertical tungsten stud vias are used to interconnect the wiring levels and stacked contacts and vias are allowed in the various product designs. As a further enhancement to wireability, metal borders around studs are not required for either the topside or underlying metal. Laser-blown metal fuses are also included in this technology and are primarily used for redundancy in stand-alone and imbedded SRAMs. Finally, in response to the I/O requirements of VLSI logic, an area array of up to 1600 lead/tin C4 terminals per chip is offered.

PROCESS DESCRIPTION

The basic process flow for each of the metal, insulator, and stud levels is repetitive and illustrated in Figure 1. The Al-Cu based film is sputter-deposited onto a planarized substrate, photo-patterned and then defined by RIE. A PECVD oxide is subsequently deposited over the underlying metal pattern. A deposition-etch-deposition sequence is used to provide adequate insulator-fill between minimum-spaced metal lines. The oxide is then planarized using a chemical-mechanical polish technique (CMP). Next, via-photo and RIE are employed to form nearly vertical vias down to the underlying metal level. A sputtered Ti/TiN liner and blanket CVD tungsten deposition processes are used to fill the vias (Figure 1d). A second CMP process then removes the tungsten and liner material from the surface, leaving it in the vias (Figure 1e).

Table 1. Interconnect thickness and wiring pitch.

Metal Level	Thickness (μm)	Wired Pitch (μm)
M1	0.85	2.0
M2	1.05	2.4
M3	1.05	2.4
M4	2.0	4.8

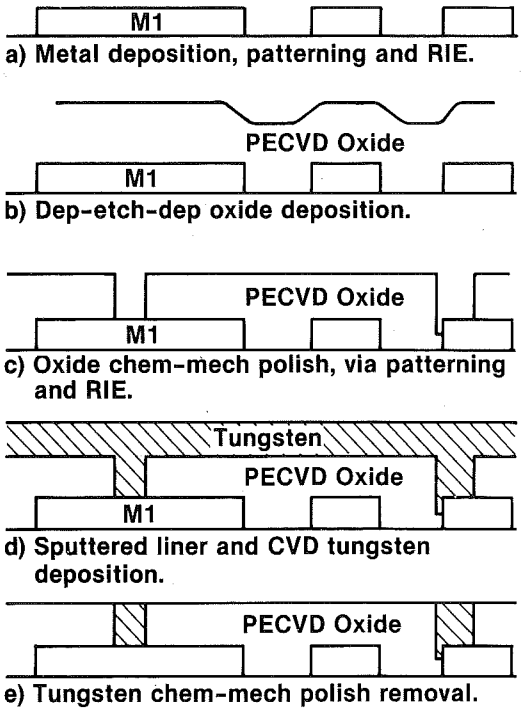

Figure 1. Process flow for metal, insulator and stud formation.

A cross section of the final integrated four-level-metal logic interconnect process is illustrated in Figure 2. As indicated, the tungsten studs are allowed to extend partially down the side of the metal wiring levels. This is a consequence of allowing designs without metal-bordering of vias. The final passivation is a layered structure of oxide, nitride and polyimide. An SEM cross section of a four-level-metal test structure fabricated with the processes described above is shown in Figure 3.

The use of a similar process sequence under the first level of metal, as shown in Figure 2, avoids reliance on reflow of highly doped BPSG glass layers for pre-M1 planarization. The result is a process that yields superior planarity, when compared to reflow, and avoids the degradation of device properties and sheet resistance of salicided materials that accompany high-temperature processes.

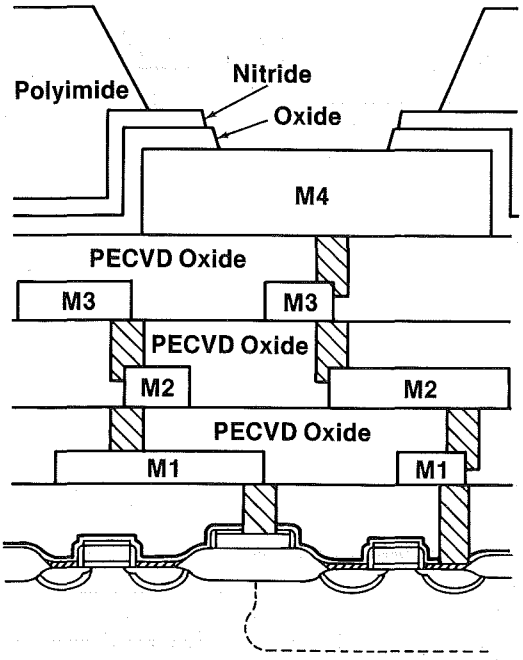

Figure 2. Cross section of four-level-metal structure.

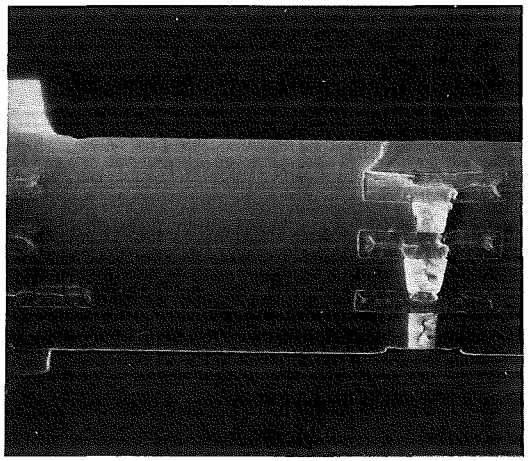

Figure 3. SEM cross section of four-level-metal structure.

The use of redundant word and bit lines to repair defects in DRAMs and SRAMs is well known. Typically, the address of the redundant feature is incorporated into the operation of the chip by selectively blowing a series of fusible links. Fuses are integrated into this interconnect technology as part of the next to last level of metal as depicted in Figure 4. Any given fuse can be blown by focusing sufficient laser energy onto the appropriate metal line. As shown in the SEM cross section in Figure 5, a portion of the metal line and overlying insulator is removed during this operation. Unblown fuses remain passivated with oxide. This technique has been demonstrated by successfully fixing partially good 256K SRAM chips. In addition, blown metal fuses have been subjected to

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