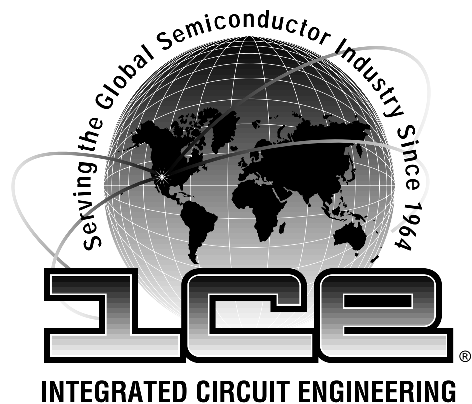
Construction Analysis

Samsung KM44C4000J-7
16 Megabit DRAM

Report Number: SCA 9311-300I



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INTRODUCTION

This report describes a construction analysis of the Samsung KM44C4000J-7 16-megabit CMOS Dynamic RAM. Four samples molded in 24-pin plastic SOJ packages and date coded 9313 were supplied for the analysis. Analysis of the packaging and assembly is included.

MAJOR FINDINGS

Questionable Items:[1]

- Silicon nodules occupied up to 75 percent[2] of metal 2 line widths (Figure 16).

Special Features:

- Twin-well process with sub-micron geometries (0.3 micron poly 1 and 0.5 micron metal 1).
- Two levels of metal, four levels of poly.
- Metal 1 contacts were completely filled with aluminum (aluminum reflow).

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2] *The seriousness depends on design margins.*

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TECHNOLOGY DESCRIPTION

Assembly:

- 24-pin (28 pin format) plastic small-outline J-lead package (SOJ).
- Iron-nickel (FeNi) leadframe.
- External leads were coated with tin-lead (SnPb) solder.
- Internal leadframe plating consisted of spot-plated silver (Ag) over a thin copper (Cu) flash. No plating was present on top of the header.
- Lead-locking provisions (anchors) were present at all pins.
- A dimpled header was employed.
- All pins were connected.
- Die attach was by silver (Ag)-epoxy.
- Dicing was by the sawn method.
- Wirebonding was by the thermosonic ball bond method using 1.3 mil O.D. gold wire.

Die Process and Design:

- Fabrication process: Selective oxidation CMOS process with twin wells in a P(?) substrate.
- Die coat: A patterned (to clear bond pads) polyimide die coat was present to protect against alpha particle-induced leakage.
- Overlay passivation: A layer of silicon-nitride over two layers of silicon-dioxide. The second layer of silicon-dioxide was multilayered.

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<u>TECHNOLOGY DESCRIPTION</u> (continued)

- Metallization: Two levels of metal conductors were used. Metal 2 consisted of aluminum only. Metal 1 consisted of aluminum with a titanium-nitride cap and barrier. Both metal levels were defined using a dry-etch technique.

- Interlevel dielectric: Three layers of silicon-dioxide plus a filler glass (SOG) between interlevel glasses 2 and 3.

- Intermediate glass: Two layers of boron- and phosphorus-doped glass in addition to the various densified oxides. Intermediate glass layers (between poly 3 and polycide, and polycide and metal 1) had been reflowed prior to deposition of subsequent layers and contact cut definition.

- Polysilicon: Four levels of dry-etched polysilicon were used. Poly 4 employed a tungsten silicide (polycide) and was used for the bit lines in the cell array and interconnect in the decode areas. Poly 3 (sheet) was used for the common passive capacitor plate and poly 2 was used for the individual active capacitor plates in the cell array. Poly 1 was used for all the gates on the die.

- Diffusions: Standard N+ and P+ implanted source/drain diffusions formed N- and P-channel transistors. Transistors were formed using an LDD process with oxide sidewall spacers.

- Wells: Twin wells in an P substrate.

- Memory cells: The memory cell used an NMOS DRAM cell design consisting of a select gate and a stacked capacitor. Polycide formed the bit lines. Poly 1 formed the word lines and was "piggybacked" by metal 1. Stacked capacitors were formed by poly 2 pads covered by a poly 3 sheet separated by a thin oxide/nitride dielectric.

- Fuses: Redundancy was implemented using polycide fuses. Laser blown fuses were noted on all samples. Oxide cuts were present above fuse locations and were then covered by the overlay passivation. No separate guardbands were found around the fuses.

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