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365/225.7

## United States Patent [19]

#### [54] REDUCED PITCH LASER REDUNDANCY FUSE BANK STRUCTURE

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- [73] Assignee: Micron Technology, Inc., Boise, Id.
- The term of this patent shall not extend [\*] Notice: beyond the expiration date of Pat. No. 5,636,172.
- [21] Appl. No.: 831,389
- [22] Filed: Apr. 1, 1997

#### **Related U.S. Application Data**

- [62] Division of Ser. No. 577,468, Dec. 22, 1995, Pat. No. 5,636,172.
- [51] Int. Cl.<sup>6</sup> ..... H01L 27/10; H01L 29/00
- [52] U.S. Cl. ...... 257/529; 257/209; 365/225.7
- [58] Field of Search ...... 257/209, 529;

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**Patent Number:** 

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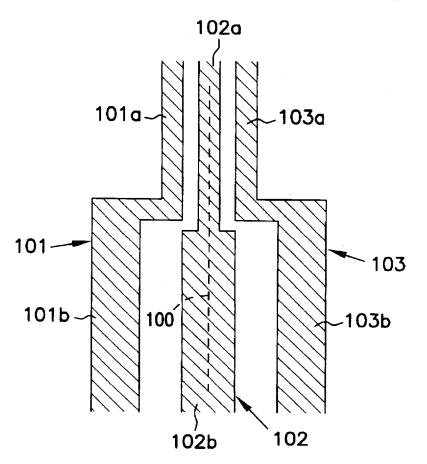
Primary Examiner-Valencia Martin Wallace Attorney, Agent, or Firm-Schwegman, Lundberg,

Woessner & Kluth, P.A.

#### ABSTRACT

A configuration for a laser fuse bank is disclosed wherein the available space is more efficiently used. Fuses of graduated width and variable configuration are placed so as to minimize the average distance between fuses and maximize fuse density. Alternatively, a common source is added to a standard laser fuse structure such that it intersects the fuses and the number of available fuses is doubled.

#### 11 Claims, 3 Drawing Sheets

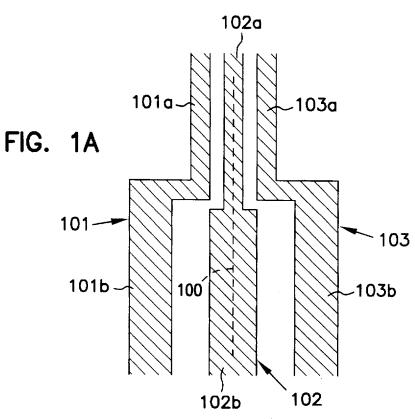


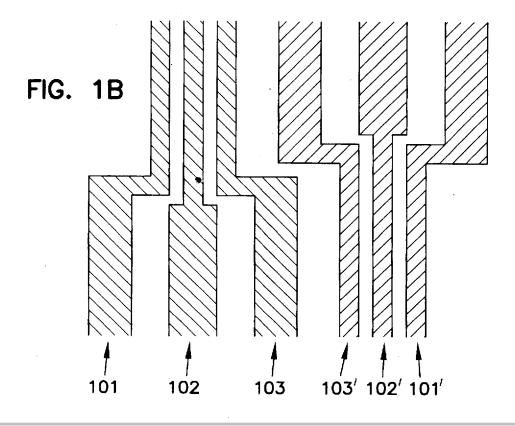
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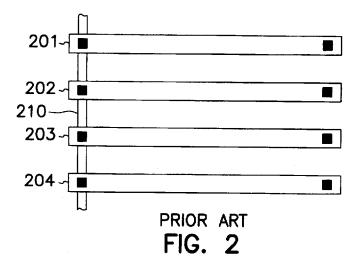
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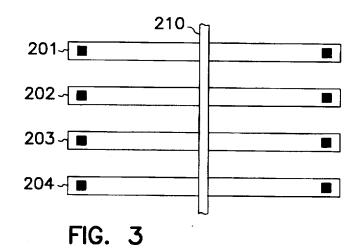


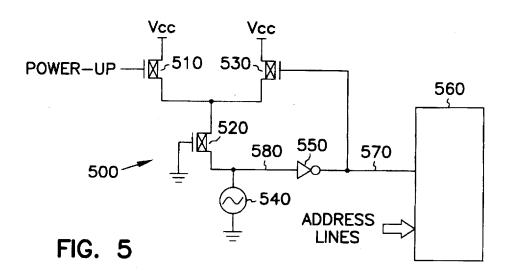


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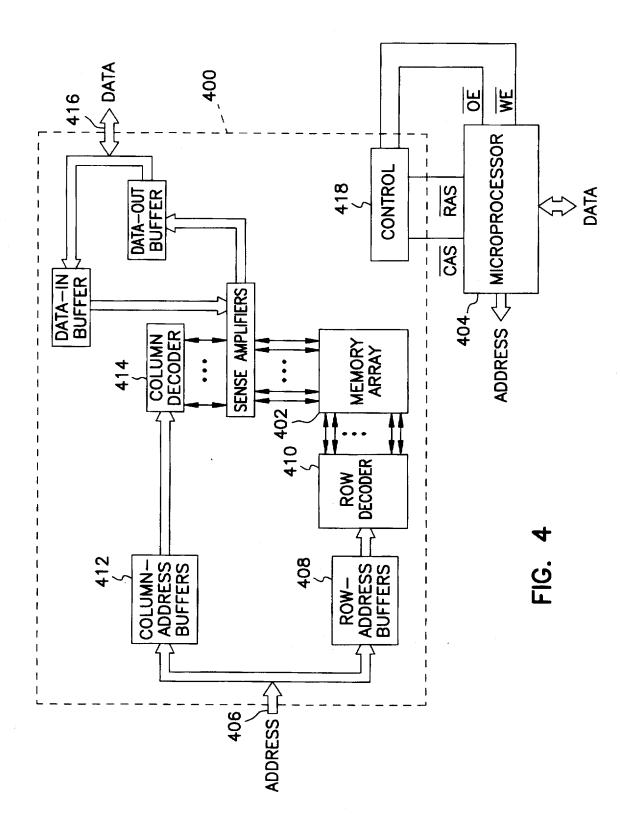


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#### REDUCED PITCH LASER REDUNDANCY FUSE BANK STRUCTURE

This application is a divisional of U.S. patent application Ser. No. 08/577,468, filed Dec. 22, 1995. U.S. Pat. No. 5 5,636,172.

#### TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to integrated circuits and in particular to a fuse bank structure used in <sup>10</sup> integrated circuits.

#### BACKGROUND OF THE INVENTION

An integrated circuit is a complete electronic circuit, 15 containing transistors, diodes, resistors, and capacitors, along with their interconnecting electrical conductors, contained entirely within a single chip of silicon. Integrated circuits continue to decrease in size, and the circuits they contain continue to increase in complexity. This increases 20 the opportunity for defective chips resulting from a failed element or a defective conductor. The complexity of these devices and the need to interconnect the circuits create very narrow performance tolerances. One way these needs have been met is to manufacture fuses into the device. Fuses can 25 be opened to isolate defective areas and allow the rest of the circuit to be used. Fuses can also be used to trim a circuit, enable a particular mode, or enable or disable different segments of the circuit. By using fuses integrated circuit manufacturers are able to reduce the amount of semicon- 30 ductor scrap. The continuous drive to reduce the overall size of integrated circuits creates a need to design fuses and other elements of integrated circuits in such a way as to minimize the space they require.

Another way to reduce semiconductor scrap is to provide 35 redundant elements on integrated circuits. If a primary element is defective a redundant element can be substituted for that defective element. One example of an integrated circuit device which uses redundant elements is electronic memory. Typical memory circuits comprise millions of 40 equivalent memory cells arranged in addressable rows and columns. By providing redundant elements, defective memory cells can be replaced. Because the individual primary memory cells of a memory are separately addressable, replacing a defective cell typically comprises opening fuse-45 type circuits to 'program' a redundant cell to respond to the address of the defective primary cell. This process is very effective for permanently replacing defective primary memory cells.

Circuit designers continuously strive to achieve higher 50 population capacities without a corresponding increase in physical size. Reducing the size of individual elements in integrated circuits is one way in which available die real estate is maximized. For example, as memory density increases the number of fuses needed for redundancy in a 55 given memory device also increases. A 256M DRAM is expected to have more than 10,000 laser fuses. Most components of the memory devices can be scaled to meet the space restrictions resulting from the higher densities. However, laser fuses used to implement redundancy can not 60 be scaled due to mechanical restrictions related to current laser technology. Fuse width must be kept large enough to cover the laser spot so that the fuse can absorb a large quantity of heat. In addition, the fuse-to-fuse space must be kept large enough to allow for mechanical laser alignment 65 tolerances and to prevent unintentional programming of a fuse adjacent to an exploding fuse. These laser alignment

tolerances, as well as the requirements for a large passivation opening, limit the length of the fuse. Currently the constraints dictated by the laser repair requirements limit the fuse pitch to about 3 microns. The demand for increasing numbers of fuses combined with the fixed pitch limitation create a need for improvements in the laser fuses.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a design which provides an increased density of laser fuses.

#### SUMMARY OF THE INVENTION

The above mentioned problems with increasing the number of fuses in a memory device are addressed by the present invention which will be understood bad reading and studying the following specification. A design embodying a more efficient fuse shape is described which allows placement of more fuses in the same amount of physical space.

According to one embodiment of the present invention, an integrated circuit laser fuse system is provided, comprising a plurality of laser fuse banks. Each laser fuse bank comprises three fuses. One of the fuses is a center fuse having a narrow end, a wide end, and a common centerline. Another of the fuses is a first outer fuse having a narrow end and a wide end, located adjacent to the center fuse such that the narrow end of the first outer fuse is adjacent to the narrowend of the center fuse and the wide end of the first outer fuse is adjacent to the wide end of the center fuse, the wide end of the first outer fuse is laterally offset from the narrow end of the first outer fuse. Another fuse of the fuse bank is a second outer fuse having a narrow end and a wide end, located adjacent to the center fuse and on the side of the center fuse opposite the first outer fuse such that the narrow end of the second outer fuse is adjacent to the narrow end of the center fuse and the wide end of the second outer fuse is adjacent to the wide end of the center fuse, and the wide end of the second outer fuse is laterally offset from the narrow end of the second outer fuse.

In one embodiment of the present invention the wide end of the first outer fuse is laterally offset from its narrow end in an outwardly direction away from the center fuse and the wide end of the second outer fuse is laterally offset from its narrow end in an outwardly direction away from the center fuse. In another embodiment the plurality of laser fuse banks comprise a first laser fuse bank and a second laser fuse bank positioned such that the second laser fuse bank is adjacent to the first laser fuse bank, and the second laser fuse bank is rotated one hundred eighty (180) degrees from the first laser fuse banks are polysilicon fabricated on an integrated circuit.

According to another embodiment of the present invention the plurality of laser fuse banks are fabricated in a dynamic random access memory (DRAM). The DRAM comprises, in addition to the laser fuse banks, a plurality of primary memory cells and a plurality of redundant memory cells. The DRAM further includes a redundant enable circuit comprising a latch circuit coupled to one of the fuses of the plurality of laser fuse banks and a comparator circuit connected to the latch circuit and a plurality of external address inputs.

Yet another embodiment of the invention is an integrated circuit memory comprising an array of primary memory cells arranged in rows and columns, a plurality of redundant memory cells, and a plurality of laser fuse banks.

In yet another embodiment of the present invention, an integrated laser fuse system is provided, comprising a plu-

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