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Yoo et al.

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[54] **PROTECTIVE FILM FOR FUSE WINDOW PASSIVATION FOR SEMICONDUCTOR INTEGRATED CIRCUIT APPLICATIONS**

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[21] Appl. No.: **684,162**

[22] Filed: **Jul. 19, 1996**

Related U.S. Application Data

[62] Division of Ser. No. 328,587, Oct. 24, 1994, Pat. No. 5,578,517.

[51] **Int. Cl.**^{6} **H01L 27/02**

[52] **U.S. Cl.** **257/529**; 257/640; 257/665

[58] **Field of Search** 257/529, 665, 257/640, 641

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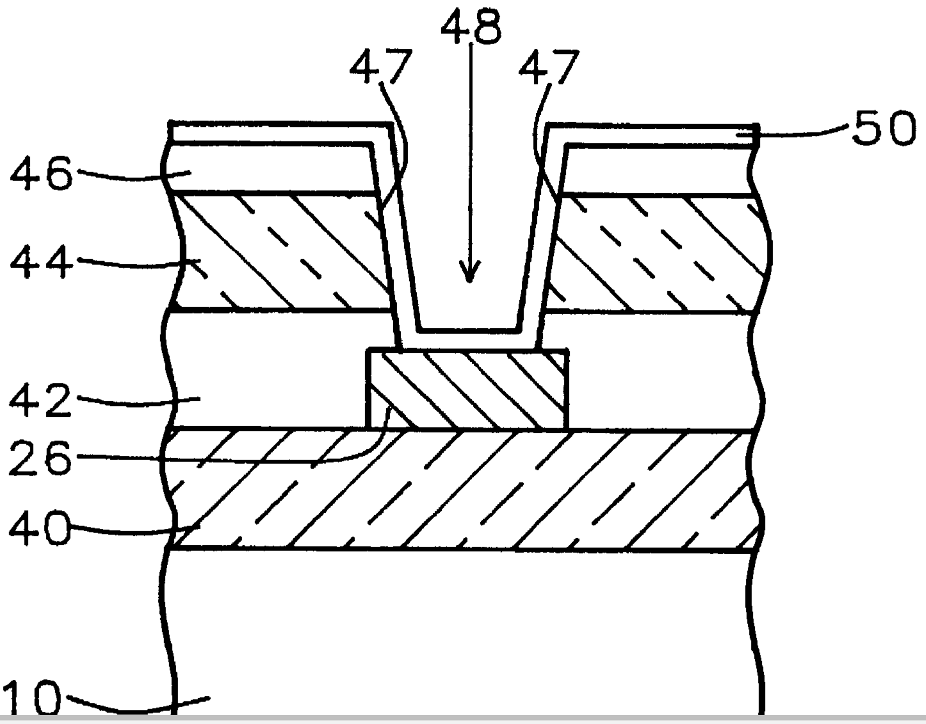
[57] **ABSTRACT**

An integrated circuit includes a conductive fusible link that may be blown by heating with laser irradiation, The integrate circuit comprises a silicon substrate; a first insulating layer; a fusible link on the first layer; a second insulating layer overlying the first layer and the fusible link; an opening through the second layer exposing the fuse; and a protective layer over the surfaces of the opening. A laser beam is irradiated through the opening and the protective layer to melt the fusible link. The protective layer is highly transparent to a laser beam and does not interfere with the laser melting (trimming) operation. Moreover, the protective layer prevents contaminates from diffusing in through the opening to harm adjacent semiconductor devices.

18 Claims, 3 Drawing Sheets



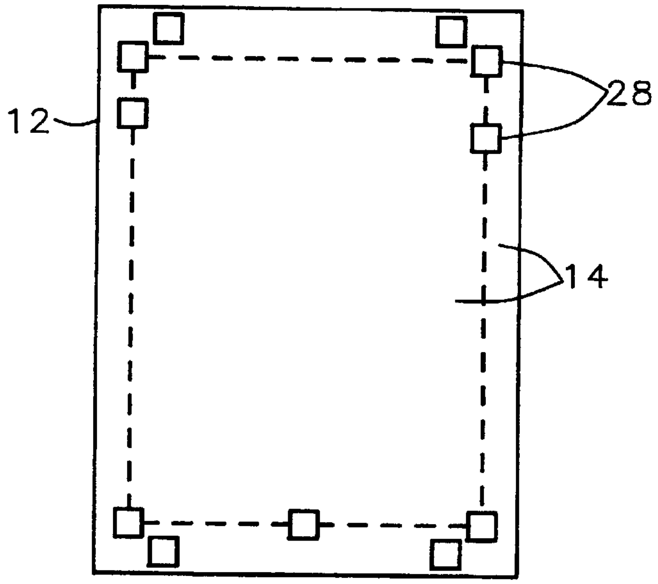


FIG. 1

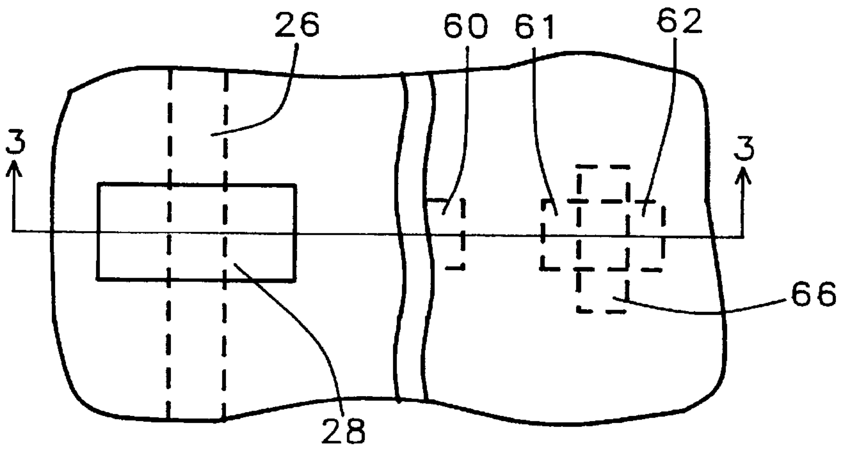


FIG. 2 – Prior Art

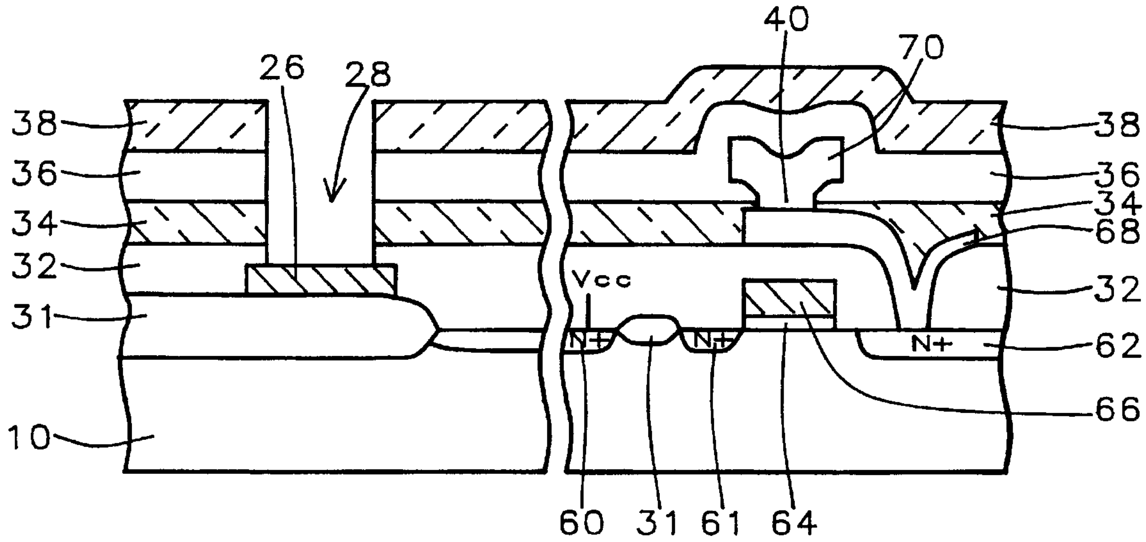


FIG. 3 – Prior Art

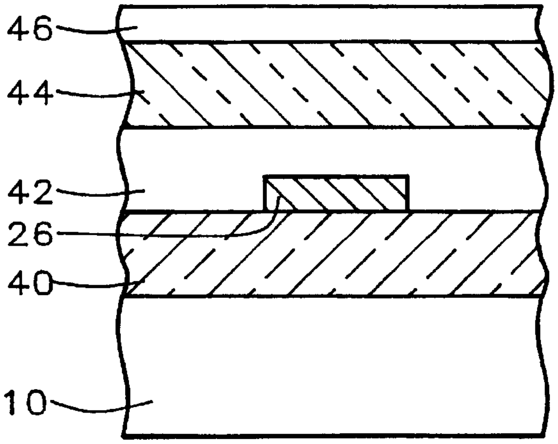


FIG. 4

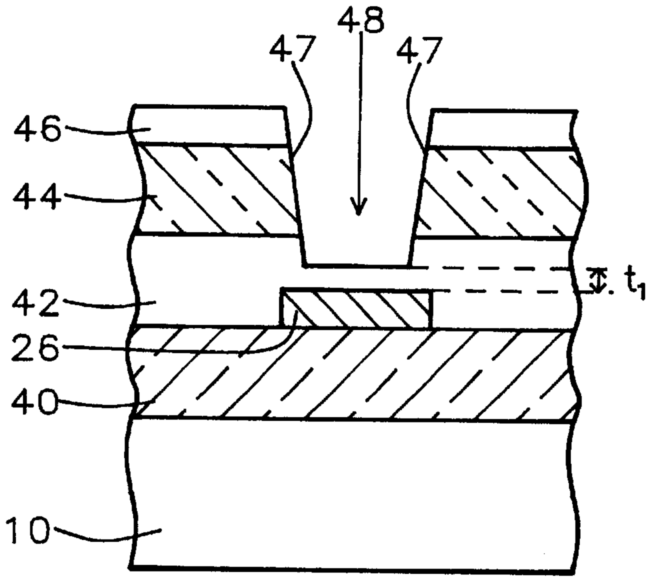


FIG. 5

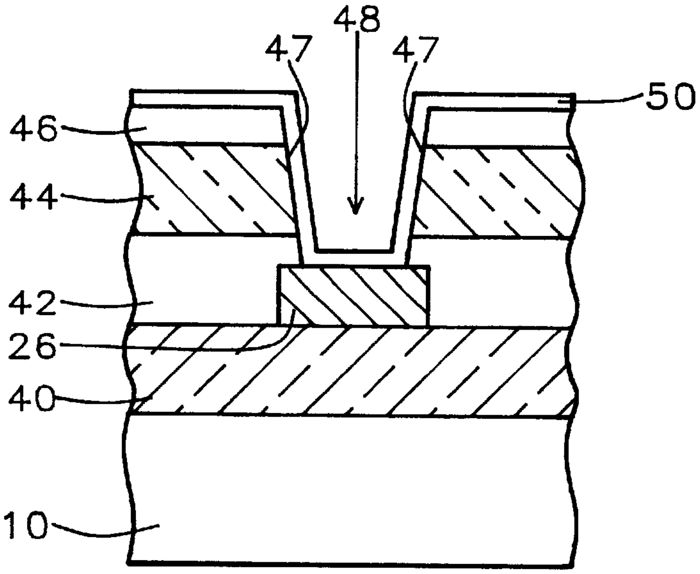


FIG. 6

PROTECTIVE FILM FOR FUSE WINDOW PASSIVATION FOR SEMICONDUCTOR INTEGRATED CIRCUIT APPLICATIONS

This application is a divisional of Ser. No. 08/328,587 filed Oct. 24, 1994, now U.S. Pat. No. 5,578,517.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to integrated circuits and semiconductor devices. It relates particularly to a structure and method for producing integrated circuits having an improved contamination passivation film for surface features, such as fusible links and photo alignments marks.

2. Description of the Prior Art

Fusible conductive links (fuses) are often used in rewiring electrical circuits to replace defective devices with redundant devices. These circuits are rewired by rendering the fuses non-conductive (i.e., blown) by applying laser energy to the fuse with a laser trimming machine.

In dynamic or static memory chips, defective memory cells may be replaced by blowing the fuses associated with the defective cells, and activating a spare row or column of cells. This circuit rewiring using fusible links considerably enhances yields and reduces the production costs.

Logic circuits may also be repaired or reconfigured by blowing fuses. For example, it is common to initially fabricate a generic logic chip having a large number of interconnected logic gates. Then in a final processing step, the chip is customized to perform a desired logic function by disconnecting the unnecessary logic elements by blowing the fuses that connect them to the desired circuitry. Still other applications of laser-blown fuses are possible.

Semiconductor chips often have openings through protective insulating layers over fusible link regions to allow a laser to irradiate the fuse. But these openings frequently lowers chip yields and reliability by allowing contamination to penetrate from the openings to the device regions.

FIG. **1** shows a top plan view of a semiconductor chip **12** with openings **28** over fusible links surrounded by active device areas **14**. A conventional fusible link (i.e., fuse) **26**, a fusible link opening **28** and an adjacent device region **60**, **61**, **62**, **66**, is shown in top plan view FIG. **2**. Referring to FIG. **3**, a cross-sectional view of the same link and device regions in FIG. **2** taken along horizontal axis labeled **3** is shown.

An important challenge is to improve the reliability of the semiconductor devices surrounding fusible links, especially when a large number of the fusible link openings **28** are on a chip **12**. A window opening **28** is normally formed through the insulating layers over a fuse **26** so that a laser beam can be used to irradiate the fuse, thereby blowing it. A problem with openings **28** over a fusible link regions is that moisture and other contaminates can diffuse from the openings, through the insulating layers, into the semiconductor devices thus reducing circuit reliability and yields.

As shown in FIG. **3**, fuse **26** is normally formed over thick field oxide regions **31** in a semiconductor substrate **10**. Fuse **26** is formed over the field oxide regions **31** to prevent shorting of the fuse **26** to the substrate **10**. Fuse **26** can be formed of a metal, such as aluminum, platinum silicide, titanium tungsten, polysilicon, or a polycide, such as tita- (BPSG), spin on glass, silicon oxide and silicon nitride respectively. Opening **28** is formed over the fuse **26** area through the insulating layers **32**, **34**, **36**, **38**. Opening **28** can have a width of 5 microns and a length of 5 microns. An adjacent semiconductor device is shown with buried N+ regions **60**, **61**, **62**, gate oxide **64**, gate **66**, via **40** and metal layers **68**, **70**.

A laser is used to blow the fuses **26**. The laser is focused through the fuse opening **28** and irradiates the fuse **26**. It is conventional to have an opening **28** over the fuse **26** in the area where the fuse **26** will be broken so that the laser heating will be more effective. Because the passivation layers overlying a fuse **26** would reduce the laser energy striking the fuse, the passivation layers are etched away so that the fuse **26** is exposed or, in an alternative, only single thin insulating layer or a portion of a thin insulating layer covers the fuse.

The fuse **26** absorbs the heat from the laser irradiation and the fuse melts. In this operation, sometimes called laser trimming, the rapid temperature rise of the upper portion of the fuse **26** causes an increase in pressure. This pressure cause any overlying film **32** to be "blown off" and the melted polysilicon fuse is removed by evaporation. Laser trimming requires that only a very thin insulating layer cover the fuse because the laser must be able to penetrate the layer and melt the fuse. The portion of the fuse **26** and thin insulating layer **32** over the fuse which is melted away or "blown" must not deposit on or interfere with near-by devices. In the example shown in FIG. **3**, an opening **28** is formed through four layers: Silicon nitride **38**, silicon oxide **36**, spin on glass **34** and borophosphosilicate glass (BPSG) layer **32**.

A major problem with a window opening in the passivation layers is that moisture and contamination can enter through the exposed passivation layers and diffuse to the semiconductor devices. The diffused moisture and contaminates can decrease device reliability and yields. Moreover, moisture is present in the air and sodium (Na+ ions) are plentiful in the environment.

As shown in FIG. **3**, moisture and other contaminates can enter through the window **28**, diffuse into spin on glass layer **34** and diffuse to the adjacent semiconductor devices **31**, **40**, **64**. Water will attack the metal interconnects **70**, and sodium and other contaminates can harm MOS devices **31**, **64**.

First, water can attack the metal interconnects **70**, with the following reaction:

$$3\ H_2O + Al \rightarrow Al(OH)_3 + 3/2\ H_2$$

The formation of $Al(OH)3$ causes the resistance of metal interconnects **70** to increase and finally causes circuit failure.

Second, contamination can harm MOS devices. FIG. **3** shows an opening **28**, buried N+ regions **60**, **61**, **62**, field oxide **31**, gate oxide **64**, polysilicon gate **66**, and metal layers **68**, **70**. Mobile ions, such as sodium ions, can diffuse through inter-metal dielectric layer **34**, and through the insulating layer **34** into the field oxide layer **31**. Mobile ions in the field oxide layer **31** can cause field inversion which allows an undesired leakage current between adjacent buried N+ (or P+) regions **60**, **61** resulting in circuit failure. Also, mobile ions in the gate oxide **64** will cause a transistor threshold shift whereby the circuit fails.

The following three U.S. patents show fusible link structures, but do not adequately solve the problem of contamination diffusing through the window opening to adjacent devices and not interfering with the laser trimming

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