

United States Patent [19]

Ting

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Apr. 5, 1994

[54]	PROCESS FOR FABRICATING SEALED SEMICONDUCTOR CHIP USING SILICON NITRIDE PASSIVATION FILM	
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[21] Appl. No.: 8,469

[22] Filed: Jan. 25, 1993

[51] Int. Cl. H01L 21/80 [52] U.S. Cl. 437/227; 156/648;

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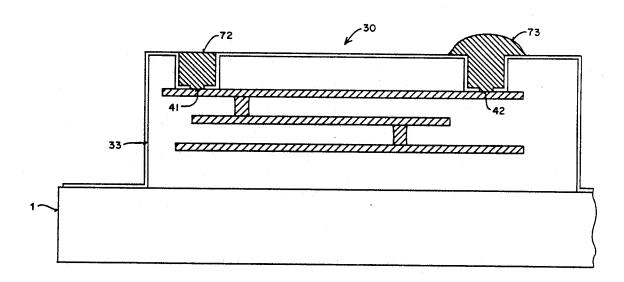
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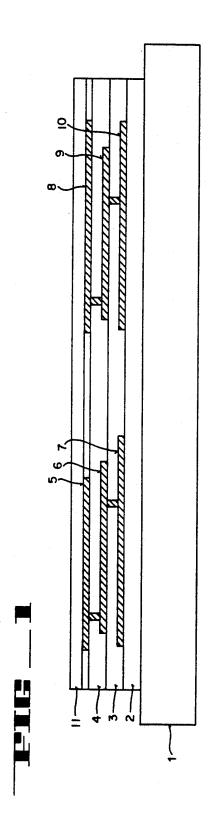
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Zafman

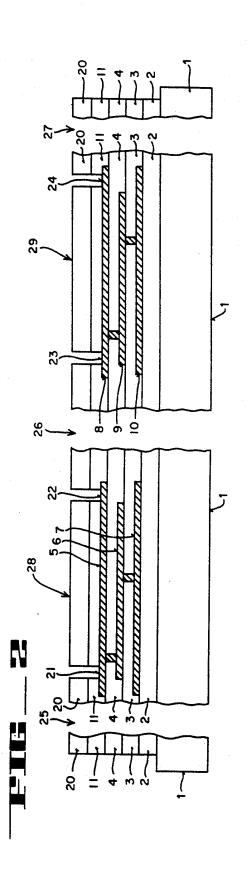
[57] ABSTRACT

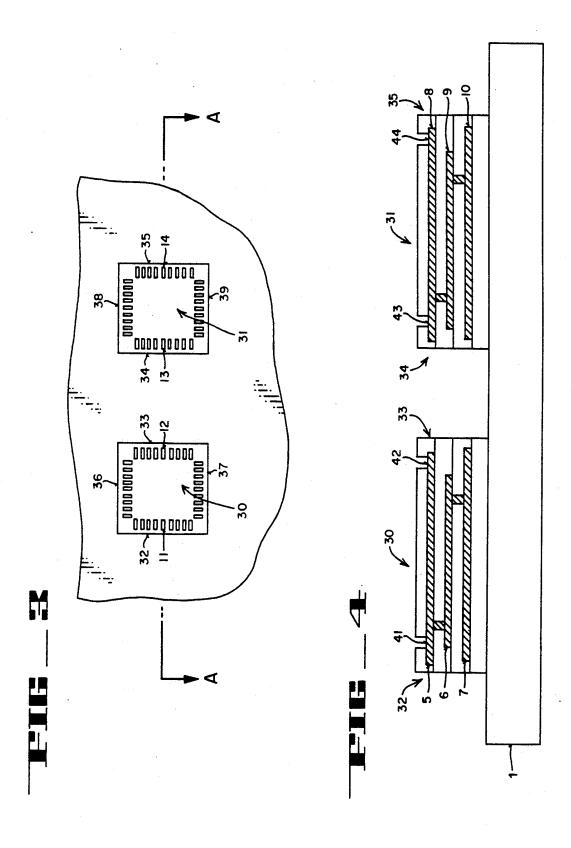
Described is a structure and process for forming a hermetically sealed chip. This hermetically sealed chip will greatly simplify packaging requirements and eventually lead to the realization of a "packageless chip". The hermetic sealing is composed of two parts, an extremely thin passivation layer which is deposited over the entire chip top and side surfaces and a passivation layer which is deposited over the bonding pad surface. Preferably, SiN is deposited as a chip surface passivation layer and Ni is selectively deposited as a metal passivation layer. The extremely thin nitride layer will minimize the stress and the amount of hydrogen in the SiN film and minimize deleterious effects upon device performance caused by stress and hydrogen. The thickness of the metal passivation layer may be the same as that of the dielectric layer so as to give a planar surface or it may be thick enough so as to give a protruding metal passivation bump.

11 Claims, 7 Drawing Sheets

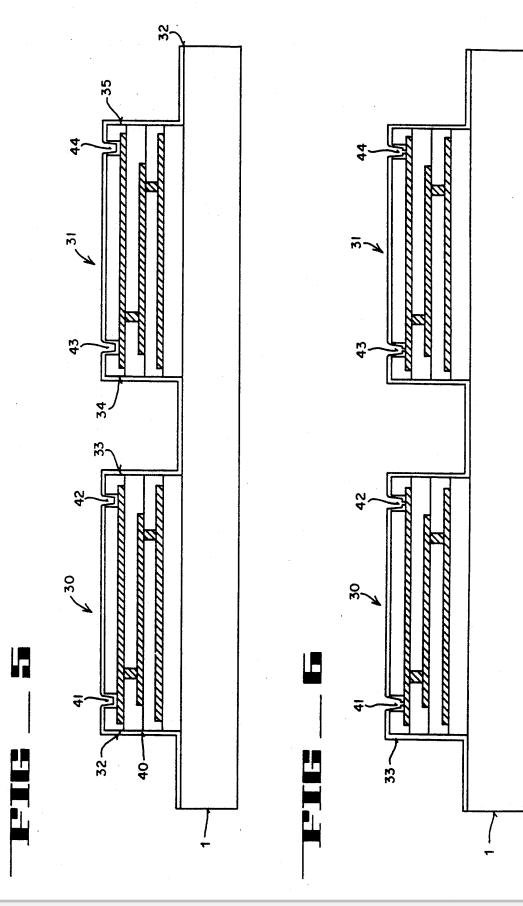




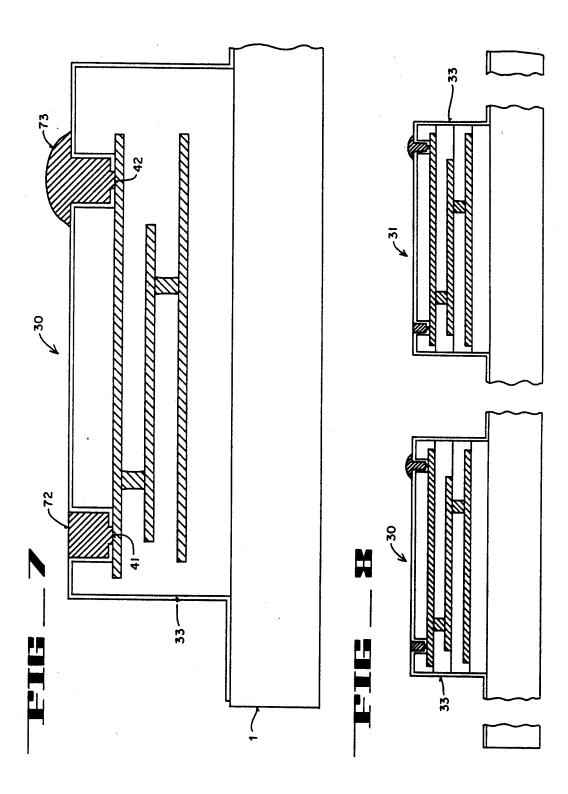














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