United States Patent [19]

Chen

[11] Patent Number: 5,538,924

[45] Date of Patent: Jul. 23, 1996

[54] **METHOD OF FORMING A MOISTURE GUARD RING FOR INTEGRATED CIRCUIT APPLICATIONS**

[75] Inventor: **Chung-zen Chen**, Hsinchu, Taiwan

[73] Assignee: **Vanguard International Semiconductor Co.**, Hsinchu, Taiwan

[21] Appl. No.: **523,792**

[22] Filed: **Sep. 5, 1995**

[51] Int. Cl.^{6} **H01L 21/465**

[52] U.S. Cl. **437/246**; 437/195; 437/191; 437/193; 437/922; 148/DIG. 55

[58] Field of Search 437/195, 191, 437/192, 193, 186, 245, 246, 922; 148/DIG. 55

[56] **References Cited**

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Primary Examiner—Trung Dang
Attorney, Agent, or Firm—George O. Saile; William J. Stoffel

[57] **ABSTRACT**

An improved structure and method for forming an integrated circuit guard ring which prevents contamination/moisture from diffusing through a fuse opening, in the insulating layer(s), to device areas, is described. A first insulating layer is formed over portions of the substrate. A gate insulating layer is formed surrounding the first insulating layer. The first ring surrounds a fuse area—including the area where the fuse will be cut by a laser or burned by a current. A first dielectric layer is formed over the substrate surface. A first passivation layer is then formed over the first insulating layer. A first opening is formed through the first passivation layer and first dielectric layer over the first ring. A fuse is formed over the first passivation layer over the fuse area and a second ring of water impervious material is formed on the first ring through the first opening. The first and second rings form a moisture impervious seal. A second insulating layer is then formed over the fuse and the first insulating layer. A fuse opening is etched over at least the fuse area through the second insulating layer and can expose the fuse. A second passivation layer is formed over the second insulating layer and the fuse.

9 Claims, 5 Drawing Sheets
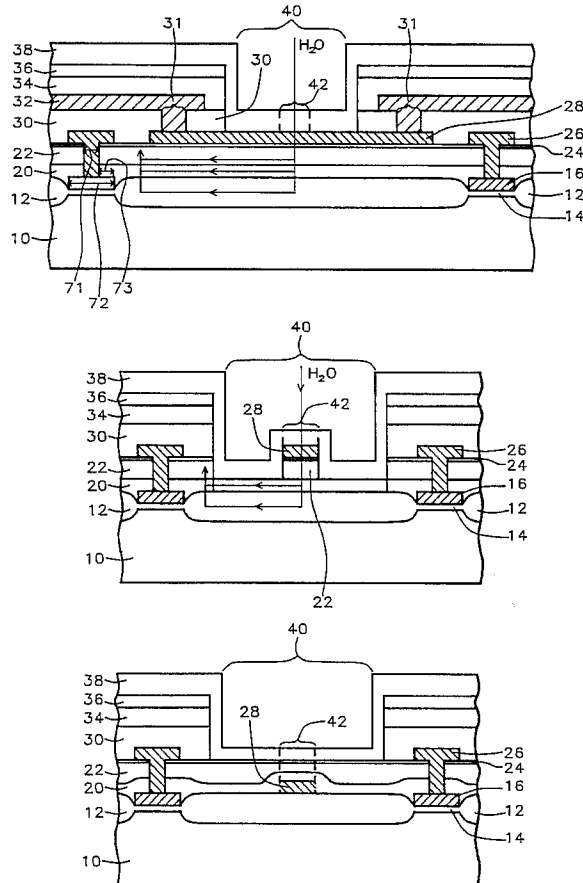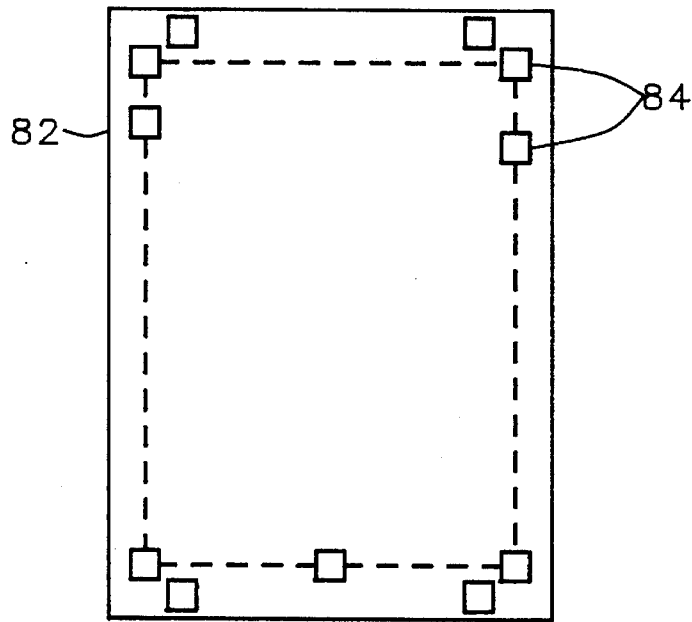
FIG. 1A
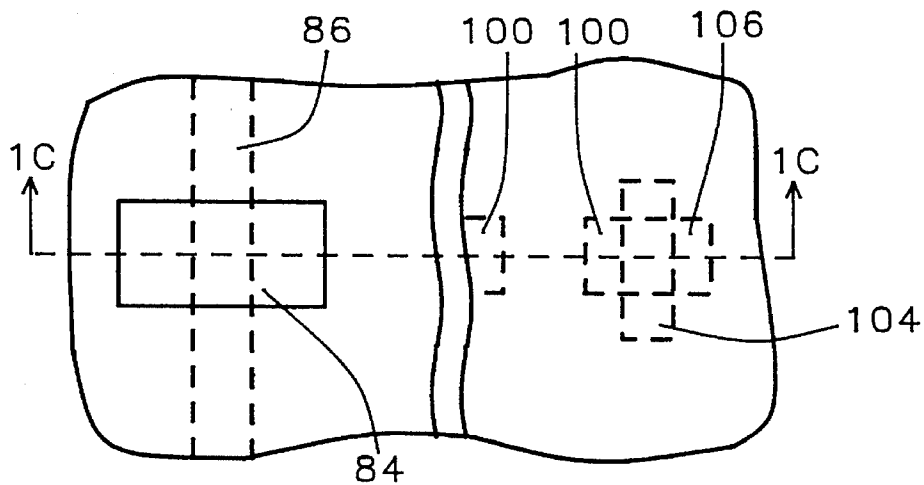
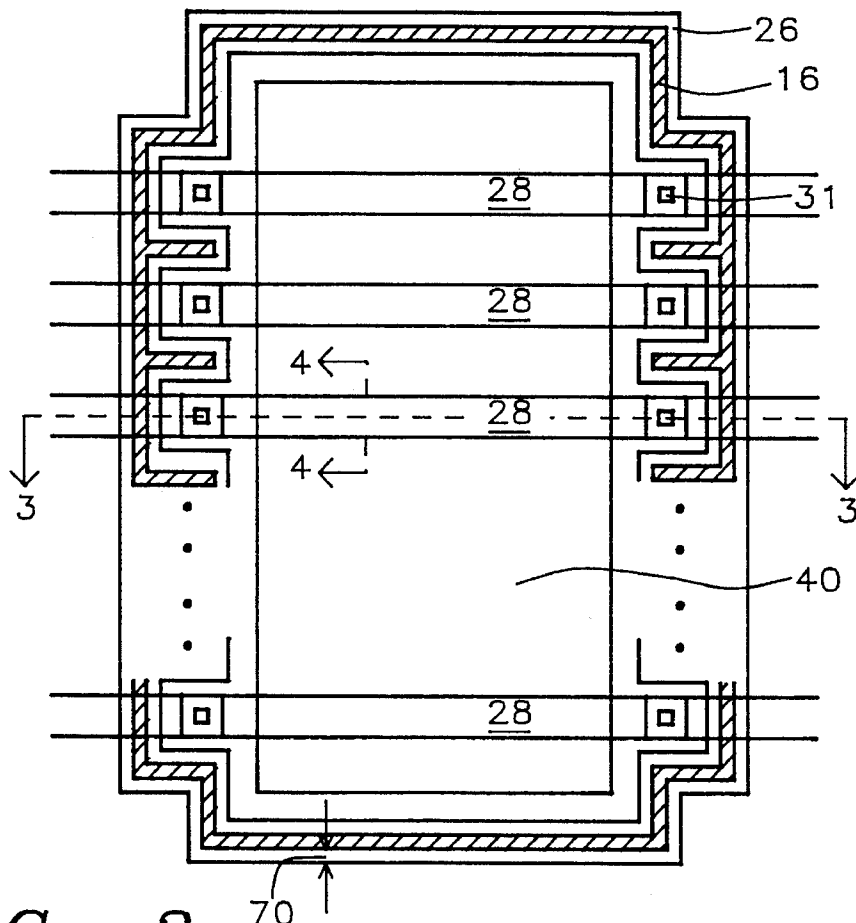*FIG. 1B - Prior Art*
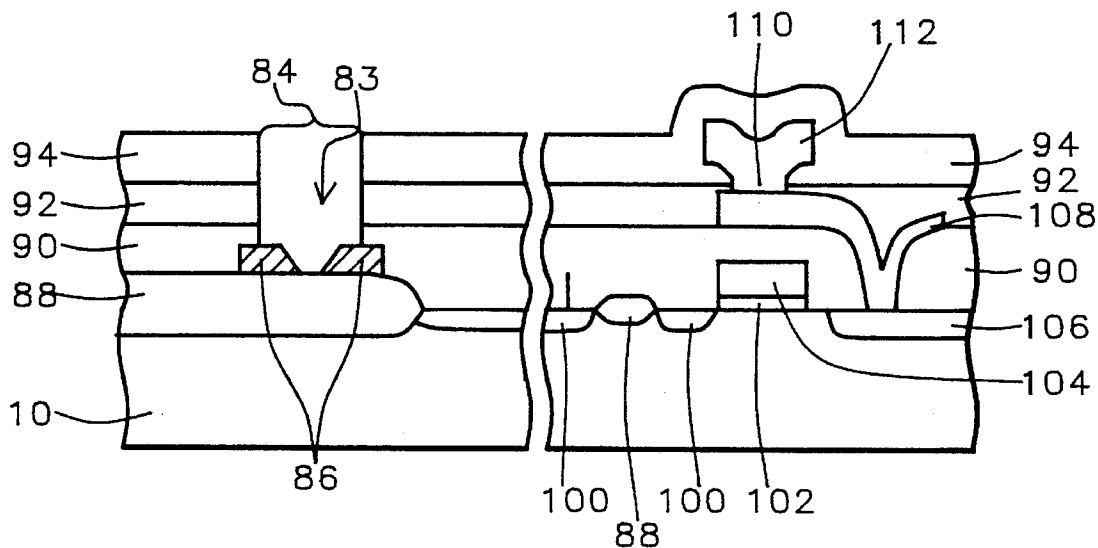
FIG. 1C – Prior Art
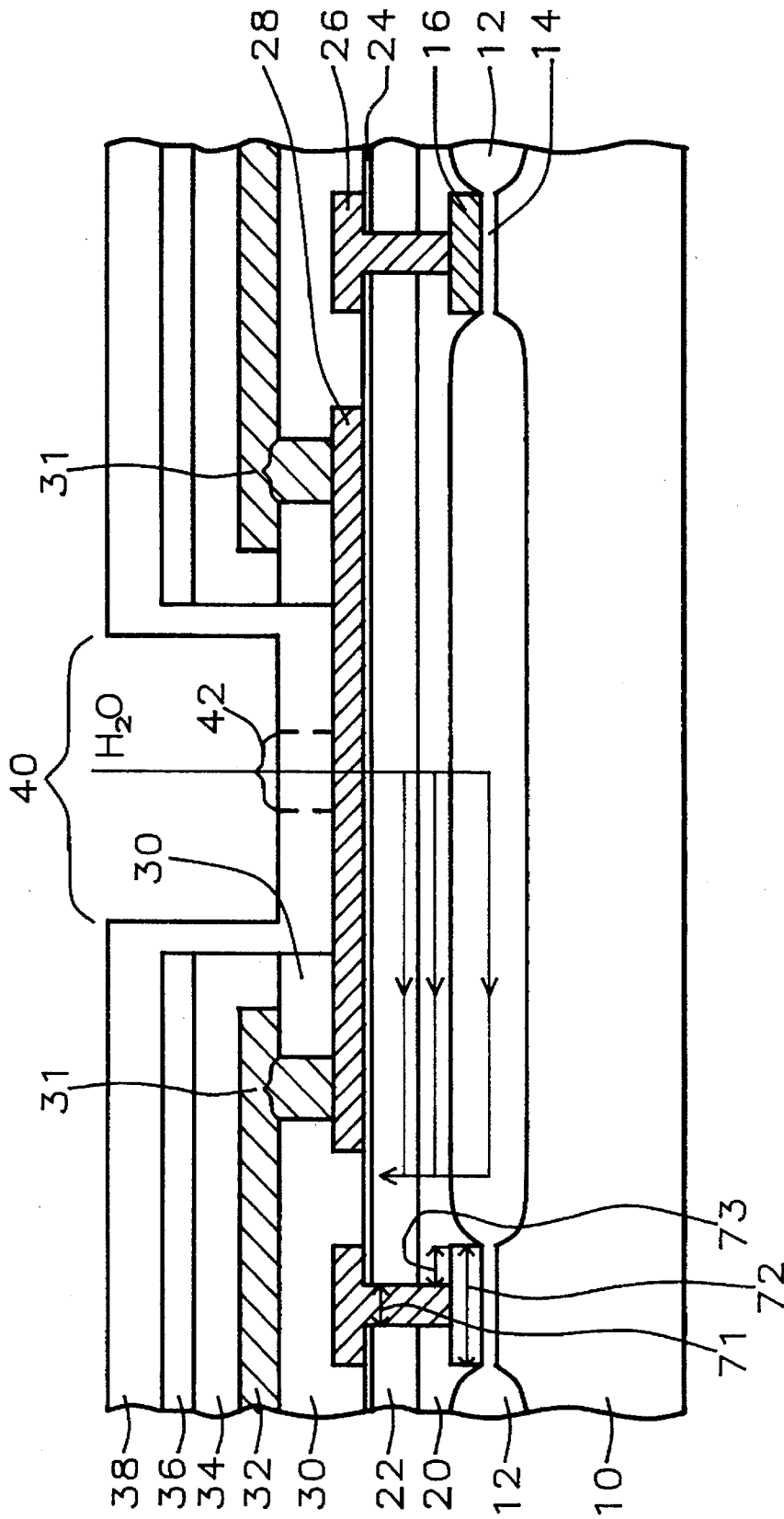
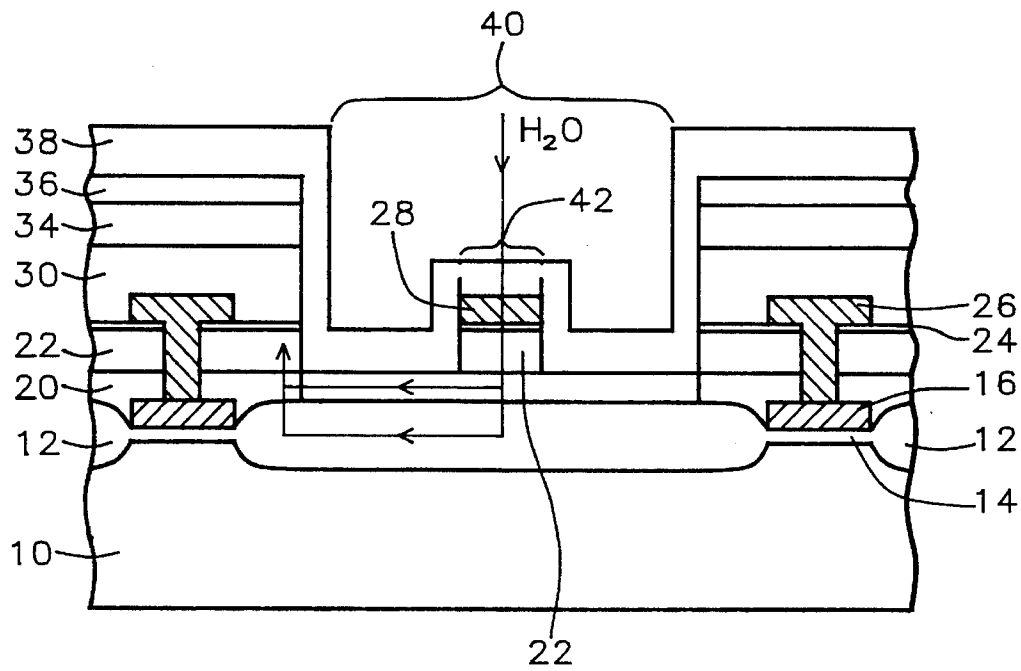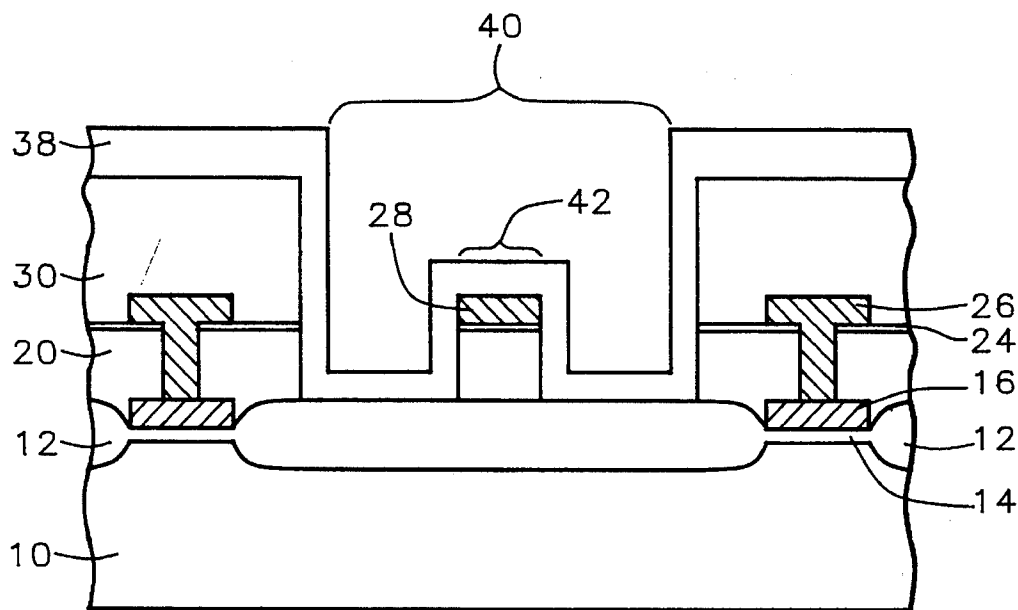**FIG. 2**

FIG. 3

FIG. 4

FIG. 5

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