Curriculum Vitae of Dr. Michael E. Thomas

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Areas of Knowledge

Industrial Engineering Management, Semiconductor Dielectric and Metal Materials Research, Expertise in PVD and CVD Processing of Materials, Interconnect Manufacturing Processes, Packaging Materials Development, Student and Professor Mentoring. Experience in establishment of IP protection and development strategies.

Experience

2003 – Present: Michael E. Thomas – Semiconductor Technology Consultant - Thomas Consulting
Los Altos CA

Activities focused on providing technical expertise and counsel to industrial clients in the areas of semiconductor process technology and intellectual property. Technical expertise in the areas of state of the art thin film electronic materials, the history of materials use in the semiconductor industry and new methods of using opto-electronic interconnect materials. Below is a summary of my major consulting activities to date:

- 10/2014 – Present. Providing consulting services to Steptoe and Johnson LLP, regarding patent litigation involving Raytheon vs. Samsung, SONY, Apple and OmniVision. Consulting for Raytheon.
- 4/2014 – Present. Providing Consulting service as expert to Cabot Microelectronics in pending litigation of CMC vs. Davies regarding slurry technology. Trial set for mid-2015.
- 2/2011 – 4/2014. Providing Consulting Services for Elpida Corporation vs. Intellectual Ventures and Elpida Corporation vs. MOSAID through the Law Offices of Kenyon and Kenyon, New York, N.Y. - Case settled.
- 10/2011: Providing Consulting Services for Microchip Corporation for Microchip Corporation vs. LSI/Agere Corporation through the Law Offices of Covington and Burling, LLP. San Diego, CA – Case Settled out of Court
- 7/2008 – 9/2010 Acted as an Expert Witness for the Defendants in the Samsung vs. AMD litigation representing Samsung. Worked with Covington and Burling Law Offices. Case settled out of Court.
- 5/2008-7/2009 Provided Analysis and Testimony as Expert Witness for Invalidity portion in ITC Court Case # 337-TA-648 as the Expert for the Defense of Multiple Corporations - Nanya, IDT, Jazz, Tower, Powerchip, Qimonda AG and Grace Semiconductor vs. LSI/Agere Corporation. The Court Hearing in Washington, D.C. on 7/20/2009 resulted in the defendants prevailing in this case, which involved the restriction of imported devices. The Agere/LSI patents ‘335 which was addressed in my opinions and testimony was found to be invalid in by the Judge and ITC 6 member board and no damages were ascribed to my clients. This case was favorably resolved out of Court for the other defense litigants in this case (National, UMC, ProMOS, Dongbu, Micronas, Microchip, Elpida, Microchip, and others).

- 1/2008 – Settled . Acted as an Expert Witness in the case of SONY vs. Agere, where SONY was the defendant. Worked with the law firm of Kenyon and Kenyon, N.Y. representing SONY.
- 1/2007 – 11/2009. Acted as professional consultant (not Expert) for SMIC (ongoing) in Court action regarding SMIC vs. TSMC regarding trade secret issues. Case has not yet gone to Court. Working with law firm of Wilson, Sonsini, Goodrich and Rosatti in Palo Alto, CA representing SMIC.
- 8/2006 – 10/2007. Testimony as Expert Witness for ROHM Corporation in Arbitration hearing on nine Agere technology patents in ROHM vs. Agere Corporation, which was completed in October 2007 in San Francisco, CA. Worked with Fish Richardson of New York, the law firm representing ROHM. Outcome was favorable to ROHM.
- 1/2006 – 6/2007. Expert Witness consulting for SEL of Japan regarding two LCD related patent litigations with Toppoly vs. SEL which was resolved out of Court and Chi Mei vs. SEL which was resolved by Court ruling. Worked with Jenner and Block law firm in Chicago in representing SEL as plaintiff in both cases.
- 12/2005 – 7/2006. Participated as Expert Witness in litigation between AMD and Oki Electric regarding CVD W interconnect technology. Worked with Kellog, Huber, Hansen, Todd, Evans & Figel, P.L.L.,Washington, D.C.representing Oki Electric, Corp. Settled out of Court.
- 6/2003 – 6/2006. Provided Analysis and Testimony as Expert Witness for Atmel Corporation in Court Case of Agere vs, Atmel Corporation held in Philiadelphia, PA in March of 2005 in collaboration with the legal offices of Heller Ehrmann. Atmel prevailed in this case as the defendant, which involved over $137 million dollars in potentially claimed damages by Agere. All four Agere patents, three of which were addressed in my opinions and testimony were found to be invalid in a jury trial and no damages were ascribed to Atmel. This case was resolved out of Court in June 2006
- 12/2005 – Provided Technical Consulting advice for White and Case, LLP in Palo Alto regarding sputtering gun technology.

1999-2003 Honeywell Electronic Materials Corporation
Sunnyvale, CA 94089

Position: Chief Technology Officer – Electronic Materials Division, Sunnyvale, CA

Responsibility as Chief Technical Officer was to construct a $50M+ state-of-the-art Materials Technology Center for Interconnect Materials solutions. Organized a 80+ person research team to assemble a facility to develop and evaluate low k dielectric, PVD metallization and lithography products for deep submicron manufacturing technologies. Oversaw new packaging materials development centered around thermal management and high I/O count interconnect for BGA and high power applications. Established a strong IP based research group which averaged over 60 patent filings / year with approximately 20 US patents granted/year. Established a formal patent filing and review process to generate IP as a strategic and tactical resource to protect technical investments from competitors and avoid early product commoditization. Spearheaded the technical aspects of global marketing effort for the organization and established guidelines for the disclosure of sensitive technical

information to our customers. Responsible for hiring and establishing a world class technical staff with a diverse skill set which married new materials synthesis and development with integrated circuit process engineering. Generated industry-wide technical reviews related to new low k dielectric materials and transport phenomena in structures at submicron feature sizes. Participated in the International Interconnect Technology Conference Organizing Committee (IITC) to promote greater knowledge of the required interconnect technology for advanced circuit requirements.

1987-1999 National Semiconductor Corporation
Santa Clara, CA 95052

Position: Engineering Project Mgr./Sr. Member of Research Staff

Responsible for identifying and examining new R&D areas related to deep submicron interconnect technology. Performed extensive yield analyses associated with interconnect processing. Conducting studies on the integration of new low e dielectrics and refractory metal/ Al alloy conductor systems into production process flows. Used cost models to examine MCM technologies as a competitive cost effective alternative to monolithic VLSI devices. Mentoring Professors and students performing CVD metal deposition research at SUNY/Albany under the sponsorship of the Semiconductor Research Corporation (SRC) Program and yield programs at Carnegie-Mellon University. Member of Selection Committee for the establishment of MARCO through the SRC. Examined new interconnect alternatives to provide low noise generation and better signal integrity in VLSI circuits. Participated as an Industrial Advisory Board Member to the Deans of Engineering at San Jose State University and San Francisco State University. Co-Chair for the SIA National Roadmap Committee for Interconnect Technology representing National Semiconductor.

1983-1987: Fairchild Research Center, Fairchild Semiconductor
Corporation, Palo Alto, CA 94304

Position: Engineering Project Mgr. / Sr. Staff Engineer

Responsibilities involved material and process R&D for micron and submicron multilevel interconnect technologies. Areas of expertise involved the fabrication of barrier and interconnect metallizations, inorganic interlevel dielectrics and novel thin film conductor structures. Generated specifications for fine pitched 3 level metal for production in advanced bipolar and CMOS memory and logic.

1982-1983: Gate Array Division, Fairchild Semiconductor Corp.

Position: Sr. Staff Engineer

Developed spin-on glass dielectrics and metal lift-off processes for use in Gate Array devices.

1979-1982: Fairchild Research Center, Fairchild Semiconductor
Corporation, Palo Alto, CA 94304

Position: Member of Technical Staff

Basic Research performed on sputtered Pt and wide gamut of refractory metal silicides for device applications. Also performed a large number of studies on potential barrier layer materials such

as nitrides, carbides and borides. Integrated TaSi2/Poly Si films into 64K MOS memories. Performed electromigration studies on a wide range of Al alloys.

Educational Background

1. 1973-1980 MSE and PhD. In Materials Science and Engineering
Stanford University, Stanford, California
Ph.D. Thesis: A Study of CO Chemisorption on Mica Supported Microsurfaces of Pd and Ni Using the Thermal Desorption Spectroscopy / Transmission Electron Microscopy / Transmission Electron Microscopy Technique.
Advisor: Professor Guy Marshall Pound

2. 1969-1973 BSE In Chemical Engineering and BSE In Metallurgical Engineering (Double Major).
University of Michigan, Ann Arbor, Michigan
Advisor: Professor Richard Flinn

Journal Publications

1. M.E. Thomas, J.T. Dickinson, H. Poppa and G.M. Pound, "Chemisorption of CO on Pd Particles Supported on Mica", J. Vac. Sci. Technol. 15(2) (1978) 475.
2. M.E. Thomas, H. Poppa and G.M. Pound, " The Study of Microsurfaces" Using Thermal Desorption Spectroscopy", Thin Solid Films, 58 (1979) 273.
3. J.M. Pierce and M.E. Thomas, " Electromigration in Aluminum Conductors which are Chains of Single Crystal Grains", Appl.Phys. Lett, 39(2) (1981) 165.
4. R.R. Razouk, M.E. Thomas, "Oxidation of TaSi2/Polycrystalline Silicon Structures in Dry Oxygen", J. Appl. Physics, 53(7) (1982) 5342.
5. J.M. De Blasi, R.R. Razouk and M.E. Thomas, " Characteristics of TaSi2 / Poly Si Films in steam for VLSI Applications", J. Electrochem. Soc., 130(12), (1983), 2478.
6. R. Beyers, R. Sinclair and M.E. Thomas, " The Effect of Oxygen in Cosputtered Ti and Si Films ", Mat. Res. Symp. Proc. 14(1983) 423.
7. R. Beyers, R. Sinclair and M.E. Thomas, " Phase Equilibria in Thin Film Metallizations", Jour. Vac. Sci. Technol. B2(4), (1984) pp. 781-784.
8. R. Beyers, R. Sinclair and M.E. Thomas, " Ternary Reactions Between Integrated Circuit Materials", Proc. of Electrochem. Soc., Fall Meeting, Las Vegas, (1986), pp. 1-3.
9. R. Beyers, M.E. Thomas and R. Sinclair, “TEM studies of cosputtered titanium silicide (TiSi2) films containing excess silicon”, Materials Research Society Symposium Proceedings , 25 (Thin Films Interfaces 2) (1984), pp. 601-605.
10. M.E. Thomas, T.K. Keyser, and E.K.W. Goo, "Interfacial CuAl2 Precipitate Nucleation and Growth During the Deposition of Al-4%Cu-1.5%Si Alloys", J. Appl. Phys. 59(11) (1986) pp. 3768 - 3773.
11. A.K. Kapoor, M.E. Thomas, and M.B. Vora, " A Low Barrier Schottky Process Using MoSi2", IEEE Trans. Electron Dev. , ED-33, No.6, June (1986)., pp. 772-778.
12. W. Maly, M.E. Thomas, J.D. Chinn and D.M. Campbell, " Double Bridge Test Structure for the Evaluation of Type, Size and Density of Spot Defects", Carnegie Mellon Report # CMUCAD-87-2, February (1987).
13. J. A. Doi,.M.E. Thomas, W. Maly, “Detection and physical characterization of spot defects in metal IC interconnections.”, Electrochemical Society (1988), 88-13 (Proc. Symp. Autom.

Integr. Circuits Manuf., 3rd, (1987), pp. 119-35.
14. W. Maly, M.E. Thomas, J.D. Chinn and D.M. Campbell, " Double Bridge Test Structure for the Evaluation of Type, Size and Density of Spot Defects", Published in the "International Workshop on Designing for Yield, Oxford, England, July (1987). Also Published in "Yield Modelling and Defect Tolerance", Editor W. moore et al, Adam Hilger Publ., Bristol, 1988.
15. M.E. Thomas and W. Maly, " Multilevel Interconnect Yield Estimates Using the Double Bridge Test Structure", V-MIC Conf., (1988) 229.
16. M.E. Thomas, M.P. Hartnett, J.E. McKay, A.K. Kapoor and J.D. Chinn , "The Potential of Using Refractory Metals and Barrier Layers to Generate High Temperature Interconnects", V-MIC Conf., (1988) 183.
17. A.K. Kapoor, M.E. Thomas, J.F. Ciacchella and M.P. Hartnett, " Tantalum Nitride - p - Si High Voltage Schottky Diodes", IEEE Trans. on Electron Dev., Vol. 35(8) (1988) pp. 1372 -1377.
18. M.E. Thomas, M.P. Hartnett and J.E. McKay, " The Use of Surface Profilometers for the Measurement of Wafer Curvature ", J. Vac. Sci. Technol., A 6(4) (1988) 2570.
19. W. Maly, R.A. Hughes, M.E. Thomas and D.M. Campbell, " Methodology for Multilevel Interconnect Yield Prediction" 1989 Sympos. on VLSI Circuits, Kyoto, Japan.
20. M.P. Brassington, M. El-Diwany, R.R. Razouk, M.E. Thomas and P.T. Tuntasood, "An Advanced Single-Level Polysilicon Submicrometer BiCMOS Technology", IEEE Trans. on Electron Dev., Vol. 36(4) (1989) pp. 712.- 719.
21. P. Renteln, M.E. Thomas and J.M. Pierce, "Characterization of Mechanical Planarization Processes", V-MIC Conf. (1990) 57.
22. M.E. Thomas, S. Sekigahama and S.A. Myers, "Issues Associated with the Use of Electroless Cu Films for Submicron Multilevel Interconnections", V-MIC Conf. (1990) 335.
23. M.E. Thomas, S. Sekigahama, P. Renteln and J.M. Pierce , " The Mechanical Planarization of Interlevel Dielectrics for Multilevel Interconnect Applications", V-MIC Conf. (1990) 438.
24. M.E. Thomas, I.A. Saadat and S. Sekigahama, "VLSI Multilevel Micro-Coaxial Interconnects for High Speed Devices", IEDM Dec. (1990) 3.5.1.
25. J. Khare, B. Daniels, D. Campbell, M.E. Thomas and W. Maly, " Extraction of Defect Characteristics for Yield Estimation Using the Douvle Bridge Test Structure", Intern, Sympos. on VLSI Tech, Systems, and Applications, Taipei, Taiwan, May (1991) 424.
26. I.A. Saadat and M.E. Thomas, "VLSI Interconnect Options for On-Chip High Performance Applications", Wescon, Nov. (1991) 318.
27. M.E. Thomas, I.A. Saadat and S. Sekigahama, " Multilevel Microcoaxial Interconnect for Microwave Applications", GOMAC (1991) 609.
28. M.E. Thomas, S. Sekigahama, P. Renteln and J.M. Pierce ," Mechanical Planarization Process Characterization," Invited Paper, 1990 Semicon Japan Technical Session Proc., Chiba, Japan, Dec. (1991) 295.
29. F.A. Sherrima, I.A. Saadat, S. Sekigahama, A. Abdo, J. O'Brien and M.E. Thomas, " Manufacturing Studies of BCB as the Interlevel Dielectric Material for Multilevel Interconnect and VLSI Applications" ISHM, San Francisco, Oct (1992) pp. 596-600.
30. W. J. Dressick, C. S. Dulcey, J. M. Calvert, J. H. Georger, G. S. Calabrese, M. E. Thomas, H. A. Stever, “Selective Electroless Metalization of Patterned Ligand Surfaces”, , Materials Research Society Symposium Proceedings (1992), 260 (Advanced Metallization and Processing for Semiconductor Devices and Circuits-II), pp. 659-64
31. A.E. Gattiker, W. Maly and M.E. Thomas, " Are There Any Alternatives to Known Good Die?" , MultiChip Module Conference, Santa Cruz, (1994) 102.
32. M.E. Thomas, " Manufacturing Considerations for VLSI Interconnect Systems", Materials Research Society Symposium Proceedings 337 (1994), - (Advanced Metallization for Devices and Circuits: Science, Technology and Manufacturability), pp. 13-24.

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