UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SHARP CORPORATION, SHARP ELECTRONICS CORPORATION, and SHARP ELECTRONICS MANUFACTURING COMPANY OF AMERICA, INC.,
Petitioners

v.

SURPASS TECH INNOVATION LLC,
Patent Owner

Case IPR2015-_____
Patent No. 7,420,550

DECLARATION OF MICHAEL J. MARENTIC IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,420,550

1. I, Michael J. Marentic, make this declaration in connection with the Petition for *Inter Partes* Review submitted by Sharp Corporation, Sharp Electronics Corporation, and Sharp Electronics Manufacturing Company of America, Inc. (collectively "Petitioners" or "Sharp") for review of Claims 1 through 5 of U.S. Patent No. 7,420,550 to Yuh-Ren et al. ("the '550 Patent"), which is assigned to Surpass Tech Innovation LLC ("Patent Owner" or "Surpass").

2. Throughout this declaration, I refer to exhibit numbers that correspond to the exhibits to the Petition for *Inter Partes* Review for which I provide this declaration.

Scope of My Assignment

3. I have been requested by counsel for Sharp to study the '550 Patent, including its claims and prosecution history, as well as the references specifically referred to in this declaration. I have also been requested by counsel for Sharp to provide my expert opinion regarding the invalidity of Claims 1-5 of the '550 Patent. I further expect to offer an additional declaration in response to any declaration submitted by any expert for the Patent Owner.

Summary of My Opinions

4. It is my opinion that Claims 1-3 of the '550 Patent are invalid as anticipated under 35 U.S.C.§ 102(b) and Claims 4-5 are obvious to a person of ordinary skill in the art under 35 U.S.C. §103(a). Moreover, it is my opinion that in addition to being anticipated, Claims 1-3 are also rendered obvious over prior art.

5. Specifically, I believe that the following are grounds to find Claims 1-5 of the '550 Patent invalid:

a. Claims 1-3 are invalid under 35 U.S.C. § 102(b) as anticipated by Japanese Patent Application Publication No. H08-305322 (Ex. 1002, "the Sharp Reference").

b. Claims 1-3 and 5 are also invalid under 35 U.S.C. § 103(a) as obvious over the Sharp Reference.

c. Claims 1-5 are also invalid under 35 U.S.C. § 103(a) as obvious over the Sharp Reference in view of U.S. Patent No. 6,407,795 to Kamizono, et al. (Ex. 1004, "Kamizono").

d. Claims 1-5 are also invalid under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 6,081,250 to Shimada et al. (Ex. 1003, "Shimada") in view of Kamizono.

Summary of My Professional Background and Qualifications

6. Exhibit 1008 is my *curriculum vitae* which sets forth my professional background and qualifications. A list of publications that I have authored or co-authored is included.

7. I have many years of experience in the flat panel display industry. I first became involved in the flat panel display industry in 1973, when I began working at the University of Illinois Coordinated Science Laboratories where the AC Plasma Display Panel

("PDP") was invented. During my studies at the University, I was employed as an intern working in the area of plasma display construction and gas discharge physics characterization. I received a B.S. degree in Engineering Physics from the University of Illinois.

8. Upon entering graduate school, I continued my work on the characterization of the gas discharge in the pixels. I received an M.S. degree in Electrical Engineering from the University of Illinois, and wrote my master's thesis on measuring the electron density in an AC PDP.

9. One of my engineering positions was with Interstate Electronics Corporation (IEC) as a design electrical engineer. IEC designed drive electronics, mechanically packaged the display modules, and incorporated them into terminals for harsh, military environments. I designed several distinct versions of drive electronics for PDPs, including one using packaged silicon integrated circuits on flexible circuits, or "chip-on-flex." During this time, I was awarded several patents relating to PDP technologies. I also investigated LCDs and thin film electroluminescent displays for incorporation into military applications.

10. I later formed Plasma Displays, Inc., a single proprietorship consulting corporation. I worked for several clients, one being Bell Laboratories and AT&T at their joint Reading, Pennsylvania facility. This facility was where the original picture phone was developed, the first commercial light emitting diodes ("LEDs") were manufactured, and

AT&T's PDPs were developed and manufactured. I worked on PDP drive electronic design, driver-to-panel interconnect reliability, driver circuit characterization, and yield improvement.

11. I was a founder and Vice President of Plasmaco, a company that acquired IBM's PDP production line in New York. Plasmaco manufactured several types of PDPs, including VGA panels with 640x480 pixels for early notebook computers. Such a panel had 5 driver ICs with 32 outputs per driver for 640 data lines. I also developed larger sized VGA panels with 1280x1024 pixels. Because of the increase in size, we used the same type of driver IC chips but doubled the number of driver ICs (i.e., using 10 driver ICs) in the display. When changing the panel design to increase the size of the panel and/or the number of pixels, it was a common practice to keep the same type of driver IC as the smaller panel, but it was necessary to increase the number of driver ICs to accommodate the added pixels in the larger display.

12. While at Plasmaco, I also developed and manufactured driver chip-on-glass ("COG") technology that passed extreme militarized environmental testing specifications. COG technology put electrode driver integrated circuits onto the glass edges of the PDP. The benefits of using COG technology were that it reduced the physical size and weight of a notebook computer display and increased the operational reliability of the display.

13. At Science Applications International Corporation, I worked on efficient backlights for LCDs, some for direct viewing in sunlight. Commercially available LCDs were

disassembled and repackaged with these backlights. The finished displays were used in cockpit avionics, medical, banking, and FAA towers.

14. At Hitachi, from 1995 to 1999, I managed a technology center that developed technologies relating to the interface between the motherboard and the LCD driver chips for flat panel monitors and notebook displays. I reported directly to the LCD design and manufacturing center in Japan. I had access to future LCD technical details and specifications, and facilitated technology transfer between Silicon Valley firms and Japan management. The Video Electronics Standards Association ("VESA") writes and publishes video standards for the electrical interfacing for displays. I was the chairman of the VESA flat panel display committee, a member of the board of directors, and later the president of the board of directors.

15. While at Philips, from 1999 to 2001, I managed a group of engineers that designed electronics for flat panel displays. My group designed interface timing ICs and video processing circuit boards for monitors and televisions utilizing LCDs. My group also worked with an IC design firm to develop the design of source and gate driver ICs for enhanced performance LCDs having various sizes. The enhanced performance LCDs were developed to provide high brightness and used multiple driver ICs, as well as the COG technology.

16. Philips invested in a tiled LCD display company, and I participated in the technology development using Philips panels. My group designed circuits and assisted with their incorporation into commercial products within Philips' worldwide subsidiaries.

17. Philips purchased the LCD factory of the Korean company LG, and later formed a joint venture called LG-Philips LCD. I was a member of the group of technical advisors that performed the due diligence for Philips for the purchase.

18. At Alien Technology, I was a member of the integrated design team that produced custom drivers made for cholesteric LCD displays, organic LEDs, and polymer dispersed LCDs. My responsibilities were IC product definition for the drivers and system architecture. Driver ICs were fabricated at silicon foundries and formed into small die for mass assembly utilizing Alien's fluidic assembly onto flexible, very low cost displays. Since Alien's products were very small sized, low cost LCDs, they typically involved only a single source driver and a single gate driver, whereas the larger sized LCD panels that I worked on while at Hitachi and Philips had multiple source and gate drivers.

19. I am the named inventor or co-inventor on three U.S. patents in the PDP field.

Materials Considered

20. In forming my opinions, I reviewed the following documents referenced by their exhibit number in the Petition for *Inter Partes* Review of the '550 Patent:

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 7,420,550 to Shen et al. ("'550 Patent")
1002	Japanese Patent Application Publication No. H08-305322 and Certified English Translation Thereof ("Sharp Reference")
1003	U.S. Patent No. 6,081,250 to Shimada et al. ("Shimada")
1004	U.S. Patent No. 6,407,795 to Kamizono et al. ("Kamizono")
1005	Prosecution History of U.S. Appl. No. 10/929,473
1006	U.S. Patent No. 5,805,128 to Kim et al. ("Kim")
1009	U.S. Patent Application Publication No. US 2003/0048249 A1 to Sekido et al. ("Sekido")

21. I also base this declaration on my knowledge from my 30 years of experience working on liquid crystal display (LCD) and related technologies.

22. I reserve the right to amend or supplement this declaration based upon any reports by any expert(s) for the Patent Owner, or any new documents and/or other information that becomes available.

Compensation

23. I am being compensated at my consulting rate of $250 per hour for my time spent in connection with this case. I am being separately reimbursed for any out-of-pocket

expenses. No part of my compensation is dependent upon the outcome of this proceeding or the nature of the opinions that I express.

Legal Standards

24. To render my invalidity analysis, I have been informed about the legal standards for patent invalidity in *inter partes* review proceedings before the Patent Trial and Appeal Board.

25. Specifically, I understand that the petitioner must prove patent invalidity by a "preponderance of the evidence," that there is no "presumption of validity" in *inter partes* review proceedings, and that claims are to be given their "broadest reasonable" construction in light of the specification as would be read by a person of ordinary skill in the art.

26. I also understand that a patent claim may be invalidated as anticipated if a single prior art reference discloses, either expressly or inherently, each and every element of the patent claim.

27. I also understand that a patent claim may be invalidated by one or more references, either alone or in combination, as being "obvious" to a person of ordinary skill in the art at the time the invention was made.

28. I understand that one way of demonstrating obviousness in the situation where a prior art reference discloses a single element but the claim requires multiple elements is to demonstrate that there are no new and unexpected results from increasing the number of such elements.

29. I further understand that an additional way of demonstrating obviousness is to demonstrate that one or more items of prior art either alone or in combination, contain all of the elements of a claim.

30. It is my understanding that in considering the issue of obviousness, I should consider what a person of ordinary skill in the pertinent art would have known at the time of the invention, as well as what such a person would have reasonably expected to have been able to do in view of that knowledge.

31. I understand that in analyzing the issue of obviousness, I should consider and determine: (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; and (3) the level of ordinary skill in the pertinent art.

32. I further understand that any of the following may provide a "reason" for combining elements known in the prior art: (a) a need or problem known in the field at the time of invention and addressed by the patent; (b) an obvious use of familiar elements beyond their primary purposes; (c) a design need or market pressure to solve a problem; (d) a simple substitution of one known element for another that would provide predictable results; (e) the use of known techniques to improve similar methods or products in the same way; or (f) some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

33. I also understand that claims may be invalid if they are directed to obvious design choices. Specifically, I understand that a patent claim that simply arranges old elements with each performing the same function it had been known to perform is not patentable. The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.

34. I also understand that certain "secondary considerations" of non-obviousness may be considered, to the extent that they exist. It is my understanding that such secondary considerations include, among others: (a) commercial success; (b) long felt but unsolved needs; and (c) the failure of others. I understand that there must be some connection to the secondary considerations and the claimed invention. I reserve my right to address any evidence or opinions the patent owner may submit on this issue.

THE '550 PATENT

35. I understand that the application leading to the '550 Patent was U.S. Patent Application No. 10/929,473, which was filed on August 31, 2004. For the purposes of my analysis, I assume that the time of the purported invention was August 31, 2004.

36. The '550 Patent relates to an active matrix liquid crystal display (LCD) device and driving circuit for the LCD device. In particular, the '550 Patent describes a specific way of connecting the gate and data lines to the thin film transistors (TFTs) driving pixels in an LCD panel.

LCD Panels and Driving Devices Were Known in the Prior Art

37. As acknowledged in the '550 Patent, active matrix LCD panels and the use of data and gate lines, or source and gate drivers for TFTs in LCD panels were all known in prior art. (Ex. 1001, '550 Patent, Col. 1:23-61, Figs. 1A-1B).

38. As shown below by multiple shaded blocks in annotated Figure 1A of the '550 Patent, the "Prior Art" driving circuit for LCD panels included multiple source drivers 11 and multiple gate drivers 12. (*Id.* at Fig. 1A). The source drivers 11 (purple boxes) provide image signals (i.e., video signals) to an LCD panel 10 through a plurality of data lines 111 (purple lines), while the gate drivers 12 (orange boxes) provide scanning signals (i.e., control signals) to the LCD panel 10 through a plurality of gate lines 121 (orange lines).

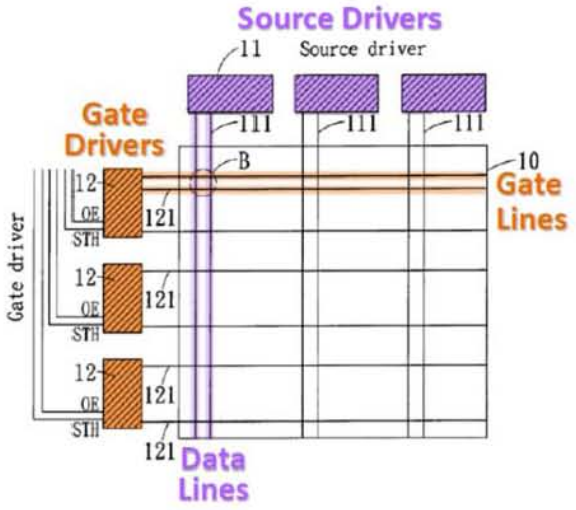


Fig. 1A (Prior Art)

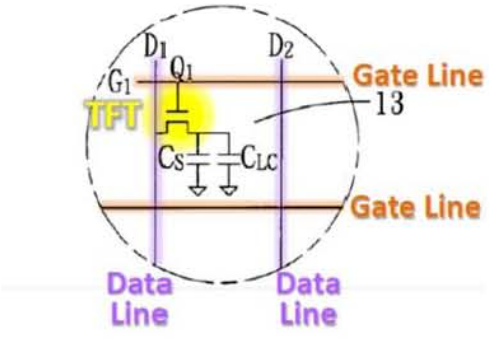


Fig. 1B (Prior Art)

39. As shown above in Figure 1A, prior art LCD panels included data lines 111 and gate lines 121 arranged in a matrix array.

40. According to the '550 Patent, the data lines 111 and gate lines 121 in the "Prior Art" shown in Figures 1A and 1B are "insulated with each other." (Ex. 1001, '550 Patent, Col. 1:45-47).

41. As shown above in Figure 1B, a pixel 13 in this prior art LCD panel is formed within each area enclosed by intersecting data lines (e.g., purple line D_1) and gate lines (e.g., orange line G_1).

42. As the '550 Patent acknowledges, each pixel 13 in prior art LCD panel included a thin film transistor Q_1 (TFT, highlighted in yellow), which is switched on and off by a control signal from the gate driver 12 through a gate line G_1.

43. The source of the TFT Q_1 receives the image signal sent from the source driver 11 through the data line D_1. An output voltage from the TFT Q_1 drives liquid crystal molecules corresponding to the pixel 13 to form an image. (*Id*. at Col. 1:45-57, Fig. 1B).

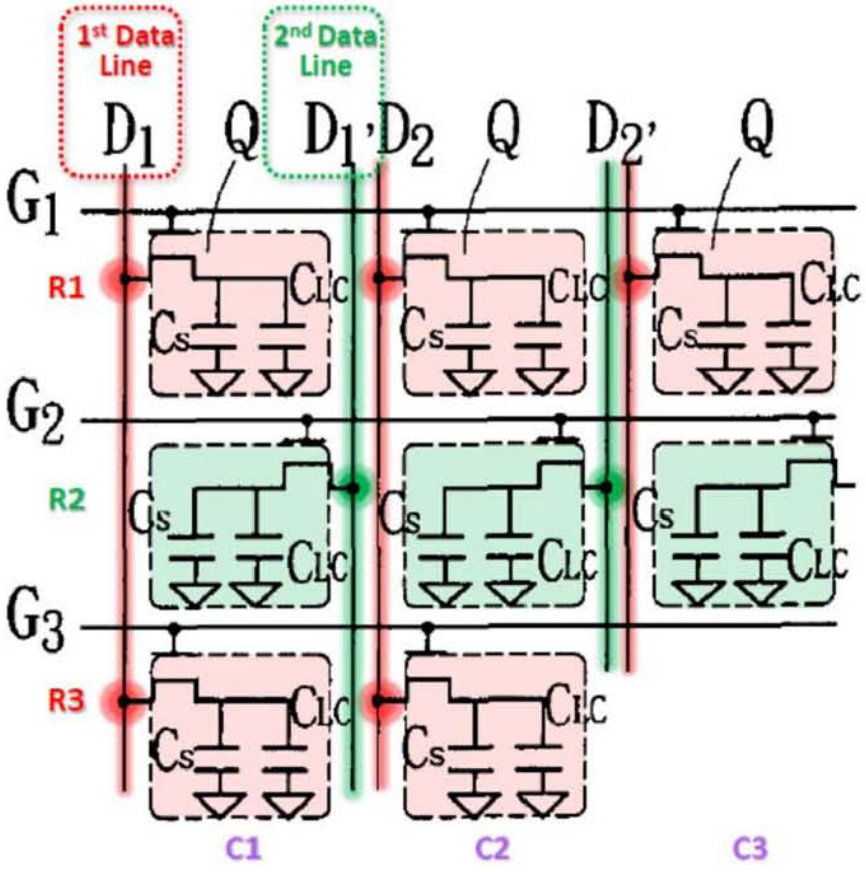
44. The time that an LCD needs to react to the driving voltage output by each TFT is called "response time," and the video quality of an LCD panel is dependent on this response time. In this regard, the video quality may be poor if the LCD response time is too long. (*Id*. at Cols. 1:62-2:41).

The Alleged Invention of the '550 Patent

45. According to the '550 Patent, its "chief object" is to provide an LCD driving circuit having a matrix structure in which the gate and data lines are connected to the TFTs in a specific way that allegedly increases "the response speed" of the LCD. (*Id*. at Col.

3:18-20, 35-40). This configuration is shown in, for example, Figure 4B, which is reproduced below.

'550 Patent Fig. 4B



46. As shown above in annotated Figure 4B, the driving device includes a matrix array formed from rows (R1-R3) and columns (C1-C3) of TFTs (Q). Each TFT in the matrix is associated with a pixel (represented by the dashed rectangles). The driving device further includes a certain number ("N") of gate lines G_i (i=1, 2, ... N), and a certain number ("M") of groups (e.g., pairs) of data lines D_j and $D_{j'}$ (j, j'=(1,1'), (2, 2'), ... (M, M')). For

example, as shown in Figure 4B above, the driving device has three gate lines, G_1, G_2, and G_3, and two groups of data lines ((D_1, $D_{1'}$) and (D_2, $D_{2'}$)).

47. As shown in Figures 4A, 5A, and 6A, the '550 Patent describes a source driver with a limit of 60 Hz but provides no further explanation or specification. Absent in the '550 Patent is the number of drive channels or outputs per source driver and matrix size. One would calculate the number of required driver ICs by dividing the horizontal pixel count by the number of drive channels per data driver. The driving device shown in Figure 4A uses 60 Hz source drivers; it doubles the normal calculated number of source drivers and mounts them on a single glass panel edge. The driving device shown in Figure 5A also uses 60 Hz source drivers; it again doubles the normal calculated number of data drivers, but mounts them on both the top and bottom edges of the panel with an interdigitated column connection. The driving device shown in Figure 6A uses 120 Hz or faster source drivers, mounted on one panel edge, and then adds dual switches to each output channel for driving the paired data electrodes.

48. The '550 Patent does not discuss the benefits or reasons for including a single source driver and a single gate driver on the one hand, and having a set of multiple source and gate drivers on the other hand.

49. Multiple source and gate drivers were commonly used in the prior art, particularly LCD panels as they increased in screen size. In fact, when I was in the LCD industry before the filing date of the '550 Patent, it was a common practice to change the

panel design to increase the size of the panel and/or the number of pixels by simply adding more driver ICs. For example, while the ***small***, low cost LCD panel (which had an equivalent pixel dimension of 7×4) that I worked on at Alien Technology had only a single source driver and a single gate driver, all the ***large sized*** LCD panels (which had pixel dimension of at least 800×600) that I worked on at Philips had multiple driver ICs.

50. Consistent with my experience, U.S. Patent Application Publication No. US 2003/0048249 A1 to Sekido et al. (Ex. 1009, "Sekido"), which was published on March 13, 2003, states that "in order to drive many gate bus lines and the source bus lines on the display circuit board, ***a plurality of the gate drivers and source drivers must*** be connected to the area around the liquid crystal display panel." (Par. [0006]) (emphasis added). Sekido further teaches that increasing the size of the LCD screen will increase the number of driver ICs in the panel. (Par. [0008]). Other prior art references discussed below also teach the use of multiple source and gate drivers for a large sized or high resolution LCD panel.

51. As shown above in Figure 4B, the gate line G_i (e.g., G_1, G_2, and G_3) in each row is connected to the gates of each TFT in that row. However, for each column, the first and second data lines D_j and $D_{j'}$ that form a group of data lines are not connected to all TFTs in that column. Instead, the first data line D_j in each column is connected only to the sources of the TFTs in the ***odd rows*** (see the red boxes in R1, R3, etc.) of that column,

while the second data line $D_{j'}$ in the same column is connected only to the sources of the TFTs in the ***even rows*** (see the green box in R2) that column. (*Id*. at Col. 8:10-31).

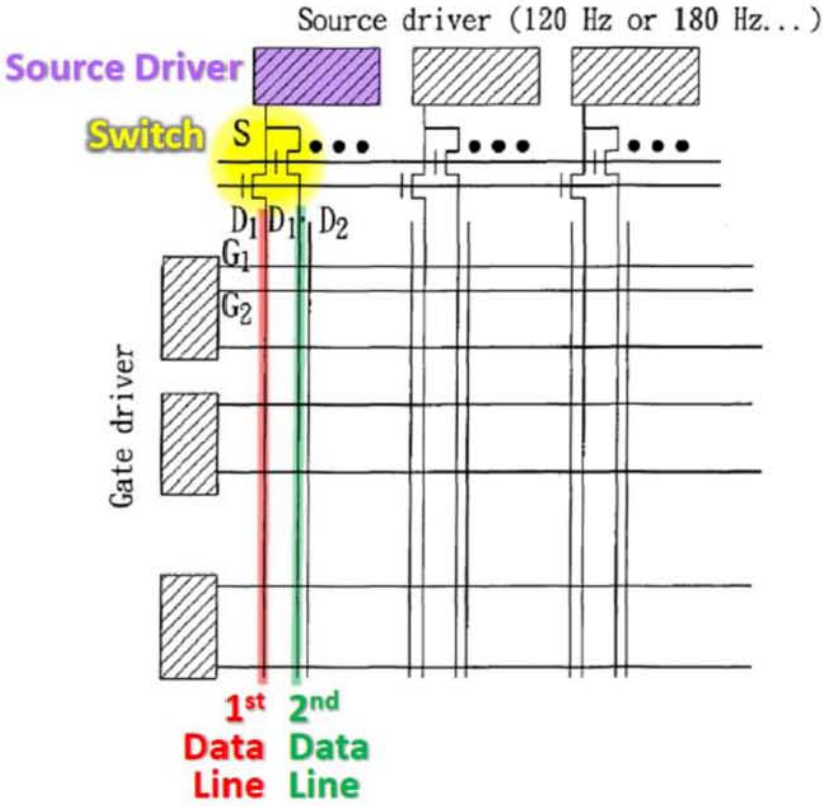
52. For example, referring to the first group of data lines D_1 and $D_{1'}$ (see the red and green lines) in first column (C1) of Figure 4B above, the first data line D_1 (see the red line) is connected to the sources (red dots) of the TFTs in the first and third rows (red boxes in R1 and R3 of the first column C1), while the second data line $D_{1'}$ (green line) is connected to the source (green dot) of the TFT in the second row (green box in R2 of the first column C1). Similarly, for the second pair of data lines (i.e., D_2 and $D_{2'}$) in the second column, the first data line (i.e., D_2) is connected to the sources of the TFTs in the first and third rows (i.e., R1 and R3 of the second column C2), while the second data line $D_{2'}$ is connected to the source of the TFT in the second row (i.e., R2 of the second column C2).

53. According to the '550 Patent, this alternating connection with the Odd Row/Even Row ("Odd Row/Even Row" configuration) reduces the response time of the LCD panel. (*Id*. at Col. 3:35-40). However, the '550 Patent does not explain how this reduction occurs.

54. The gate lines are connected to the gate driver are "insulated with each other;" and the data lines are connected to the source driver and are "insulated with each other." (Ex. 1001, '550 Patent, Col. 8:20-22, Col. 8:29-31). The '550 Patent goes on to explain that a space is provided between the neighboring data lines (e.g., $D_{1'}$ and D_2) to prevent them from short circuiting. (Ex. 1001, '550 Patent, Col. 8:31-36, Fig. 4C).

55. As shown below in annotated Figure 6A, the first and second data lines D_j and $D_{j'}$ (e.g., red and green lines D1 and D1') in each group (i.e., pair) of data lines are connected to the same source driver (purple box), and data is transferred to these data lines by an electronic switch S (highlighted in yellow). (*Id.* at Col. 5:4-8, Col. 8:50-52).

'550 Patent Fig. 6A



56. In addition, all of the source drivers are installed on the same side (e.g., upper side) of the LCD panel. (*See also id.* at Fig. 4A, Col. 8:37-38). The '550 Patent acknowledges that these components were arranged in the exact same way in the "Prior Art" in Figure 1A. (*Id.* at Col. 1:36-45, Fig. 1A).

57. The '550 Patent also states that the gate driver can be "a chip on glass or an integrated gate driver circuit on glass." (*Id.* at Col. 8:53-54). However, the '550 Patent does not define either of these terms, nor does it explain the difference between "a chip on glass" and "an integrated gate driver circuit on glass."

PROSECUTION HISTORY OF THE '550 PATENT

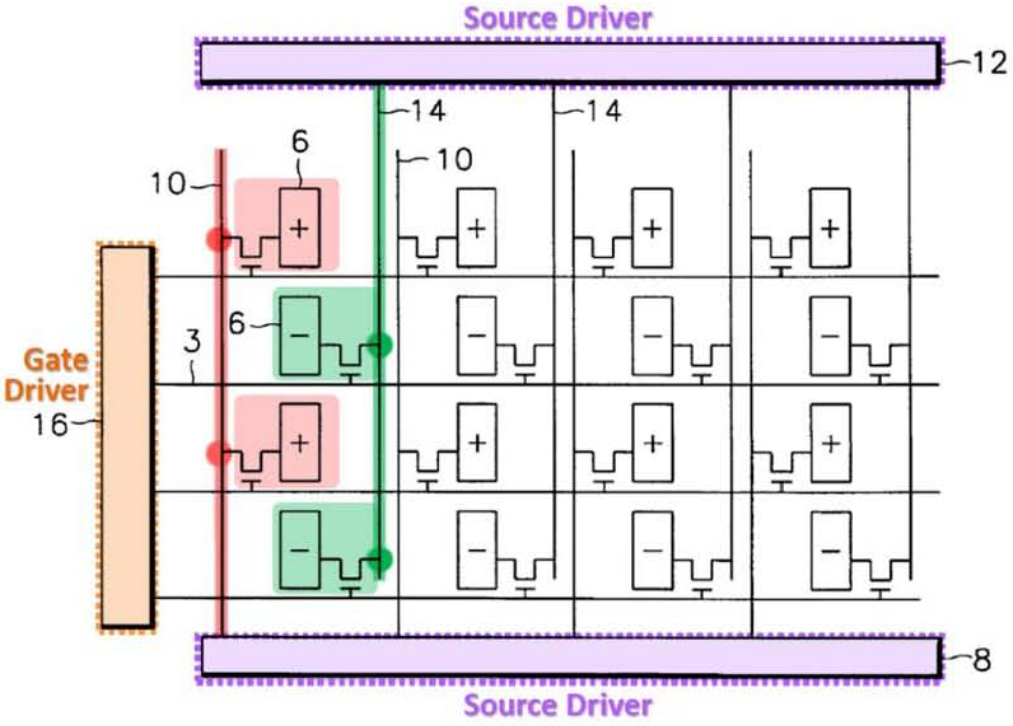
58. I understand that as originally filed, the application for the '550 Patent included claims directed to six different embodiments described in the '550 Patent. I also understand that, in response to a "Restriction Requirement" (Ex. 1005, p. 122), only the claims directed to the "First Embodiment" (i.e., "Species I; Figures 4A-4C") (*Id.* at p. 127) were elected and the claims directed to the other embodiments were canceled.

59. I understand that during prosecution, the application claim corresponding to Claim 1 of the '550 Patent was rejected as anticipated by U.S. Patent No. 5,805,128 to Kim et al. (Ex. 1006, "Kim"). (*See* Ex. 1005, p. 141). This application claim was identical to Claim 1, except that it did not include the last element of Claim 1, namely "the first data lines and the second data lines of each group of data lines are connected with the same source driver." (*See id.* at pp. 31, 152).

60. As shown below, annotated Figure 5 of Kim shows an LCD driving device of matrix structure type including the Odd Row/Even Row configuration, gate lines 3 connected to a gate driver 16, first data lines 10 connected to a data driver 8 on the bottom, and second data lines 14 connected to a data driver 12 on the top. (Ex. 1006, Kim, Col.

3:26-37, Col. 4:28-51, FIG. 5). I note that Figure 5 of Kim shows the Odd Row/Even Row configuration that is virtually identical to the one shown in Figures 5A and 5B of the '550 Patent.

Kim Fig. 5



61. In the prosecution history, I did not find any argument by the applicants disputing the Examiner's position that Kim disclosed ***all elements*** of the rejected claim, including the Odd Row/Even Row configuration and gate driver**s**. Rather, the applicants distinguished the rejected claim over Kim by including an additional claim limitation, namely that "the first data lines and the second data lines of each group of data lines are connected with the same source driver." (Ex. 1005, pp. 152, 156). The claim was subsequently allowed by the Examiner.

62. Even though Figure 5 of Kim does not disclose "the same source driver" limitation, the technique of connecting first and second data lines of each group of data lines with the same source driver in an LCD device was well known in the prior art, including the Sharp Reference and Shimada as discussed below. I understand that none of the Sharp Reference, Shimada, and Kamizono referred to in this declaration was considered by the Examiner during prosecution of the '550 Patent.

CLAIM CONSTRUCTION

63. I understand that in *inter partes* review proceedings, patent claims are to be given their "broadest reasonable" construction in light of the specification as would be read by a person of ordinary skill in the art.

64. Most of the terms of Claims 1-5 of the '550 Patent are clear to me, except for the following terms.

"The first and the second date lines of the first group of date lines"

65. Independent Claims 1 and 2 each recite that "the first and the second **date lines** of the first group of **date lines** are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column . . . ." (Ex. 1001, '550 Patent, Col. 19:52-56, Col. 20:13-17) (emphasis added). Nowhere else in the '550 Patent is there any mention or discussion of "date lines." I believe that the term "date lines" in this claim recitation is meant to be "data lines."

"Gate lines . . . insulated with each other" and "data lines . . . insulated with each other"

66. Independent Claims 1 and 2 each recite "a group of N gate lines . . . **insulated with each other**" and "M groups of data lines . . . **insulated with each other**." (Ex. 1001, '550 Patent, Col. 19:44-45, 51-52, Col. 20:5-6, 12-13) (emphasis added). The '550 Patent does not explain what "insulated with each other" means. Rather, the specification uses the same phrase "insulated with each other" when describing the data lines 111 and gate lines 121 shown in the "Prior Art" in Figures 1A and 1B of the '550 Patent (*id.* at Col. 1:45-47), as well as the data lines (D_1, $D_{1'}$, D_2, $D_{2'}$) and the gate lines (G_1, G_2, G_3) shown in Figures 4A-4C of the First Embodiment. (*Id.* at Col. 8:20-22, 29-31).

67. I believe that "insulated with each other" means "spaced apart from and parallel to each other." This is consistent with Figures 1A-1B of the "Prior Art" in the '550 Patent, which show that the data lines 111 are spaced apart from and parallel to each other (thereby "insulated with each other") and the gate lines 121 are likewise spaced apart from and parallel to each other (thereby "insulated with each other"). This is also consistent with all of the figures that describe the First Embodiment of the '550 Patent (e.g., Figs 4A-4C, 5A-5B, 6A-6B), which also show that the data lines (e.g., D_1, $D_{1'}$, D_2, $D_{2'}$) are spaced apart from and parallel to each other (thereby "insulated with each other"), and the gate lines (e.g., G_1, G_2, G_3) are spaced apart from and parallel to each other (thereby "insulated with each other").

"the gate drivers" and the "source drivers"

68. Independent Claims 1 and 2 refer to "gate lines connected to the ***gate drivers***" and "data lines connected to the ***source drivers***." However, the term "source driver" is not mentioned in the specification of the '550 Patent. Rather, the specification refers to "data drivers."

69. Using the broadest reasonable construction, I believe that a person of ordinary skill in the art would construe these terms as written in the plural form, that is, "the gate drivers" refer to more than one gate driver and "the source drivers" refer to more than one source driver.

70. However, the specification, drawings, and prosecution history of the '550 Patent use the terms "source drivers" and "gate drivers" to cover a variety of driving circuits and configurations known at the time of the invention. These are discussed below:

1. "Gate Drivers" and "Source Drivers" May Refer to Multiple Driving Circuits

71. In the certain figures in the '550 Patent, the "gate drivers" and "source drivers" are used to refer to multiple driving circuits, as shown in the "Prior Art" (e.g., Fig. 1A of the '550 Patent). As shown in Figure 1A, the "gate driver" and "source driver" each comprise multiple driver circuits (e.g., integrate circuit (IC) chips in the purple and orange boxes).

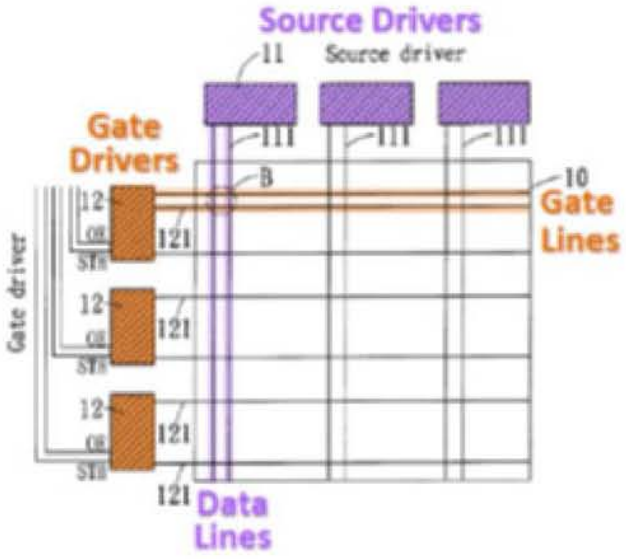


Fig. 1A (Prior Art)

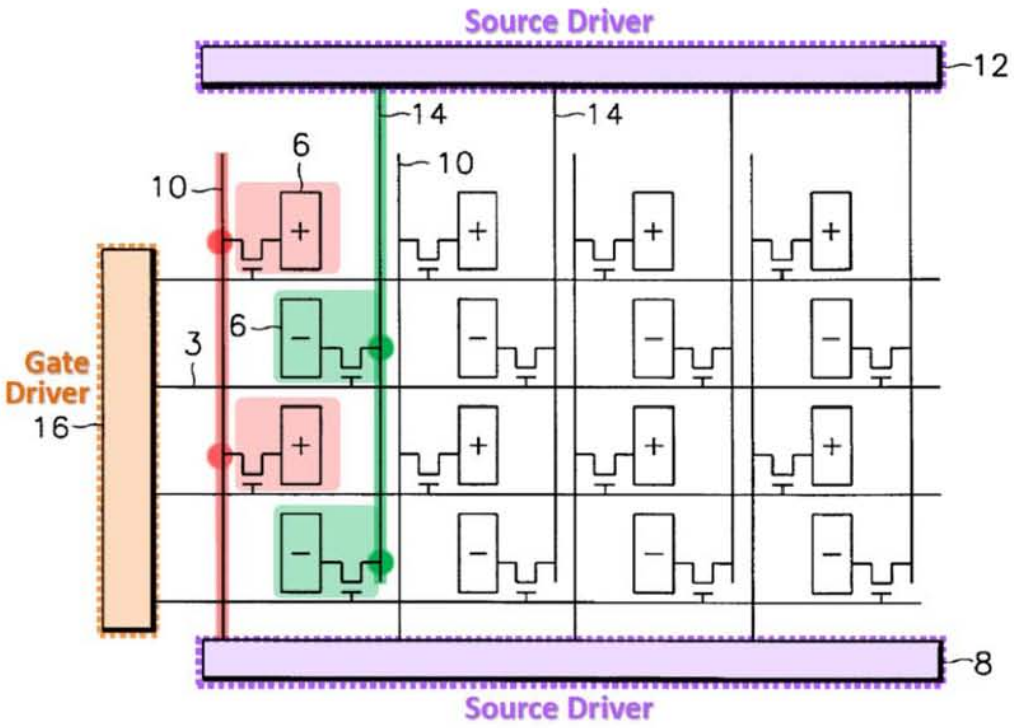
72. At the time that the '550 Patent was filed, it was widely known that such drivers could be implemented using multiple IC chips. Specifically, as LCD displays increase in size with the increased number of pixels, the number of gate lines and data lines likewise increases. However, it becomes difficult, from a packaging and cost perspective, to fabricate a ***single*** chip capable of driving ***hundreds or even thousands*** of data and source lines. Therefore, a person of ordinary skill in the art would use multiple driver IC chips in larger sized LCD panels to keep costs, time and labor down and to simplify packaging.

2. "Gate Drivers" and "Source Drivers" May Refer to A Single Circuit With Multiple Outputs

73. In addition, a person of ordinary skill in the art would understand that "gate drivers" and "source drivers" includes a single circuit (whether an IC or made up of discrete components) having multiple outputs. In that case, a person of ordinary skill in the art would understand that each data or gate line is connected to a separate "driver." This is because

each output provides a unique signal to a data or gate line. This is illustrated, for example, in the Kim reference (Ex. 1006), cited during the prosecution of the '550 Patent (discussed above). As shown below in Figure 5, the gate driver 16 of Kim is depicted as a single circuit block having multiple output lines. The Examiner found that Kim discloses the claimed "gate drivers." (Ex. 1005, p. 141). The applicants did not dispute this. The Examiner and applicants' understanding is consistent with that of a person of ordinary skill in the art at the time of the invention.

Kim Fig. 5



LEVEL OF SKILL IN THE ART

74. A person of ordinary skill in the art would have had an undergraduate degree in electrical engineering, or equivalent work experience. That person would also have had 2

to 5 years of experience designing flat panel display drive electronics, designing active matrices for LCDs, or designing IC drivers.

STATE OF THE ART

75. By the filing date of the '550 Patent in 2004, the LCD display industry had numerous multi-national companies manufacturing LCD displays in volume for various consumer applications like notebook computers, desktop monitors, televisions, pocket entertainment devices, and mobile phones. Competition for market share was fierce, and older LCD issues like limited viewing angle, display brightness, and motion blur were incrementally improved with each product introduction. As the LCD industry grew, so did the support infrastructure for liquid crystal material, substrate glass, polarizer material, backlight modules, light control films, chemicals for color filters, and silicon drive ICs. The LCD manufacturer had multiple supply sources for each of these components.

76. The LCD driver ICs for source and gate drivers were designed by companies in close communication with the panel manufacturers. These ICs use conventional single crystal silicon processing and are manufactured in multiple foundries. The time from driver specification to volume manufacture was on the order of one year. Therefore, panel manufacturers used the ICs that were available at the time of their product introductions.

77. The LCD driver ICs had increasing number of output channels, faster clocking speeds, different logic interfaces, and more features for the display manufacturers. The ICs were sold for COG assembly or Tape Automated Bonding (TAB). The COG method uses an

Anisotropic Conductive Film (ACF) for interconnection between the driver pads and the panel electrodes. The TAB method, along with numerous variations, attaches the driver die to a flexible film with copper traces. The driver outputs are connected to the panel electrodes with ACF, and the logic inputs and power to the driver are connected with ACF or conventional connectors. The display module assembly used COG and TAB extensively since the 1990's. It was also well-known at the time of the filing date of the '550 Patent that an LCD panel must include a glass substrate or other substantially transparent substrate to transmit the light from the backlight to the LCD viewer's eyes. LCD panels modulate the light generated by the backlight assembly and passed through the glass substrate (or other transparent substrate) according to the TFT drive signals. The light exits the LCD surface nearest the viewer and allows the viewer to see the visual image generated based on the electrical input signal.

78. The number and location of source and gate drivers depends on the LCD panel size, pixel size, and other market driven factors. The available drivers could be mounted on a single panel edge or both panel edges. This is true for both the gate axis and the data or source axis. This design change was made as early as the 1970s. When the drivers are attached on opposite panel edges, the interconnection density of connections per linear distance is halved, the driver's power dissipation is spread out, the data clocking rate is halved, peak currents to drivers are distributed more evenly, and the image is more uniform if electrode resistance is an issue across the panel.

79. As of the filing date of the '550 patent, workers in the field of LCD devices were aware of several developments, including:

a. active matrix LCD panels;

b. the Odd Row/Even Row configuration;

c. the use of single or multiple gate drivers and single or multiple source drivers, with the decision to use multiple drivers driven, at least in part, by the size of the LCD panel;

d. the use of chip on glass technology; and

e. the use of integrated driver circuit on glass

SHARP REFERENCE

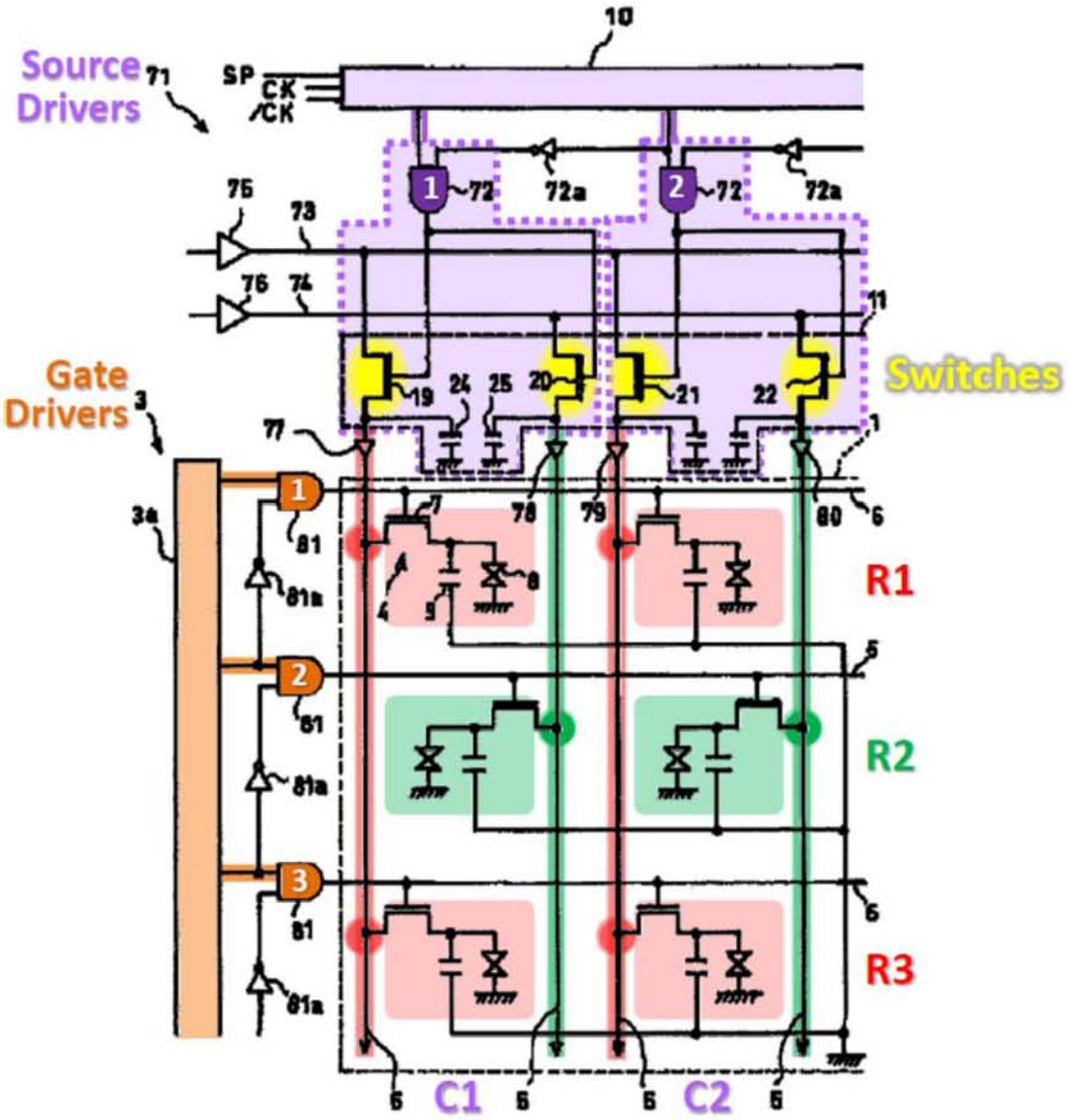
80. The Sharp Reference discloses an LCD device comprising a matrix array of thin film transistors (TFTs) 7, which drive the corresponding array of pixel units 4, as shown below in annotated Figure 10. (Ex. 1002, Sharp Reference, Pars. [0049], [0130], [0140]-[0145], FIG. 10).

81. The Sharp Reference states that its object is to improve image quality by reducing data signal noise and crosstalk (e.g., image blurring) and preventing a "ghost phenomenon" arising from the slow response time. (*Id.*, Par. [0030]).

82. The Sharp Reference also teaches that source driver circuits can be implemented in a certain way (using "driver sample hold method") to solve the problem of

insufficient image data write time arising from increasing the number of pixels in the horizontal scan direction in an LCD panel. (*Id.*, Pars. [0013]-[0019]).

Sharp Reference Fig. 10



83. As shown above in annotated Figure 10, each gate bus line 6 is connected to a gate driver 3. Specifically, each gate bus line 6 is associated with a unique AND circuit 81 (e.g., shaded in orange and labeled as "1"), and gate shift register 3a. In this way, each

gate bus line 6 is individually driven by the output of the unique AND circuit 81. (*Id.*, Pars. [0142]-[0145], FIG. 10).

84. I believe that under the broadest reasonable construction discussed above, a person of ordinary skill in the art would have understood that Figure 10 of the Sharp Reference explicitly shows multiple gate drivers. Specifically, I believe that each gate driver includes gate shift register 3a and an AND circuit 81 connected to an individual gate line 6 because they operate together to generate a non-overlapping gate pulse for each gate line 6. The first gate driver is the AND circuit "1" in communication with shift register 3a; the second gate driver is the AND circuit "2" in communication with shift register 3a; and the third gate driver is the AND circuit "3" in communication with shift register 3a. (*Id.*).

85. Annotated Figure 10 also shows groups of source bus lines 5 connected to the source drivers 71.

86. I believe that under the broadest reasonable construction discussed above, a person of ordinary skill in the art would have understood that Figure 10 of the Sharp Reference explicitly shows multiple source drivers. Specifically, I believe that each source driver includes source shift register 10, AND circuit 72, data signal lines 73, 74, sampling switches 19, 20 (or 21, 22), and sampling capacitors 24, 25 (or 26, 27). The first source driver includes AND circuit 72 (labeled "1") in communication with shift register 10, data signal lines 73, 74, sampling switches 19, 20, and sampling capacitors 24, 25. The second source driver includes AND circuit 72 (labelled "2") in communication with shift register 10,

sampling switches 21 and 22, and sampling capacitors (not numbered). (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], [0145], FIG. 10).

87. As shown above in annotated Figure 10, each set of first source bus line 5 (red) and second source bus line 5 (green) in each column (e.g., C1, C2) is associated with a unique AND circuit 72 (e.g., shaded in purple and labeled as "1" and "2"). This unique AND circuit 72 operates with the associated circuit elements, i.e., source shift register 10, and a unique set of sampling switches (e.g., 19, 20) and sampling capacitors (e.g., 24, 25) to drive the first and second source bus lines (red and green lines) in each group of source bus lines 5. (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], [0145], FIG. 10).

88. For example, for the first source driver in the first column C1, the AND circuit 72 obtains the output of the source shift register 10 and inputs its logical product to the gate terminals of the sampling switches 19 and 20. Meanwhile, data signals from the data signal lines 73 and 74 are respectively input to the source terminals of the sampling switches 19 and 20, and their outputs are respectively held in the sampling capacitors 24 and 25. These held output signals are then input to the first and second source bus lines 5 on both sides of pixel units 4 in the first column C1. For the second source driver in the second column C2, the AND circuit 72 obtains the output of the source shift register 10 and inputs its logical product to the gate terminals of the sampling switches 21 and 22. Meanwhile, data signals from the data signal lines 73 and 74 are respectively input to the source terminals of the sampling switches 21 and 22, and their outputs are respectively held in the sampling

capacitors (not numbered). These held output signals are then input to the first and second source bus lines 5 on both sides of pixel units 4 in the second column C2. (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], [0145], FIG. 10). In this way, each set of first and second source bus lines 5 associated with each column of pixel units 4 are individually driven by a separate source driver. Accordingly, I believe that the Sharp Reference explicitly teaches multiple source drivers.

89. The Sharp Reference also teaches that the gate bus lines 6 are spaced apart from and parallel to each other (i.e., insulated with each other), and that the source bus lines 5 are likewise spaced apart from and parallel to each other (i.e., insulated with each other). (*Id.*, FIG. 10).

90. As shown above in annotated Figure 10, each gate bus line 6 is connected with the gates of all of the TFTs 7 in the row associated with that gate bus line. For example, the first gate line 6 is connected with the gates of all of the TFTs 7 of the first row (R1), the second gate line 6 is connected with the gates of all of the TFTs 7 of the second row (R2), etc. (*Id.*, Par. [0143], FIG. 10).

91. Annotated Figure 10 above also shows the claimed Odd Row/Even Row configuration. In this regard, the first source bus line 5 (red line) and the second source bus line 5 (green line) in each group of data bus lines are respectively connected with the sources of all of the TFTs 7 of the **odd rows** (red boxes in R1 and R3) and **even rows**

(green boxes in R2) of the column (C1, C2) associated with that group of source bus lines, as required by all Claims of the '550 Patent.

92. For example, the first source bus line 5 (red line) of the first group is connected with the sources (red dots) of the TFTs 7 of the first row and third row (see the red boxes in R1 and R3) in the first column C1, while the second source bus line 5 (green line) of the first group is connected with the sources (green dot) of the TFT 7 of the second row (green box in R2) in the first column C1. (*Id.*, Pars. [0131]-[0140], [0145], FIG. 10). The same Odd Row/Even Row configuration is provided in each column (e.g., C2).

93. The benefits of the Odd Row/Even Row configuration were already well known in the prior art, including the Sharp Reference. The Sharp Reference teaches that the Odd Row/Even Row configuration in an LCD Panel prevents adjacent pixel TFTs 7 in the column direction from being turned on simultaneously. This reduces the effect of data signal noise and therefore improves the video quality of the LCD panel. (*Id.*, Pars. [0144]-[0145], [0030]).

94. In this regard, I believe that the benefits of using the Odd Row/Even Row configuration became particularly significant as the size of the LCD panel and/or the number of pixels increased. When LCD screens became large enough to compete against the conventional cathode ray tube (CRT) screens, there was market and design need to improve the video quality of LCD panels. But this required increased number of pixels in an LCD panel and at the same time, a faster way to drive these pixels accurately. The Odd

Row/Even Row configuration was one of the various techniques developed in the prior art to meet this need.

95. As shown in Figure 10, the source drivers 71 for all source bus lines 5 are installed on the same side (e.g., upper side) of the display panel.

96. Figure 10 also shows that the first and the second source bus lines 5 (the red and green lines) in each group of source bus lines are connected with the same source driver. (*Id.*, Pars. [0131]-[0140], FIG. 10).

97. The transfer of data signals from the data signal lines 73, 74 to the first and the second source bus lines 5 (the red and green lines) is switched by sampling switches 19, 20 (or 21, 22) (highlighted in yellow). (*Id.*, Pars. [0134]-[0135], [0137]-[0139], FIG. 10).

THE SHARP REFERENCE ANTICIPATES CLAIMS 1-3

98. As discussed below, I believe that the Sharp Reference explicitly discloses each and every element of Claims 1-3 of the '550 Patent.

99. As shown below in annotated Figure 10, the Sharp Reference teaches an LCD device comprising a matrix array of thin film transistors (TFTs) 7, which drive the corresponding array of pixel units 4. (*Id.*, Pars. [0049], [0130], [0140]-[0145], FIG. 10).

THE SHARP REFERENCE DISCLOSES MULTIPLE GATE DRIVERS

100. As explained above in paragraph 84, I believe that Figure 10 of the Sharp Reference explicitly discloses multiple gate drivers.

101. As shown in Figure 10, gate lines 6 are connected to the corresponding gate drivers 3, as required by Claims 1 and 2.

102. Each gate driver comprises gate shift register 3a, and AND circuit 81. (*Id.*, Pars. [0142]-[0145], FIG. 10).

THE SHARP REFERENCE DISCLOSES MULTIPLE SOURCE DRIVERS

103. As explained above in paragraphs 86-88, Figure 10 also explicitly discloses multiple source drivers.

104. As shown in Figure 10, groups of data lines 5 are connected to the corresponding source drivers 71.

105. Each source driver comprises source shift register 10, AND circuit 72, data signal lines 73, 74, sampling switches 19, 20 (or 21, 22), and sampling capacitors 24, 25 (or 26, 27). (Ex. 1002, Sharp Reference, Pars. [0131]-[0139], FIG. 10).

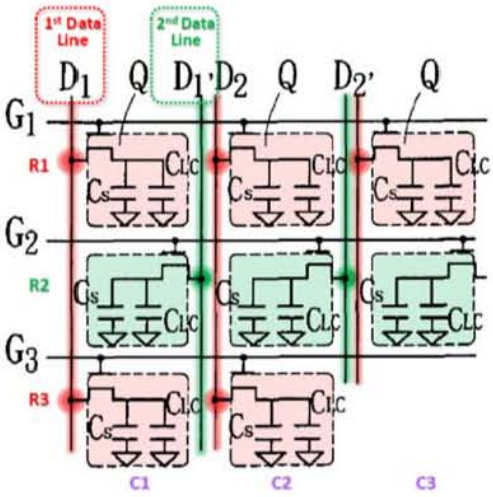
THE SHARP REFERENCE DISCLOSES THAT FIRST AND SECOND DATA LINES IN EACH GROUP OF DATA LINES ARE CONNECTED WITH THE SAME SOURCE DRIVER

106. As required by Claims 1-2, annotated Figure 10 of the Sharp Reference shows that the first and second data lines (e.g., red and green lines 5) in each group of data lines are connected with the ***same*** source driver (e.g., source driver in purple comprising source shift register 10, AND circuit 72, data signal lines 73, 74, sampling switches 19, 20 (or 21, 22), and sampling capacitors 24, 25 (or 26, 27)). (*Id.*, Pars. [0131]-[0140], FIG. 10). As discussed above, during prosecution, Claim 1 of the '550 Patent was allowed over Kim based on this feature.

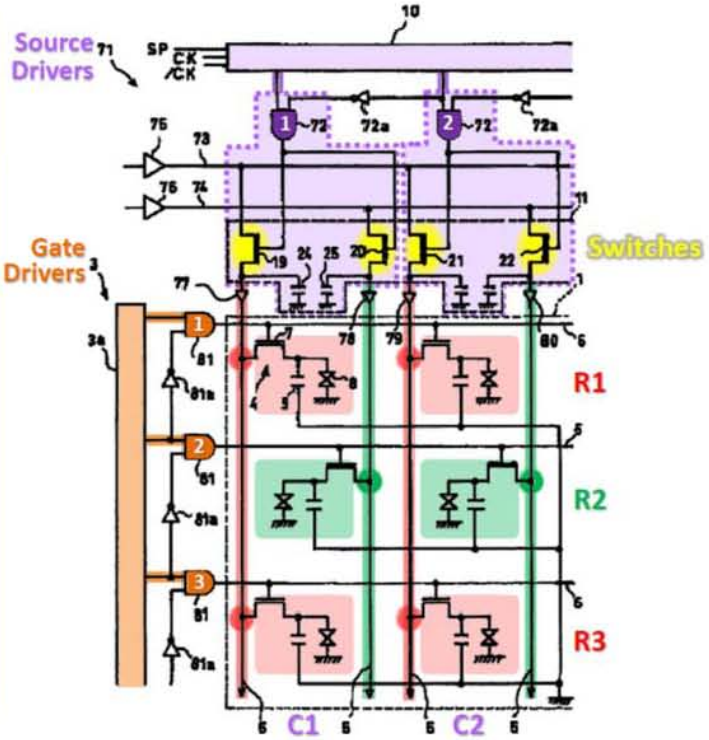
THE SHARP REFERENCE DISCLOSES THAT DATA LINES/GATE LINES ARE INSULATED WITH EACH OTHER

107. As explained above, Figure 10 of the Sharp Reference also shows that the gate lines 6 are "insulated with each other" under the broadest reasonable construction of this term since they are spaced apart from and parallel to each other; and the data lines 5 are likewise insulated with each other as they are spaced apart and parallel to each other. (Ex. 1002, Sharp Reference, FIG. 10). Indeed, the spacing (insulation) between the data and gate lines in the Sharp Reference and the '550 Patent is virtually identical, as shown below in the side-by-side comparison of Figure 4B of the '550 Patent and Figure 10 of the Sharp Reference.

'550 Patent Fig. 4B



Sharp Reference Fig. 10



THE SHARP REFERENCE TEACHES THE ODD ROW/EVEN ROW CONFIGURATION

108. The claimed Odd Row/Even Row configuration of the '550 Patent (shown on the left) is present in the LCD device of the Sharp Reference (shown on the right). (*Id*., Pars. [0144]-[0145], FIG. 10). Specifically, the first data line 5 (see the red line) is connected to the sources (red dots) of the TFTs (red boxes) in the odd rows (R1 and R3). The second data line 5 (green line) is connected to the sources (green dot) of the TFTs (green boxes) in the even rows (R2). Figure 4B of the later '550 Patent (shown on the left) has the exact same Odd Row/Even Row configuration.

THE SHARP REFERENCE DISCLOSES THAT EACH SOURCE DRIVER IS INSTALLED ON THE SAME SIDE OF THE DISPLAY PANEL

109. Figure 10 of the Sharp Reference also shows that each source driver (e.g., source drivers in purple) is installed on the same side (e.g., upper side) of the display panel (Ex. 1002, Sharp Reference, Pars. [0130]-[0140], FIG. 10), as required by Claim 2.

THE SHARP REFERENCE DISCLOSES SWITCHES FOR DATA TRANSFER

110. Figure 10 of the Sharp Reference shows that data transfer is switched by each sampling switch 19, 20, 21, 22 (*id*., Pars. [0134]-[0135], [0137]-[0139], FIG. 10), as required by Claim 2.

THE SHARP REFERENCE DISCLOSES A SPACE BETWEEN NEIGHBORING DATA LINES TO PREVENT SHORT CIRCUITING

111. Claim 3, which depends from Claim 2, recites that "there is a space [i.e., a gap] between the neighboring data lines to prevent them from short circuit." Figure 10 of

the Sharp Reference clearly shows a space between the neighboring data lines 5 that prevents short circuiting.

112. Just like in Figure 4B of the '550 Patent, Figure 10 shows that the first data line 5 (red) is on the left side of the pixel TFTs in the first column (C1), and the second data line 5 (green) is on the right side of the pixel TFTs in the first column (C1). This space prevents short circuiting between the first and second data lines.

113. When two neighboring data lines are shown to be spaced apart from each other in the schematic circuit diagrams for an LCD driving device, such as Figure 10 of the Sharp Reference or Figure 4B of the '550 Patent, I expect that there is a sufficient space between these data lines to prevent short circuiting. Otherwise, the LCD driving device would not be operating as described in the reference.

SHARP REFERENCE DISCLOSES EACH AND EVERY ELEMENT OF CLAIMS 1-3

114. The following claim charts summarize where I believe each element of Claims 1-3 is taught by the Sharp Reference:

The Claims Of The '550 Patent	Sharp Reference
1. A liquid crystal display driving device of matrix structure type including:	Sharp Reference discloses a liquid crystal display driving device of matrix structure type (Ex. 1002, Sharp Reference, Pars. [0001]-[0003], [0130], FIG. 10).
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels	Sharp Reference discloses a group of thin film transistors 7 with matrix array consisting of n (e.g., 3) rows and m (e.g., 2) columns of thin film transistors 7, wherein each thin film transistor can drive one pixel unit 4 so that n×m

The Claims Of The '550 Patent	Sharp Reference
can be driven;	(e.g., 3×2) of pixel units can be driven (Ex. 1002, Sharp Reference, Pars. [0049], [0130], [0140]- [0145], FIG. 10).
a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	Sharp Reference discloses a group of n (e.g., 3) gate bus lines 6 connected to the gate drivers 3. The first gate driver is the AND circuit "1" in communication with shift register 3a; the second gate driver is the AND circuit "2" in communication with shift register 3a; and the third gate driver is the AND circuit "3" in communication with shift register 3a. The gate lines are insulated with each other by being spaced apart from and parallel to each other. The first gate bus line 6 is connected with the gates of all the thin film transistors 7 of the first row. The second gate bus line 6 is connected with the gates of all the thin film transistors 7 of the second row . . . and the n^{th} (e.g., 3^{rd}) gate bus line 6 is connected with the gates of all the thin film transistors 7 of the n^{th} (e.g., 3^{rd}) row (Ex. 1002, Sharp Reference, Pars. [0142]-[0145], FIG. 10).
M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines	Sharp Reference discloses m (e.g., 2) groups of source bus lines 5 connected to the source drivers 71. The first source driver includes AND circuit 72 (labeled "1") in communication with shift register 10, data signal lines 73, 74, sampling switches 19, 20, and sampling capacitors 24, 25. The second source driver includes AND circuit 72 (labelled "2") in communication with shift register 10, sampling switches 21 and 22, and sampling capacitors (not numbered). The groups of data lines are insulated with each other by being spaced apart from and parallel to each other. The first and the second source bus lines 5 of the first group of source bus lines are respectively connected

The Claims Of The '550 Patent	Sharp Reference
are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column, and	with the sources of all the thin film transistors 7 of the odd and the even rows of the first column. . . . The first and the second source bus lines 5 of the m^{th} (e.g., 2^{nd}) group of source bus lines are respectively connected with the sources of the all the thin film transistors 7 of the odd and the even rows of the m^{th} (e.g., 2^{nd}) column (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], [0145], FIG. 10).
the first data lines and the second data lines of each group of data lines are connected with the same source driver.	Sharp Reference discloses that the first source bus lines 5 and the second source bus lines 5 of each group of source bus lines are connected with the same source driver 10, 72, 73, 74, 19, 20, 24, 25 (or 10, 72, 73, 74, 21, 22, 26, 27) (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], FIG. 10).
2. The liquid crystal display device of matrix structure type including:	See Claim 1 above.
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels can be driven;	See Claim 1 above.
a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	See Claim 1 above.
M groups of data lines connected to the source drivers and insulated with	See Claim 1 above.

The Claims Of The '550 Patent	Sharp Reference
each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column,	
wherein the first data lines and the second data lines of each group of data lines are connected with the same source driver,	See Claim 1 above.
each source driver is installed on the same side of the display panel and	Sharp Reference discloses that the first source driver(AND circuit 72 (labeled "1") in communication with shift register 10, data signal lines 73, 74, sampling switches 19, 20, and sampling capacitors 24, 25) and the second source driver (AND circuit 72 (labelled "2") in communication with shift register 10, sampling switches 21 and 22, and sampling capacitors (not numbered)) are installed on the same side (e.g., upper side) of the display unit 1 (Ex. 1002, Sharp Reference, Pars. [0130]-[0140], FIG. 10).
the data transfer is switched by an electronic switch.	Sharp Reference discloses that the data transfer is switched by each sampling switch 19, 20, 21, 22 (Ex.1002, Sharp Reference, Pars. [0134]-[0135], [0137]-[0139], FIG. 10).
3. The liquid crystal display driving	Sharp Reference discloses that there is a space

The Claims Of The '550 Patent	Sharp Reference
device of matrix structure type as claimed in claim 2, wherein there is a space between the neighboring data lines to prevent them from short circuit.	between the neighboring data lines 5. These spaces prevent the data lines from short circuiting. (Ex. 1002, Sharp Reference, FIG. 10).

115. Accordingly, it is my opinion that Claims 1-3 of the '550 Patent are anticipated by the Sharp Reference.

THE SHARP REFERENCE RENDERS CLAIMS 1-3 AND 5 OBVIOUS TO A PERSON OF ORIDNARY SKILL IN THE ART

116. As discussed above, it is my opinion that the Sharp Reference explicitly discloses each and every element of Claims 1-3 of the '550 Patent, including the claimed source and gate drivers, and thus anticipates Claims 1-3.

117. I believe that no reasonable person of ordinary skill in the art would have interpreted the Sharp Reference as disclosing only a single source driver and a single gate driver in Figure 10.

118. Even under such a tenuous and narrow interpretation of the Sharp Reference, I believe that Claims 1-3 would be obvious to a person of ordinary skill in the art.

THERE IS NO UNEXPECTED RESULT FROM USING MULTIPLE SOURCE AND GATE DRIVERS IN AN LCD PANEL INSTEAD OF A SINGLE SOURCE DRIVER AND A SINGLE GATE DRIVER

119. I understand that one way of demonstrating obviousness in the situation where a prior art reference discloses a single element but the claim requires multiple

elements is to demonstrate that there are no new and unexpected results from increasing the number of such elements.

120. The duplication of the source and gate drivers shown in Figure 10 of the Sharp Reference simply allows more pixels to be added when increasing the size of the LCD panel. The addition of source and gate drivers would not change the way the LCD Panel of the Sharp Reference operates in the Odd Row/Even Row configuration. Accordingly, no unexpected results would be produced from duplicating the source and gate driver circuits (i.e., adding more drivers) shown in Figure 10 of the Sharp Reference.

121. The prior art was abundant with examples of larger sized LCD panels using multiple source and gate drivers. In fact, when I was working in the LCD industry prior to the filing date of the '550 Patent, it was a routine industry practice to change the panel design to increase the size of the panel and/or the number of pixels by simply adding more driver ICs. For example, while the ***small***, low cost LCD panel (which had an equivalent pixel dimension of 7×4) that I worked on at Alien Technology had only a single source driver and a single gate driver, the ***large sized*** LCD panels (which had pixel dimension of at least 800×600) that I worked on at Philips used multiple driver ICs. Using additional source and gate drivers in connection with increasing the size of the panel or the number of pixels in an LCD panel was a well-known and readily available design option.

122. Consistent with my experience and as discussed above, the prior art reference (Ex. 1009) states that "in order to drive many gate bus lines and the source bus

lines on the display circuit board, ***a plurality of the gate drivers and source drivers must*** be connected to the area around the liquid crystal display panel." (*Id.*, Par. [0006]) (emphasis added). Sekido further teaches that increasing the size of the LCD screen will increase the number of the driver ICs. (*Id.*, Par. [0008]).

123. As explained in the Sharp Reference, its use of the Odd Row/Even Row configuration improves the image quality of an LCD panel with the increased number of pixels by reducing the effect of data signal noise. (Ex. 1002, Sharp Reference, Pars. [0144]-[0145], [0030]).

124. Hence, I believe that duplication of source and gate drivers for a larger sized LCD device would have involved only routine skill in the art and does not produce any unexpected result.

125. The '550 Patent fails to demonstrate or even suggest any new and unexpected results stemming from having more than one source driver circuit and more than one gate driver circuit in the claimed LCD driving device. The '550 Patent includes no explanation of the difference between having a single source driver and a single gate driver and having multiple source and gate drivers in the LCD device.

126. In fact, the '550 Patent interchangeably uses the singular ("source driver"/"gate driver") and plural ("source drivers"/"gate drivers") to describe these components. (*See* Ex. 1001, '550 Patent, Col. 8:21 ("[T]here are N gate lines connected to

gate driver . . . ." (emphasis added)); *see also id.*, Figure 1A and Col. 1:36-45 (using the singular terms "data driver 11" and "gate driver 12")).

127. In addition, during prosecution of the '550 Patent, the applicants did not dispute the Examiner's finding that Figure 5 of Kim (Ex. 1006), which shows a ***single*** block for gate driver 16, meets the gate driver***s*** limitation of Claims 1 and 2. (Ex. 1005, p. 156).

128. Even if, contrary to my opinion, Patent Owner contends that the Sharp Reference does not disclose the claimed "source drivers" and "gate driver," I believe that it would nevertheless have been obvious to a person of ordinary skill in the art to modify the LCD driving device of the Sharp Reference to include additional source and gate driver circuits in addition to what are shown in Figure 10.

129. It is my opinion that at a minimum, Claims 1-3 of the '550 Patent are obvious over the Sharp Reference.

THE SHARP REFERENCE DISCLOSES INTEGRATED GATE DRIVER CIRCUIT

130. Claim 5 requires that the "gate driver is an integrated gate driver circuit installed on glass." However, this would have also been obvious in view of the Sharp Reference.

131. The Sharp Reference teaches that the gate driver, the source driver, and the display unit consisting of a plurality of pixel units in an LCD device can be formed monolithically on the same substrate in an LCD panel to "to improve the drive force of the pixel transistor that accompanies larger screen size, and to reduce the drive IC mounting

costs and the like." (Ex. 1002, Sharp Reference, Claim 6, Pars. [0160], [0172]-[0173], [0008], [0020], [0036], [0045]). Since the gate drivers are formed monolithically on the same substrate as the pixel TFTs, the result is an integrated gate driver circuit installed on the same substrate as the pixel TFTs.

132. Moreover, It was well-known at the time of the filing date of the '550 Patent that an LCD panel must include a glass substrate or other substantially transparent substrate to transmit the light from the backlight to the LCD viewer's eyes. LCD panels modulate the light generated by the backlight assembly and passed through the glass substrate (or other transparent substrate) according to the TFT drive signals. The light exits the LCD surface nearest the viewer and allows the viewer to see the visual image generated based on the electrical input signal.

133. The use of a glass substrate was the preferred choice, especially in an LCD panel having a large number of pixels. Compared to other transparent materials, glass is cheaper, provides a smoother surface, and is also more resistant to a high temperature required for processing TFTs in an LCD panel. In addition, a glass substrate protects liquid crystal materials and TFTs in the LCD panel from moisture. In my experience, LCD panels with a large number of pixels using TFTs all included glass substrates.

134. Thus, I believe that it would have been obvious to a person of ordinary skill in the art that the integrated gate driver circuit taught by the Sharp Reference is installed on a glass substrate in an LCD panel since the use of glass substrate is one of small number of

widely known design options for an LCD panel having the light transmitted from the backlight. Since this technology was widely understood and available at the time the '550 Patent was filed, I believe that a person of ordinary skill in the art would have been successful in forming an integrated gate driver circuit on a glass substrate.

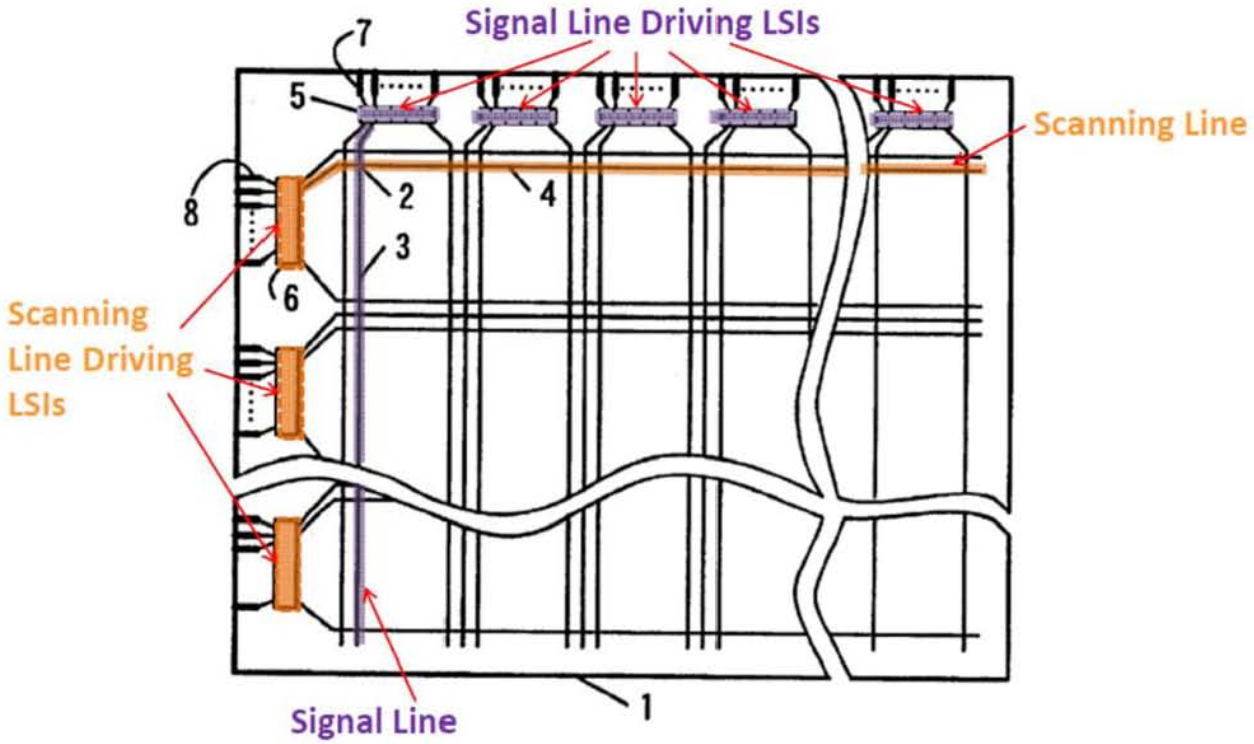
135. Accordingly, it is my opinion that Claim 5 of the '550 Patent is also obvious over the Sharp Reference.

KAMIZONO

136. Kamizono describes an active matrix LCD for a video monitor such as a television receiver or a computer display, and teaches fabricating circuits that are suitable for a large sized LCD panel. (Ex. 1004, Kamizono, Abstract, Col. 1:5-7, Col. 3:1-36).

137. As shown below in annotated Figure 15, Kamizono teaches an LCD panel 1 having data lines ("signal lines 3") connected to multiple source driver ICs ("signal line driving LSIs 5") and gate lines ("scanning lines 4") connected to multiple gate driver ICs ("scanning line driving LSIs 6"). A pixel is located at the intersection 2 between a data line 3 and a gate line 4. The pixels are arranged in the image display region of the LCD panel, while the driving LSIs are arranged in the non-image display region of the panel. (*Id.*, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15). The source driver ICs 5 send data signals to operate TFTs and pixels via data lines 3, while the gate driver ICs 6 send voltage pulse to the gates of TFTs via gate lines 4.

Kamizono Fig. 15



138. Kamizono further teaches that while a "small sized" LCD panel has "a few (2 or 3) of the [driving] LSIs," a "large-screen" LCD panel uses more driving LSIs, such as 4 or 5 scanning line driving LSIs and 10 or more signal line driving LSIs. (*Id.*, Col. 9:19-20, Col. 11:53-64, FIGS. 5, 9, and 15).

139. Kamizono also teaches that for an LCD device having an "increased screen size," these multiple source or gate drivers ("liquid crystal driving LSIs") are commonly mounted as a semiconductor chip by a chip-on-glass (COG) method or a tape automated bonding (TAB) method. According to Kamizono, the COG method is preferred over the TAB

method because of the operational reliability and reduction of the overall product size provided by the COG method, which is consistent with my experience. (*Id.*, Col. 1:12-58).

140. I understand chip-on-glass (COG) to be a method of attaching single-crystal silicon die or Large Scale Integrated (LSI) circuits directly on the glass substrate of the LCD panel. The benefits of using COG are increased reliability, smaller LCD module size, and less weight. The silicon die are designed and fabricated by conventional silicon wafer processes. The die are electrically connected to the panel either through wire bonding or using Anisotropic Conductive Film (ACF). ACF is a type of plastic that contains metalized spheres. The density of the spheres in the film prevents adjacent sphere to sphere connection but connects the die output pads to the panel electrode pads through the thin plastic film.

141. Kamizono further teaches that an LCD panel 1 can be a poly-Silicon TFT panel and the source and gate drivers can be mounted on the panel in the non-image display area of the panel ("a spare area other than a display area of the liquid crystal panel 1"). (*Id.*, Col. 13:50-55). Since the gate drivers are formed on the same substrate as the pixel TFTs, the result is integrated gate driver circuit installed on the same substrate as the pixel TFTs.

CLAIMS 1-5 ARE OBVIOUS OVER THE SHARP REFERENCE IN VIEW OF KAMIZONO

142. I reiterate my opinion discussed above that the Sharp Reference expressly discloses each and every element of Claims 1-3, including the claimed source and gate drivers, and thus anticipates Claims 1-3.

143. Again, to the extent that the Patent Owner argues that the Sharp Reference discloses only a single source driver and a single gate driver in Figure 10, no reasonable person of ordinary skill in the art would agree.

MODIFICATION OF THE LCD DRIVING DEVICE OF THE SHARP REFERENCE TO INCLUDE MULTIPLE SOURCE AND GATE DRIVERS OF KAMIZONO WOULD HAVE BEEN WITHIN THE SKILL OF A PERSON OF ORDINARY SKILL IN THE ART AND WOULD HAVE PRODUCED NO UNEXPECTED RESULT

144. Kamizono teaches the use of multiple source driver ICs 5 and multiple gate driver ICs 6 to send signals through data lines and gate lines in an LCD device. Indeed, Figure 15 of Kamizono is virtually identical to Figure 4A of the '550 Patent.

145. For the reasons discussed below, it is my opinion that even under such a misreading of the Sharp Reference, it would still have been obvious to a person of ordinary skill in the art to combine the teachings of the Sharp Reference and Kamizono to arrive at the LCD driving device of Claims 1-5 of the '550 Patent.

146. The Sharp Reference and Kamizono are in the same field of LCD display technology. They both disclose active matrix LCD devices and are both directed to improving the performance of a large sized LCD panel. The Sharp Reference teaches that source drivers can be implemented in a certain way (e.g., using "driver sample hold

method") to solve the problem of insufficient image data write time arising from increasing the number of pixels in in an LCD panel. (Ex. 1002, Sharp Reference, Pars. [0013]-[0019]). Kamizono teaches that a "large-screen" LCD panel uses more source and gate driver LSIs than a "small sized" LCD panels would use. (Ex. 1004, Kamizono, Col. 9:19-20, Col. 11:53-64, FIGS. 5 and 9). Because both references addressed the same design needs for larger sized LCD panels, I believe that a person of ordinary skill in the art making the source and gate driving circuit for a large-screen LCD panel would have been motivated to combine the teachings of the Sharp Reference and Kamizono.

147. The technique of using multiple gate and source drivers has been used to improve Kamizono's larger sized LCD panels. The source drivers and the Odd Row/Even Row configuration taught in the Sharp Reference also improve the larger sized LCD panels. Hence, a person of ordinary skill in the art would recognize that Kamizono's technique would improve similar devices, such as larger sized LCD panels of the Sharp reference, in the same way. In my opinion, using multiple source and gate driver ICs as taught in Kamizono in the LCD panel of the Sharp Reference is well within the level of ordinary skill in the art, particularly since Figure 10 of the Sharp Reference is configured to have separate circuitry drive data through each gate line and each pair of data lines and Kamizono likewise shows separate circuit (i.e., source drivers 5 and data drivers 6).

148. Based on my experience and knowledge, I believe that modifying the LCD driving device of the Sharp Reference to include the multiple source and gate driver ICs of

Kamizono would not produce unexpected result, but would merely lead to a predictable result, since such a modification simply allows more pixels to be added to increase the size of the LCD panel without changing the way LCD Panel operates.

149. Kamizono teaches the use of multiple source and gate drivers (as does the Sharp Reference), and the Sharp Reference discloses all of the other limitations of Claims 1-3, as shown in the claim charts provided above. Moreover, for the reasons discussed above, there was a clear motivation to combine these references. Thus, to the extent that the Patent Owner argues that the Sharp Reference does not teach multiple source and gate drivers, which is contrary to my opinion discussed above, I believe that, at a minimum, Claims 1-3 of the '550 Patent would be obvious over the Sharp Reference in view of Kamizono.

KAMIZONO DISCLOSES A CHIP ON GLASS

150. Dependent Claim 4 requires that the gate driver is a chip installed on glass.

151. Kamizono teaches that the use of a chip-on-glass is the preferred way of implementing the gate drivers for a large sized LCD panel. (Ex. 1004, Kamizono, Col. 1:12-58).

152. Based on my experience and knowledge, I believe that using the chip on glass of Kamizono for the gate driver in the LCD device of the Sharp Reference would not produce any unexpected result and would not affect, for example, the Odd Row/Even Row configuration in the LCD device of the Sharp Reference.

153. Based on my experience and knowledge, I believe that a person of ordinary skill in the art would recognize that Kamizono's technique of using a chip on glass for the gate driver to improve a large screen LCD panel (e.g., increasing the operational reliability and reducing the overall product size--see Ex. 1004, Kamizono, Col. 1:12-58) can be also used to improve the large screen LCD panel of the Sharp Reference in the same way.

154. A person of ordinary skill in the art making a large-screen LCD panel would have been motivated to combine the teachings of the Sharp Reference and Kamizono to arrive at Claim 4.

THE SHARP REFERENCE DISCLOSES INTEGRATED GATE DRIVER CIRCUIT

155. Claim 5 requires that the gate driver is an integrated gate driver circuit installed on glass. As discussed above, this would have been obvious in view of the Sharp Reference.

156. The Sharp Reference teaches that the gate driver, the source driver, and the display unit consisting of a plurality of pixel units in an LCD device can be formed monolithically on the same substrate in an LCD panel to "to improve the drive force of the pixel transistor that accompanies larger screen size, and to reduce the drive IC mounting costs and the like." (Ex. 1002, Sharp Reference, Claim 6, Pars. [0160], [0172]-[0173], [0008], [0020], [0036], [0045]). Since the gate drivers are formed monolithically on the same substrate as the pixel TFTs, the result is integrated gate driver circuit installed on the same substrate as the pixel TFTs.

157. Moreover, as discussed above, it was well-known at the time of the filing date of the '550 Patent that an LCD panel must include a glass substrate or other substantially transparent substrate to transmit the light from the backlight to the LCD viewer's eyes. LCD panels modulate the light generated by the backlight assembly that passes through the glass substrate (or other transparent substrate) according to the TFT drive signals. The light exits the LCD surface nearest the viewer and allows the viewer to see the visual image generated based on the electrical input signal.

158. Again, the use of a glass substrate was the preferred choice, especially in an LCD panel having a large number of pixels. Compared to other transparent materials, glass is cheaper, provides a smoother surface, and is also more resistant to a high temperature required for processing TFTs in an LCD panel. In addition, a glass substrate protects liquid crystal materials and TFTs in the LCD panel from moisture. In my experience, LCD panels with a large number of pixels using TFTs all included glass substrates.

159. Thus, I believe that it would have been obvious to a person of ordinary skill in the art that the integrated gate driver circuit taught by the Sharp Reference is installed on a glass substrate in an LCD panel since the use of glass substrate is one of small number of widely known design options to make an LCD panel and to have the light transmitted from the backlight.

THE COMBINATION OF THE SHARP REFERENCE AND KAMIZONO TEACHES ALL ELEMENTS OF CLAIMS 1-5

160. The following claim charts summarize where I believe each element of Claims 1-5 is taught by the combination of the Sharp Reference and Kamizono:

The Claims Of The '550 Patent	Sharp Reference in View of Kamizono
1. A liquid crystal display driving device of matrix structure type including:	Sharp Reference discloses a liquid crystal display driving device of matrix structure type (Ex. 1002, Sharp Reference, Pars. [0001]-[0003], [0130], FIG. 10).
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels can be driven;	Sharp Reference discloses a group of thin film transistors 7 with matrix array consisting of n (e.g., 3) rows and m (e.g., 2) columns of thin film transistors 7, wherein each thin film transistor can drive one pixel unit 4 so that n×m (e.g., 3×2) of pixel units can be driven (Ex. 1002, Sharp Reference, Pars. [0049], [0130], [0140]- [0145], FIG. 10).
a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	Sharp Reference discloses a group of n (e.g., 3) gate bus lines 6 connected to the gate drivers 3. The gate lines are insulated with each other by being spaced apart from and parallel to each other. The first gate bus line 6 is connected with the gates of all the thin film transistors 7 of the first row. The second gate bus line 6 is connected with the gates of all the thin film transistors 7 of the second row . . . and the n^{th} (e.g., 3^{rd}) gate bus line 6 is connected with the gates of all the thin film transistors 7 of the n^{th} (e.g., 3^{rd}) row (Ex. 1002, Sharp Reference, Pars. [0142]-[0145], FIG. 10). Kamizono discloses scanning lines 4 connected to multiple scanning line driving LSIs 6 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).

The Claims Of The '550 Patent	Sharp Reference in View of Kamizono
M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column, and	Sharp Reference discloses m (e.g., 2) groups of source bus lines 5 connected to the source drivers 71. The groups of data lines are insulated with each other by being spaced apart from and parallel to each other. The first and the second source bus lines 5 of the first group of source bus lines are respectively connected with the sources of all the thin film transistors 7 of the odd and the even rows of the first column. . . . The first and the second source bus lines 5 of the m^{th} (e.g., 2^{nd}) group of source bus lines are respectively connected with the sources of the all the thin film transistors 7 of the odd and the even rows of the m^{th} (e.g., 2^{nd}) column (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], [0145], FIG. 10). Kamizono discloses signal lines 3 connected to multiple signal line driving LSIs 5 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).
the first data lines and the second data lines of each group of data lines are connected with the same source driver.	Sharp Reference discloses that the first source bus lines 5 and the second source bus lines 5 of each group of source bus lines are connected with the same source driver 10, 72, 73, 74, 19, 20, 24, 25 (or 10, 72, 73, 74, 21, 22, 26, 27) (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], FIG. 10).
2. The liquid crystal display device of matrix structure type including:	See Claim 1 above
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels can be driven;	See Claim 1 above
a group of N gate lines connected to	See Claim 1 above

The Claims Of The '550 Patent	Sharp Reference in View of Kamizono
the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	
M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column,	See Claim 1 above.
wherein the first data lines and the second data lines of each group of data lines are connected with the same source driver,	See Claim 1 above
each source driver is installed on the same side of the display panel and	Sharp Reference discloses that the first source driver(AND circuit 72 (labeled "1") in communication with shift register 10, data signal lines 73, 74, sampling switches 19, 20, and sampling capacitors 24, 25) and the second

The Claims Of The '550 Patent	Sharp Reference in View of Kamizono
	source driver (AND circuit 72 (labelled "2") in communication with shift register 10, sampling switches 21 and 22, and sampling capacitors (not numbered)) are installed on the same side (e.g., upper side) of the display unit 1 (Ex. 1002, Sharp Reference, Pars. [0130]-[0140], FIG. 10).
the data transfer is switched by an electronic switch.	Sharp Reference discloses that the data transfer is switched by each sampling switch 19, 20, 21, 22 (Ex.1002, Sharp Reference, Pars. [0134]-[0135], [0137]-[0139], FIG. 10).
3. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein there is a space between the neighboring data lines to prevent them from short circuit.	Sharp Reference discloses that there is a space between the neighboring data lines 5. These spaces prevent the data lines from short circuiting. (Ex. 1002, Sharp Reference, FIG. 10).
4. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein the gate driver is a chip installed on glass.	Kamizono discloses that a liquid crystal driving LSI is commonly mounted as a semiconductor chip by a chip-on-glass (COG) method. (Ex. 1004, Kamizono, Col. 1:12-58).
5. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein the gate driver is an integrated gate driver circuit installed on glass.	Kamizono discloses LCD driving circuits that form an integrated structure with a poly-Silicon TFT panel. (Ex. 1004, Kamizono, Col. 13:50-55).

161. Accordingly, it is my opinion that Claims 4-5 of the '550 Patent are also obvious over the Sharp Reference in view of Kamizono.

CLAIMS 1-5 ARE OBVIOUS OVER SHIMADA IN VIEW OF KAMIZONO

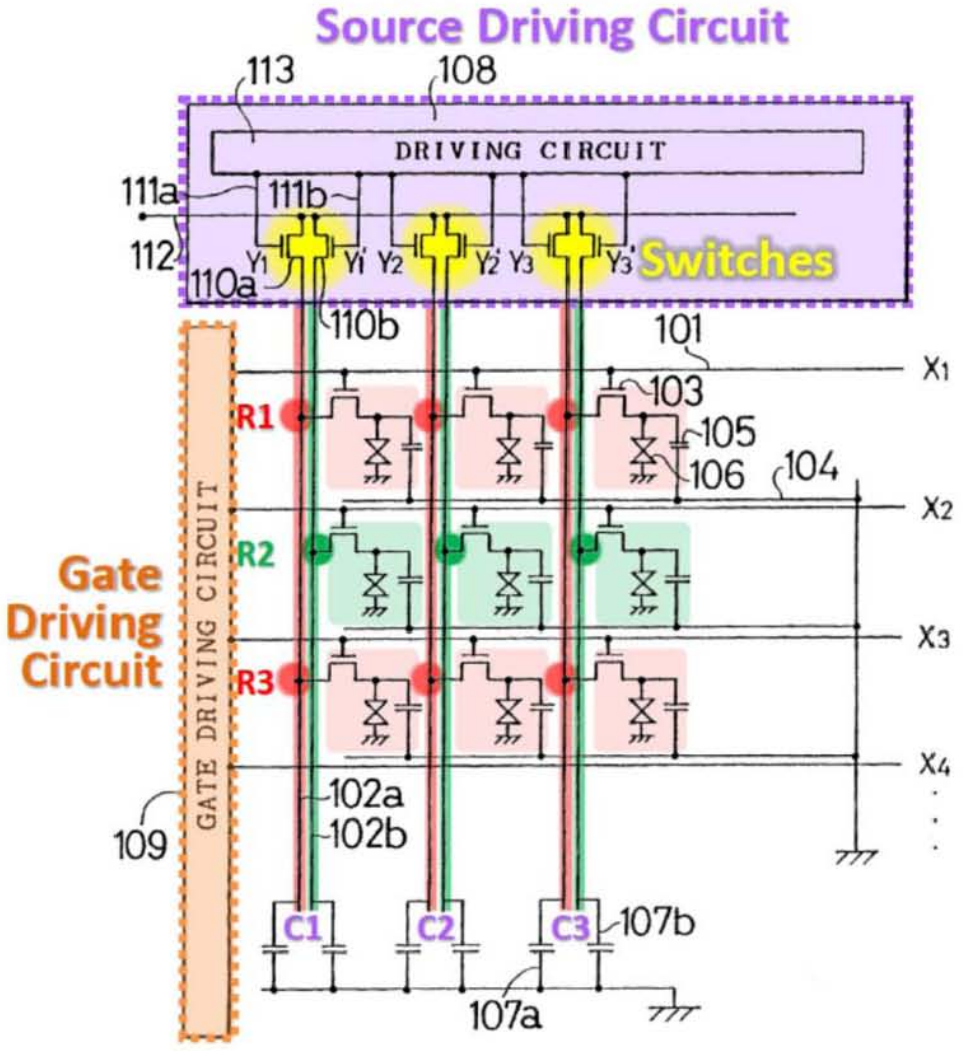
162. As explained below, it is my opinion that Claims 1-5 of the '550 Patent are also obvious over Shimada in view of Kamizono.

SHIMADA

163. As shown below in annotated Figure 4, Shimada teaches an LCD device comprising a matrix array of thin film transistors (TFTs) 103, which drive the corresponding array of pixels 106. (Ex. 1003, Shimada, Col. 4:31-63, Fig. 4).

164. Like the Sharp Reference and Kamizono, Shimada addresses the technical problems arising from increasing the size of the LCD panel and the number of pixels, such as line delay. (*Id*. at Cols. 2:35-3:63). Shimada states that its object is to "reduce the effect of signal delay on display quality" of the LCD device, thereby improving image quality. (*Id*. at Col. 2:66-67).

Shimada Fig. 4



165. As shown in Figure 4, a group of gate bus lines 101 (X_1, X_2, X_3, . . .) is connected to the gate driving circuit 109, and each gate bus line is connected with the gates of all of the TFTs 103 in the row associated with that gate bus line. For example, the first gate line X_1 is connected with the gates of all of the TFTs 103 of the first row (R1), the

second gate line X_2 is connected with the gates of all of the TFTs 103 of the second row (R2), etc. (*Id.* at Col. 4:31-40, Fig. 4).

166. Shimada also teaches that the gate bus lines 101 (X_1, X_2, X_3, . . .) are spaced apart from and parallel to each other (i.e., insulated with each other). (*Id.*, Fig. 4).

167. Figure 4 also shows groups of data bus lines 102a, 102b (the red and green lines) connected to the ***same*** source driving circuit 108. I understand that this was the basis for allowance of Claim 1 by the Patent Office. Figure 4 also shows that the data bus lines (e.g., 102a, 102b) are spaced apart from and parallel to each other (i.e., insulated with each other). (*Id.*, Col. 4:31-40, Fig. 4).

168. As shown above in Figure 4 of Shimada, the first data bus line 102a (red line) and the second data bus line 102b (green line) in each group of data bus lines are respectively connected with the sources of all of the TFTs 103 of the **odd rows** (red boxes in R1 and R3) and **even rows** (green boxes in R2) of the column (C1, C2, C3) associated with that group of data bus lines, as required Claims 1-5 of the '550 Patent.

169. For example, the first data bus line 102a (red line) of the first group is connected with the sources (red dots) of the TFTs 103 of the first row and third row (see the red boxes in R1 and R3) in the first column (C1), while the second data bus line 102b (green line) of the first group is connected with the sources (green dot) of the TFT 103 of the second row (green box in R2) in the first column (C1). (*Id.* at Col. 4:41-63, Fig. 4). The same Odd Row/Even Row configuration is provided in each column (e.g., C2 and C3).

170. Shimada teaches that this Odd Row/Even Row configuration reduces the effect of signal delay caused by the increased number of pixels, thereby improving the video quality of the display of a larger-sized LCD panel. (*Id*. at Cols. 2:34-3:2, Col. 5:49-66).

171. As shown in Figure 4, the source driving circuit 108 for all data bus lines is installed on the same side (e.g., upper side) of the display panel.

172. Figure 4 also shows that the transfer of video signals from the video signal line 112 to the first and the second data bus lines 102a, 102b is switched by the switches 110a, 110b. (*Id*. at Col. 4:41-51, Fig. 4).

IT WOULD HAVE BEEN OBVIOUS TO COMBINE SHIMADA'S LCD DEVICE WITH KAMIZONO'S TEACHING OF MULTIPLE SOURCE AND GATE DRIVERS

173. The LCD device of Shimada discloses all of the key elements of Claims 1-3 of the '550 Patent, including the Odd Row/Even Row configuration.

174. Kamizono discloses source drivers 5 and gate drivers 6. (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).

175. As discussed below, I believe that it would have been obvious to a person of ordinary skill in the art at the time the '550 Patent was filed to combine the teachings of Shimada and Kamizono to arrive at the LCD driving device of Claims 1-3.

176. Shimada and Kamizono are in the same field of LCD display technology. They both disclose active matrix LCD devices and are both directed to improving the performance of a large screen LCD panel. Shimada states that increasing the number of pixels causes undesirable line delay and teaches the Odd Row/Even Row configuration in a

larger sized LCD device to reduce the effect of signal delay on display quality of the LCD device. (Ex. 1003, Shimada, Cols. 2:35-3:63). Kamizono teaches that a "large-screen" LCD panel uses more source and gate driver LSIs than a "small sized" LCD panels would use. (Ex. 1004, Kamizono, Col. 9:19-20, Col. 11:53-64, FIGS. 5 and 9). Because both references addressed the same design need for larger sized LCD panels, I believe that a person of ordinary skill in the art making the source and gate driving circuit for a large-screen LCD panel would have been motivated to combine the teachings of Shimada and Kamizono to arrive at Claims 1-3.

177. Based on my experience and knowledge, I believe that modifying the LCD driving device of Shimada to include the multiple source and gate driver ICs of Kamizono would not produce unexpected results, since such a modification simply allows more pixels to be added to increase the size of the LCD panel. This modification would not change the way Shimada's LCD panel operates in the Odd Row/Even Row configuration.

178. In addition, I believe that a person of ordinary skill in the art would recognize that Kamizono's technique of including multiple source and gate drivers to improve a large screen LCD panel can also be used to improve the large screen LCD panel of Shimada in the same way. This would be well within the level of ordinary skill in the art.

179. Indeed, the prior art was replete with examples of larger sized LCD panels using multiple source and gate drivers. In fact, when I was working in the LCD industry prior to the filing date of the '550 Patent, it was a routine industry practice to change the panel

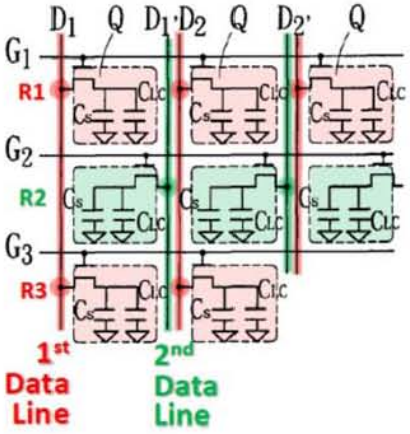
design to increase the size of the panel and/or the number of pixels by simply adding more driver ICs. For example, while the ***small***, low cost LCD panel (which had an equivalent pixel dimension of 7×4) that I worked on at Alien Technology had only a single source driver and a single gate driver, the ***large sized*** LCD panels (which had pixel dimension of at least 800×600) that I worked on at Philips used multiple driver ICs. Using additional source and gate drivers in connection with increasing the size of the panel or the number of pixels in an LCD panel was a well-known and readily available design option.

180. Consistent with my experience, the prior Sekido reference (Ex. 1009) states that "in order to drive many gate bus lines and the source bus lines on the display circuit board, ***a plurality of the gate drivers and source drivers must*** be connected to the area around the liquid crystal display panel." (Ex. 1009, Sekido, Par. [0006]) (emphasis added). This prior art further teaches that increasing the size of the LCD screen will increase the number of the driver ICs. (*Id.*, Par. [0008]).

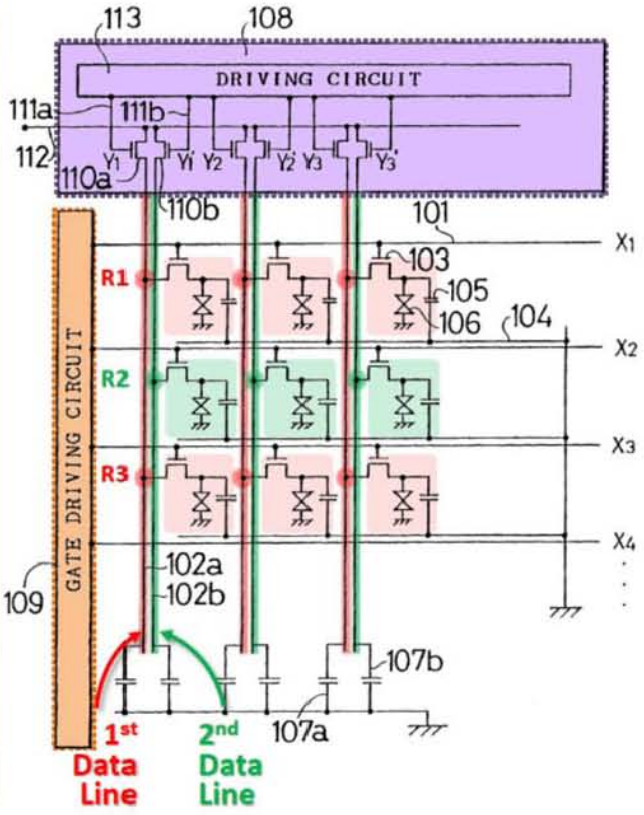
181. Accordingly, I believe that it would have been obvious to a person of ordinary skill in the art to modify the LCD driving device of Shimada to include the multiple source and gate drivers shown in Kamizono and connect them to the data lines (e.g., 102a, 102b) and the gate lines (X_1, X_2, X_3, X_4) of Shimada, respectively.

182. Moreover, as discussed below, Shimada teaches all of the other limitations of Claims 1 and 2 of the '550 Patent.

'550 Patent Fig. 4B



Shimada Fig. 4



SHIMADA DISCLOSES THE ODD ROW/EVEN ROW CONFIGURATION

183. As shown above in annotated Figure 4, Shimada discloses the claimed Odd Row/Even Row configuration of the '550 Patent (shown on the left). (Ex. 1003, Shimada, Col. 4:41-63, Fig. 4).

184. Specifically, the first data line 102a (see the red line) is connected to the sources (red dots) of the TFTs (red boxes) in the odd rows (R1 and R3). The second data line 102b (green line) is connected to the sources (green dot) of the TFTs (green boxes) in the even rows (R2). Figure 4B of the later '550 Patent has the same Odd Row/Even Row configuration.

185. Like the '550 Patent, Shimada teaches that this Odd Row/Even Row configuration reduces the effect of signal delay on the quality of the display, thereby improving image quality. (*Id.* at Cols. 2:66-3:2).

SHIMADA DISCLOSES THAT FIRST AND SECOND DATA LINES IN EACH GROUP OF DATA LINES ARE CONNECTED WITH THE SAME SOURCE DRIVER

186. As shown above in Figure 4 of Shimada, the first and second data lines (e.g., 102a (red line) and 102b (green line)) in each group of data lines in are connected with the ***same*** source driver 108 (*Id.* at Col. 4:41-51, Fig. 4), as required by Claims 1 and 2. I understand that this was the basis for allowance of Claim 1 during prosecution.

SHIMADA DISCLOSES THAT EACH SOURCE DRIVER IS INSTALLED ON THE SAME SIDE OF THE DISPLAY PANEL

187. As shown above in Figure 4 of Shimada, each source driver 108 is installed on the same side of the display panel (*id*. at Col. 4:41-46, Fig. 4), as required by independent Claim 2.

SHIMADA DISCLOSES AN ELECTRONIC SWITCH FOR DATA TRANSFER

188. As shown above in Figure 4 of Shimada, data transfer is switched by an electronic switch 110a, 110b (*id*.), as required by independent Claim 2.

SHIMADA DISCLOSES THAT GATE LINES/DATA LINES ARE INSULATED WITH EACH OTHER

189. In addition, Shimada teaches that the gate lines 101 (X_1, X_2, X_3, . . .) are "insulated with each other" under the broadest reasonable construction since they are shown to be spaced apart from and parallel to each other. Likewise, Shimada teaches that

the data bus lines (e.g., 102a, 102b) are insulated with each other as they are spaced apart from and parallel to each other. (*Id*. at FIG. 4).

190. Because Shimada and Kamizono combine to disclose all of the elements of Claims 1 and 2, and further because there was a clear motivation for a person of ordinary skill in the art to combine these references, I believe that Claims 1 and 2 are obvious over Shimada in view of Kamizono.

SHIMADA DISCLOSES A SPACE BETWEEN THE NEIGHBORING DATA LINE TO PREVENT SHORT CIRCUITING

191. Claim 3, which depends from Claim 2, recites that "there is a space [i.e., a gap] between the neighboring data lines to prevent them from short circuit." Figure 4 of Shimada clearly shows that there is a space between the neighboring data lines (e.g., between 102a and 102b) that prevents short circuiting.

192. When two neighboring data lines are shown to be spaced apart from each other in the schematic circuit diagram for an LCD driving device, such as Figure 4 of Shimada, I expect that there is a sufficient space between these data lines to prevent short circuiting. Otherwise, the LCD driving device would not be operating as described in the reference.

KAMIZONO DISCLOSES A CHIP ON GLASS

193. Dependent Claim 4 requires that the gate driver is a chip installed on glass.

194. Kamizono teaches that the use of a chip-on-glass is the preferred way of implementing the gate drivers for a large sized LCD panel. (Ex. 1004, Kamizono, Col. 1:12-58).

195. Shimada and Kamizono are in the same field of LCD display technology. They both disclose active matrix LCD devices and are both directed to improving the performance of a large screen LCD panel. Shimada states that increasing the number of pixels causes undesirable line delay and teaches the Odd Row/Even Row configuration in a ***larger sized*** LCD device to reduce the effect of signal delay on display quality of the LCD device. (Ex. 1003, Shimada, Cols. 2:35-3:63). Kamizono teaches that a "large-screen" LCD panel uses more source and gate driver LSIs than a "small sized" LCD panels would use. (Ex. 1004, Kamizono, Col. 9:19-20, Col. 11:53-64, FIGS. 5 and 9). Because both references addressed the same design need for larger sized LCD panels, I believe that a person of ordinary skill in the art making the gate drivers for a large-screen LCD panel would have been motivated to combine the teachings of Shimada and Kamizono to arrive at Claim 4.

196. Based on my experience and knowledge, I believe that using the chip on glass of Kamizono for the gate driver in the LCD device of Shimada would not produce any unexpected result and would not affect, for example, the Odd Row/Even Row configuration in Shimada's LCD device.

197. Based on my experience and knowledge, I believe that a person of ordinary skill in the art would recognize that Kamizono's technique of using a chip on glass for the gate driver to improve a large screen LCD panel (e.g., increasing the operational reliability and reducing the overall product size) can be also used to improve the large screen LCD panel of Shimada in the same way.

198. Accordingly, a person of ordinary skill in the art making a large-screen LCD panel would have been motivated to combine the teachings of Shimada and Kamizono to arrive at Claim 4.

199. Accordingly, it is my opinion that Claim 4 is also obvious over Shimada in view of Kamizono.

KAMIZONO DISCLOSES INTEGRATED GATE DRIVER CIRCUIT

200. Claim 5 requires that the gate driver is an integrated gate driver circuit installed on glass.

201. Kaminozo teaches that an LCD panel can be a poly-Silicon TFT panel and the source and gate drivers can be mounted on the panel in a spare area other than the display area of the panel (i.e., forming an integrated structure with the LCD panel). (Ex. 1004, Kamizono, Col. 13:50-55). Since the gate drivers are formed on the same substrate as the pixel TFTs, the result is integrated gate driver circuit installed on the same substrate as the pixel TFTs.

202. Moreover, as discussed above, it was well-known at the time of the filing date of the '550 Patent that an LCD panel must include a glass substrate or other substantially transparent substrate to transmit the light from the backlight to the LCD viewer's eyes. LCD panels modulate the light generated by the backlight assembly and passed through the glass substrate (or other transparent substrate) according to the TFT drive signals. The light exits the LCD surface nearest the viewer and allows the viewer to see the visual image generated based on the electrical input signal.

203. The use of a glass substrate was the preferred choice, especially in an LCD panel having a large number of pixels. Compared to other transparent materials, glass is cheaper, provides a smoother surface, and is also more resistant to a high temperature required for processing TFTs in an LCD panel. In addition, a glass substrate protects liquid crystal materials and TFTs in the LCD panel from moisture. In my experience, LCD panels with a large number of pixels using TFTs all included glass substrates.

204. Thus, I believe that it would have been obvious to a person of ordinary skill in the art that the integrated gate driver circuit taught by Kamizono is installed on a glass substrate in an LCD panel since the use of glass substrate is one of small number of widely known design options to make an LCD panel and to have the light transmitted from the backlight.

205. As discussed above, because Shimada and Kamizono addressed the same design need for larger sized LCD panels, I believe that a person of ordinary skill in the art

making the gate drivers for a large-screen LCD panel would have been motivated to combine the teachings of Shimada and Kamizono to arrive at Claim 5.

206. Based on my experience and knowledge, I believe that using the integrated gate driver circuit on glass of Kamizono for the gate driver in the LCD device of Shimada would not produce any unexpected result and would not affect, for example, the Odd Row/Even Row configuration in Shimada's LCD device.

207. Accordingly, it is my opinion that Claim 5 of the '550 Patent is also obvious over Shimada in view of Kamizono.

THE COMBINATION OF SHIMADA AND KAMIZONO TEACHES ALL ELEMENTS OF CLAIMS 1-5

208. The following claim charts summarize where I believe each element of Claims 1-5 is taught by the combination of Shimada and Kamizono:

The Claims Of The '550 Patent	Shimada in View of Kamizono
1. A liquid crystal display driving device of matrix structure type including:	Shimada discloses a liquid crystal display driving device of matrix structure type (Ex. 1003, Shimada, Col. 1:8-10, Col. 4:31-67, Figs. 4, 7).
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels can be driven;	Shimada discloses a group of thin film transistors 103 with matrix array consisting of N (e.g., 3) rows and M (e.g., 3) columns of thin film transistors 103, wherein each thin film transistor can drive one pixel 106 so that N×M of pixels can be driven (Ex. 1003, Shimada, Col. 4:31-63, Fig. 4).
a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the	Shimada discloses a group of N gate lines 101 (e.g., X_1, X_2, X_3, . . .) connected to the gate driver (e.g., gate driving circuit 109) and insulated with each other by being spaced apart

The Claims Of The '550 Patent	Shimada in View of Kamizono
thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	from and parallel to each other. The first gate line X_1 is connected with the gates of all the thin film transistors 103 of the first row. The second gate line X_2 is connected with the gates of all the thin film transistors 103 of the second row . . . and the N^{th} gate line X_N is connected with the gates of all the thin film transistors 103 of the N^{th} row. (Ex. 1003, Shimada, Col. 4:31-40, Figs. 4, 7). Kamizono discloses scanning lines 4 connected to multiple scanning line driving LSIs 6 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).
M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column, and	Shimada discloses M (e.g., 3) groups of data lines 102a, 102b connected to the source driver (e.g., the source driving circuit 108) and insulated with each other by being spaced apart from and parallel to each other. The first and the second data lines 102a, 102b of the first group of data lines are respectively connected with the sources of all the thin film transistors 103 of the odd and the even rows of the first column. The first and the second data lines 102a, 102b of the second group of data lines are respectively connected with the sources of all the thin film transistors 103 of the odd and the even rows of the second column . . . and the first and the second data lines 102a, 102b of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors 103 of the odd and the even rows of the M^{th} column (Ex. 1003, Shimada, Col. 4:41-63, Fig. 4). Kamizono discloses signal lines 3 connected to multiple signal line driving LSIs 5 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).

The Claims Of The '550 Patent	Shimada in View of Kamizono
the first data lines and the second data lines of each group of data lines are connected with the same source driver.	Shimada discloses that the first data lines 102a and the second data lines 102b of each group of data lines are connected with the same source driver 108 (Ex. 1003, Shimada, Col. 4:41-63, Fig. 4; *compare with* Ex. 1001, '550 Patent, Fig. 6A).
2. The liquid crystal display device of matrix structure type including:	Shimada discloses a liquid crystal display driving device of matrix structure type (Ex. 1003, Shimada, Col. 1:8-10, Cols. 4:31-5:15, Figs. 4, 7).
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels can be driven;	Shimada discloses a group of thin film transistors 103 with matrix array consisting of N (e.g., 3) rows and M (e.g., 3) columns of thin film transistors 103, wherein each thin film transistor can drive one pixel 106 so that N×M of pixels can be driven (Ex. 1003, Shimada, Col. 4:31-63, Fig. 4).
a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	Shimada discloses a group of N gate lines 101 (e.g., X_1, X_2, X_3, . . .) connected to the gate driver (e.g., gate driving circuit 109) and insulated with each other by being spaced apart from and parallel to each other. The first gate line X_1 is connected with the gates of all the thin film transistors 103 of the first row. The second gate line X_2 is connected with the gates of all the thin film transistors 103 of the second row . . . and the N^{th} gate line X_N is connected with the gates of all the thin film transistors 103 of the N^{th} row (Ex. 1003, Shimada, Col. 4:31-40, Figs. 4, 7). Kamizono discloses scanning lines 4 connected to multiple scanning line driving LSIs 6 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).
M groups of data lines connected to the source drivers and insulated with	Shimada discloses M (e.g., 3) groups of data lines 102a, 102b connected to the source driver

The Claims Of The '550 Patent	Shimada in View of Kamizono
each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column,	(e.g., the source driving circuit 108) and insulated with each other by being spaced apart from and parallel to each other. The first and the second data lines 102a, 102b of the first group of data lines are respectively connected with the sources of all the thin film transistors 103 of the odd and the even rows of the first column. The first and the second data lines 102a, 102b of the second group of data lines are respectively connected with the sources of all the thin film transistors 103 of the odd and the even rows of the second column . . . and the first and the second data lines 102a, 102b of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors 103 of the odd and the even rows of the M^{th} column (Ex. 1003, Shimada, Col. 4:41-63, Fig. 4). Kamizono discloses signal lines 3 connected to multiple signal line driving LSIs 5 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).
Wherein the first data lines and the second data lines of each group of data lines are connected with the same source driver,	Shimada discloses that the first data lines 102a and the second data lines 102b of each group of data lines are connected with the same source driver 108 (Ex. 1003, Shimada, Col. 4:41-63, Fig. 4; *compare with* Ex. 1001, '550 Patent, Fig. 6A).
each source driver is installed on the same side of the display panel and	Shimada discloses that each source driver 108 is installed on the same side (e.g., upper side) of the display panel (Ex. 1003, Shimada, Col. 4:41-46, Fig. 4).
The data transfer is switched by an electronic switch.	Shimada discloses that the data transfer is switched by an electronic switch 110a, 110b (Ex. 1003, Shimada, Col. 4:41-46, Fig. 4).

The Claims Of The '550 Patent	Shimada in View of Kamizono
3. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein there is a space between the neighboring data lines to prevent them from short circuit.	Shimada discloses that there is a space between the neighboring data lines 102a, 102b (Ex. 1003, Shimada, Figs. 4, 7).
4. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein the gate driver is a chip installed on glass.	Kamizono discloses that a liquid crystal driving LSI is commonly mounted as a semiconductor chip by a chip-on-glass (COG) method. (Ex. 1004, Kamizono, Col. 1:12-58).
5. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein the gate driver is an integrated gate driver circuit installed on glass.	Kamizono discloses LCD driving circuits that form an integrated structure with a poly-Silicon TFT panel. (Ex. 1004, Kamizono, Col. 13:50-55).

209. Accordingly, it is my opinion that Claims 1-5 of the '550 Patent are also obvious over Shimada in view of Kamizono.

210. At this time I am not aware of any arguments and evidence of "secondary considerations" that would render the claims of the '550 Patent non-obvious with respect to my opinions set forth herein on the issue of obviousness. Should Patent Owner present such evidence, I reserve the right to respond to such evidence and arguments.

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: March 20, 2015

By: Michael J. Marentic

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