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CERTIFICATION

This is to certify that the attached translation is, to the best of my knowledge and belief, a true and accurate translation from Japanese into English of the attached Unexamined Patent Application No. H08-305322.

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Sworn to and subscribed before me
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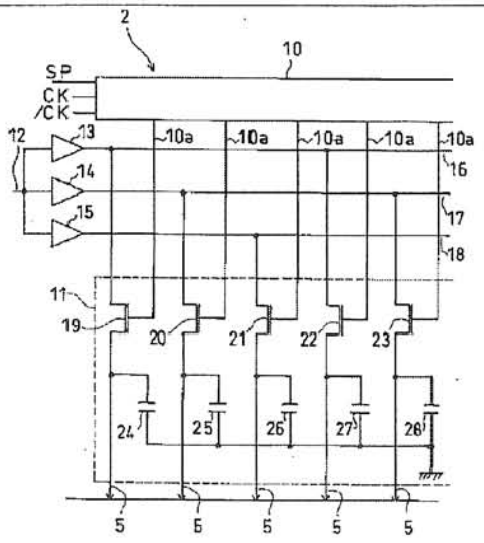
(54) [Title of the Invention] Display Device

(57) [Abstract]
[Constitution] After the same data signals from a data signal line 12 are supplied to three data signal lines 16 to 18 via buffer circuits 13 to 15, they are supplied to sampling switches 19 to 23 of a sampling hold circuit 11. The data signals sampled by the sampling hold circuit 11 are supplied to source bus lines 5....
[Effect] Because it is possible to correctly sample data signals with little corruption or noise, high-resolution display with limited decrease in the horizontal resolution and decrease in the display quality becomes possible.



[Claims]

[Claim 1] A display device provided with a plurality of data signal lines by which data signals are respectively supplied,

a plurality of sampling circuits by which the data signals supplied from the plurality of data signal lines are respectively sampled,

a plurality of data bus lines respectively connected to the plurality of sampling circuits,

a plurality of pixel units that are both connected to the plurality of data bus lines and arranged in matrix form, and

a drive circuit including the sampling circuits and that drives the data bus lines, wherein

at least two of the plurality of data signal lines have the same data signals supplied and are connected to different sampling circuits via respectively different buffer circuits.

[Claim 2] The display device according to claim 1, wherein of the plurality of sampling circuits, the sampling circuits for which the timing of the sampling is synchronized are both connected to respectively different data signal lines and have no time overlap of the ON time of the respective sampling circuits.

[Claim 3] The display device according to claim 1 or 2, wherein the buffer circuits are formed on the same substrate as the sampling circuits.

[Claim 4] A display device provided with a plurality of data signal lines by which data signals are respectively supplied,

a plurality of sampling circuits by which the data signals supplied from the plurality of data signal lines are respectively sampled,

a plurality of data bus lines respectively connected to the plurality of sampling circuits,

a plurality of pixel units that are both connected to the plurality of data bus lines and arranged in matrix form, and

a drive circuit that includes the sampling circuits and that drives the data bus lines, wherein

the data signal line is divided into a plurality in the horizontal direction of the display, and each divided signal line is connected to sampling circuits via respectively different buffer circuits.

[Claim 5] A display device provided with a plurality of data signal lines by which data signals are respectively supplied,

a plurality of sampling circuits by which the data signals supplied from the plurality of data signal lines are respectively sampled,

a plurality of data bus lines respectively connected to the plurality of sampling circuits,

a plurality of pixel units that are both connected to the plurality of data bus lines and arranged in matrix form, and

a drive circuit that includes the sampling circuits and that drives the data bus lines, wherein

of the plurality of pixel units, respectively different data bus lines are connected to the plurality of pixel units adjacent in the column direction, and the same sampling circuits are connected via the buffer circuits to these data bus lines.

[Claim 6] The display device according to claim 1, 2, 3, 4 or 5, wherein the drive circuit and the image display unit comprising the plurality of pixel units are formed monolithically on the same substrate.

[Detailed Description of the Invention]

[0001] [Field of Industrial Use] The present invention relates to a display device such as a liquid crystal display device or the like.

[0002] [Prior Art] Conventionally, display devices, for example, as shown in FIG. 12, liquid crystal display devices (hereafter called LCD) have been constituted by a display unit 101 having a plurality of pixel units 104..., and a source driver 102 and a gate driver 103 as a drive circuit for driving each pixel unit 104.

[0003] Each of the pixel units 104... is respectively arranged at a place at which a plurality of source bus lines 105... connected to the source driver 102 and a plurality of gate bus lines 106... connected to the gate driver 103 intersect orthogonally. Thus, the arrangement of the pixel units 104... is in a matrix form in the display unit 101.

[0004] Also, a pixel unit 104 is constituted by a pixel transistor 107 formed from TFT (thin film transistors), pixel capacity 108 and additional capacity 109; the gate terminals of pixel transistor 107 are connected to gate bus line 106, source terminals are connected to source bus line 105, and drain terminals are connected to pixel capacity 108 and additional capacity 109.

[0005] Source driver 102 is constituted by shift register 110, and sampling switches 111 formed from transistors, sampling capacitors 112, data signal lines 113 and the like; sampling hold circuit 114 is formed from the above sampling switches 111, sampling capacitors 112, data signal lines 113, and source bus lines 105.

[0006] Start pulses (SP) and drive clocks (CK, /CK) input to the shift register 110, and the input SP are sequentially shifted according to the CK and /CK and output to sampling hold circuit 114.

[0007] Gate driver 103 has a shift register 115 and sequentially outputs scan signals to each gate bus lines 106....

[0008] Furthermore, when the above display unit 101, source driver 102, and gate driver 103 are formed monolithically on the same substrate, there are cases when only display unit 101 is formed on the insulated substrate.

[0009] Here we will describe the operation of the displace device with the constitution noted above. First, the SP input to the shift register 110 of the source driver 102

is sequentially shifted by CK and /CK and output to sampling hold circuit 114, and become the sampling pulses for sampling hold circuit 114. Then, sampling switch 111 goes to an ON state by means of the input sampling pulse, and the data signal of data signal line 113 at the point in time that this sampling pulse is input is sampled.

[0010] Then, the data signal sampled by the sampling pulse is held in sampling capacitor 112 and output to source bus line 105 as a source bus line signal.

[0011] Meanwhile, the output of each digit of shift register 115 of gate driver 103 is output as scan signals (gate bus line signals) sequentially to gate bus lines 106...; pixel transistors 107 connected to selected gate bus lines 106 turn ON, and the source bus line signals at that point in time are sequentially written as image data to pixel capacity 108 and additional capacity 109.

[0012] Then, by driving the liquid crystal corresponding to each pixel unit 104, the desired display is achieved.

[0013] Therefore, with the LCD of the constitution noted above, as described above, source driver 102 uses the panel sample hold method by which image data is held on the display unit 101 side. With an LCD having this kind of source driver 102, when the number of pixel units 104 in the horizontal scan direction becomes high, the image data write time is different for pixel unit 104 connected to the least significant digit of the shift register 110 and the pixel unit 104 connected to the most significant digit. Because of this, it is possible to make the image data write time longer with the pixel units 104 connected to the upper digits of the shift register 110, but there is the problem that it is not possible to have sufficient image data write time with the pixel units 104 connected to the lower digits.

[0014] In light of that, to solve the problems noted above, we propose an LCD that uses a driver sample hold method source driver by which image data is held on the source driver side.

[0015] In the following, we will describe an LCD that uses the source driver of the driver sample hold method noted above. Furthermore, this LCD, with the exception of the source driver, has the same display unit 101 and gate driver 103 as that of the LCD shown in FIG. 12; therefore, in this description, we will describe only the source driver of the driver sample hold method.

[0016] The source driver of the driver sample hold method noted above has a constitution in which the output side of sampling hold circuit 114 of source driver 102 shown in FIG. 12 is connected to a transfer circuit 120 formed from transfer switch 116, hold capacitor 117, buffer circuit 118, and transfer signal line 119.

[0017] In other words, at the time point that data of one scan line has been sampled by sampling hold circuit 114, a transfer signal is output from transfer signal line 119 by transfer circuit 120, transfer switch 116 goes to an ON state, and after the data held in sampling capacitor 112 of sampling hold circuit 114 has been simultaneously transferred to hold capacitor 117, sampling of the next scan period is performed.

[0018] In other words, during the period that data of the next one scan line is being sampled, the sampling data of the previous scan line held in hold capacitor 117 is continuously applied as source bus line signals to source bus lines 105 (FIG. 12) via the buffer circuit 118.

[0019] In this way, by using the source driver of the driver sample hold method, even when there is a large number of pixel units 104 in the horizontal scan direction, it is possible to obtain sufficient write time for the image data to the respective pixel units 104.... By doing this, it is possible to make the image data write time almost the same for the pixel unit 104 connected to the least significant digit of the shift register 110 and the pixel unit 104 connected to the most significant digit.

[0020] Furthermore, when the LCD is formed monolithically by a driver on the insulated substrate, the speed at which the shift register formed using p-SiTFT operates stably is about several MHz, and with the shift register inside the source driver of the LCD with a large number of pixels in the horizontal direction which requires high speed operation, a problem occurs of having the shift register operating speed be insufficient.

[0021] In light of that, to reduce the operating speed of the shift register, for example, as shown in FIG. 14, we propose a source driver for which a plurality of systems, in this case four systems of shift registers 131 to 134, are provided, and by having the respective shift registers 131 to 134 operate at CK1 to CK4, /CK1 to /CK4 of different phases, each level of shift register 131 to 134 is operated at low speed with the overall shift speed remaining as is.

[0022] With the source driver having the four systems of shift registers 131 to 134 noted above, as shown in FIG. 15, the start pulses SP are sequentially shifted by CK1 to CK4 and /CK1 to /CK4 and sampling pulses SMP1 to SMP8 are output. Furthermore, the width of SMP1 to SMP8, which are the output of the four systems of shift registers 131 to 134, is four times that of when the shift register has one system, but the phase skew of SMP1 to SMP8 is the same as when the shift register has one system.

[0023]

[Problems the Invention Attempts to Solve] However, with the source driver having the four systems of shift registers 131 to 134 noted above, as shown in FIG. 15, each sampling pulse

SMP1 to SMP8 is in a mutually overlapping form. Because of this, when seen at a given moment, there are always eight sampling transistors 111... ON. In other words, the capacitance of eight sampling capacitors 112... has become the load via sampling transistors 111 for data signal line 113 or for the data signal output circuit. Furthermore, there is wiring resistance on data signal lines 113 and ON resistance on sampling transistors 111, and therefore the response of the data signals with each sampling capacitor 112 deteriorates with operation of a time constant of the RC integrating circuit, and the waveform becomes corrupted compared with the original data signal.

[0024] With sampling of data signals done based on this kind of corrupted waveform, the band information that the data signal originally had is lost, so the display has low horizontal resolution. Furthermore, for the scan signals as well (not illustrated), depending on the constitution, two adjacent outputs of the gate shift register are overlapping, and for the pixel part as well, the same kind of problem occurs as with the sampling unit of the source driver noted above.

[0025] To prevent this kind of problem, we propose a display device for which a video signal line is arranged for each shift register 131 to 134. In this case, for example, the Nth (SMP1) fall of the sampling pulse shown in FIG. 15 and the N $+8^{th}$ (SMP9) rise have the same timing, but in actuality, due to signal waveform corruption or delay, a phenomenon occurs of the N $+8^{th}$ sampling transistor simultaneously turning ON before the Nth sampling transistor 111 goes completely OFF.

[0026] When this kind of phenomenon occurs, as described above, even if the video signal line is divided into a plurality of parts, the sampling data of the Nth sampling hold circuit 114 of the source driver is affected not only by the N +4 sampling signal, but also by the N $+8^{th}$ sampling data, and an adverse effect is given to the display as a ghost phenomenon or noise.

[0027] Furthermore, the phenomenon described above can also occur in the same manner with the display unit. Because of this, for example, the present applicant, in Patent Application No. H05-300537, proposed a display device for which the same video signal line is branched into a plurality of parts external to the drive circuit. In this way, by branching the same video signal line into a plurality of parts external to the drive circuit, having a plurality of sampling circuits connected to one video signal line turning on simultaneously is eliminated, and as a result, corruption of the signal in each video signal line is reduced, and the resolution of the display device is improved.

[0028] However, even when the same video signal line is simply divided into a plurality of parts, when divided into a plurality of parts on the same substrate as the panel, by means of contact resistance with a flexible substrate or the like, wiring resistance, and also output impedance of the video signal supply source, it is possible to increase the time constant, but it is not possible to totally inhibit the occurrence of ghosts. Also, even when the same video signal line is simply divided into a plurality outside the panel, by means of the aforementioned contact resistance with a flexible substrate or the like, wiring resistance, and also output impedance of the video signal supply source, it is possible to increase the time constant, but it is not possible to totally inhibit the occurrence of ghosts.

[0029] Also, when we look at sampling circuits connected to the same data signal lines constituting the source driver, there is OFF resistance in the sampling transistor; however, when it is not possible to make the OFF resistance of the sampling transistor sufficiently large, the problem occurs of the sampling data written to the sampling capacitor going through the OFF resistance of the transistors and the data signal lines and having crosstalk with each other.

[0030] The present invention was created in light of the problem points noted above, and its objective is to provide a display device that reduces data signal corruption or data signal noise due to adjacent transistors being ON simultaneously and that reduces crosstalk due to insufficient or decreased transistor OFF characteristics, thus preventing a ghost phenomenon and also being able to realize high resolution display for which a decrease in horizontal resolution and a decrease in display quality due to crosstalk are inhibited.

[0031]

[Means for Solving the Problems] The display device of claim 1 is equipped with a plurality of data signal lines by which data signals are respectively supplied, a plurality of sampling circuits by which the data signals supplied from the plurality of data signal lines are respectively sampled, a plurality of data bus lines respectively connected to the plurality of sampling circuits, a plurality of pixel units connected to the plurality of data bus lines and arranged in matrix form, and a drive circuit including the sampling circuits for driving the data bus lines, wherein at least two of the plurality of data signal lines have the same data signals supplied, and are connected to different sampling circuits via respectively different buffer circuits.

[0032] The display device of claim 2 is the display device according to claim 1, wherein of the plurality of sampling circuits, the sampling circuits for which the timing of the sampling is synchronized are connected to respectively different data signal lines, and there is no time overlap of the ON time of the respective sampling circuits.

[0033] The display device of claim 3 is the display device according to claim 1 or 2, wherein the buffer circuits are formed on the same substrate as the sampling circuits.

[0034] The display device of claim 4 is equipped with a plurality of data signal lines by which data signals are respectively supplied, a plurality of sampling circuits by which the data signals supplied from the plurality of data

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