UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

- -x

SHARP CORPORATION, :

SHARP ELECTRONICS :

CORPORATION, and SHARP :

ELECTRONICS : CaseIPR2015-00913

MANUFACTURING COMPANY : Patent No. 7,420,550

OF AMERICA, INC.,

Petitioners,

v.

SURPASS TECH

INNOVATION LLC,

Patent Owner.

- -x

Deposition of MICHAEL J. MARENTIC

NEW YORK, NEW YORK

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Deposition of MICHAEL J. MARENTIC, held at the offices of:

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Pursuant to agreement, before Nancy Mahoney, CCR/RPR/CLR, Notary Public in and for the State of New York.

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C O N T E N T S

E X H I B I T S

(Attached to transcript.)

P R O C E E D I N G S

MICHAEL J. MARENTIC,

after having been first duly sworn or affirmed to testify to the truth, was examined and testified as follows:

EXAMINATION BY COUNSEL FOR THE PATENT OWNER

WAYNE HELGE:

Q Good morning, Mr. Marentic.

A Good morning.

Q Good to see you again.

Are you familiar with U.S. Patent No. 7,420,550?

A Yes.

Q That's the patent at issue in Sharp v. Surpass Tech Innovation, Case No. IPR2015-00913. Is that right?

A Yes, that is correct.

Q And you provided a declaration with some opinions about that patent, correct?

A Yes.

Q We're here this morning to talk about those opinions, correct?

A Yes.

Q That's the purpose of your deposition?

A Yes.

Q Mr. Marentic, can you give your full name, please, for the record.

A Michael James Marentic.

Q Mr. Marentic, we did this just about a month ago, last deposition. I just want to check. Is there any reason today that you would not be able to give true and accurate testimony in this deposition?

A No.

Q Mr. Marentic, I'm also going to read the same paragraph that I read for you last time into the record. We talked about this last time. I don't think there will be any confusion. But this comes from the Office Patent Trial Practice Guide. The paragraph reads, Once the cross-examination of a witness has commenced, and until cross-examination of the witness has concluded, counsel offering the witness on direct examination shall not: (a) consult or confer with the witness regarding the substance of

the witness' testimony already given, or anticipated to be given, except for the purposes of conferring and whether to assert a privilege against testifying or on how to comply with the Board order; or (b) suggest to the witness the manner in which any questions should be answered.

Do you recall that I had read that paragraph for you before?

A I remember hearing a similar paragraph.

Q And you understand the prohibitions against conferring with your counsel today until your entire deposition is concluded, correct?

A I do.

Q Okay, thank you.

Mr. Marentic, has there been any change to your CV since October, since early October?

A No.

Q Have you given any further depositions or undertaken any further engagements since your last deposition?

A No.

Q In preparing for this deposition, who did

you talk to?

A I talked to attorneys at ARE.

Q Anybody else?

A No.

Q And what documents did you review in preparation for this deposition?

A My declaration, the '550 patent, the Sharp reference, and Kamizono.

Q Did you review the petition also?

A No.

Q When was the last time you reviewed the petition in this case?

A A long time ago. I can't attach a date to it.

Q Was it before it was filed or after it was filed?

A It was after it was filed.

Q Did you prepare your declaration without seeing the petition?

MR. BERKOWITZ: Objection to form.

A The declaration was prepared --

MR. BERKOWITZ: I'll just interrupt the

witness. To the extent that it involves any privileged communication not to reveal that.

Again, if you can answer the question without revealing any privileged communication, please go ahead.

A I did not see the petition prior to the filing date of March 20 exactly.

Q How many days before March 20, 2015 did you see your petition -- excuse me. How many days before March 20, 2015 did you first see your declaration?

MR. BERKOWITZ: Objection to form, relevance.

A I worked on my declaration most of the month of March.

Q In preparation for today's deposition, did you look at any documents from any of the other IPRs filed against Surpass?

MR. BERKOWITZ: Objection to form, outside the scope.

A No, not that I'm aware of.

Q Are you aware that there was a deposition earlier this month -- excuse me, it was actually late

last month -- in a case also against the '550 patent?

A I was not aware of that.

Q So you didn't review a transcript of that deposition?

A No.

Q Mr. Marentic, when did you last look at your declaration?

A Last night.

Q Was that the first time you'd reviewed it since it was filed?

A No.

Q You'd been reviewing it in preparation of this deposition over a series of days then?

A Yes.

Q You reviewed your declaration against the '843 patent in preparation for your October deposition, correct?

A Yes.

Q And you reviewed your declaration against the '550 patent in preparation for this deposition, correct?

A Correct.

Q Having recently reviewed both of those declarations, do you believe that your methodologies were consistent in those two cases?

MR. BERKOWITZ: Objection to form.

A The last time I looked at the '843 declaration was the date of the deposition. I've not looked at it since. Would you ask the question again?

Q My question was whether you felt that your methodologies in these two declarations were consistent.

A Consistent with what, each other?

Q Yes.

A I believe so.

Q Did you spot any errors in the '550 declaration when you reviewed it in preparation for this deposition?

A I didn't find any errors. There was a point of clarification and that is about Claim 5 that speaks to the integrated gate drivers. The claim chart relies upon Kamizono, and in the text there was a discussion of Sharp showing integrated gate drivers

as well as Kamizono showing integrated gate drivers. Both of those references show it. The claim chart seemed to have a stronger description, and I relied upon Kamizono claim chart, but both Kamizono and both Sharp show integrated gate driver technology as a way of implementing the drivers that drive the gates.

Q So, Mr. Marentic, how would you -- how would you have revised that declaration to capture this clarification that you want to make?

MR. BERKOWITZ: Objection to form.

A I may reorganize the material a little different in sequence and paragraphs, but both of them strongly show a path towards integrated gate drivers.

Q So are you saying you would have changed organization but not changed the content?

A Generally, yes.

Q Is there anything you want to add to what I just said?

A I don't believe so.

Q Are there any other changes to the declaration that you would have made based on your

recent review?

A Somewhere was a misspelling. Gate, I think was spelled g-a-t-d, obvious what it was, and I can't recall where it is.

Q Anything else you'd want to change?

A No.

Q So everything else is technically accurate and you stand by those words. Is that right?

A That is correct.

Q Mr. Marentic, we're going to talk a lot today I think about drivers, gate drivers, source drivers. Let's talk about source drivers first.

Generally speaking, in a LCD panel what is the purpose of a source driver?

A The purpose of the source driver is to provide an analog voltage on the source lines, source spots, that represents the video input signal.

Q Does the source driver have to drive an analog voltage?

MR. BERKOWITZ: Objection to form.

A For the larger content -- or larger displays displaying video, they would be analog

voltage.

Q So it has to be analog voltage?

A There are certain applications where it wouldn't need to be. It could be an on/off, but then that display wouldn't be capable of displaying gray scale. It would be full on, full off. There aren't displays out there that require just that.

Q And an analog voltage has to be sufficient to do certain things in the pixel. Is that right?

MR. BERKOWITZ: Objection to form.

A The output range of an analog output needs to match the liquid crystal cell characteristics.

Q And what goes into those characteristics, what factors are there?

A Making sure that the cell can be driven to a full off state and a full on state. So, for instance, it wouldn't be biased in such a way that the cell is always on or the cell is always off.

Q Well, let me ask you this. Is it common for an LCD panel to include a storage capacitor?

MR. BERKOWITZ: Objection to form.

A There is a number of components that appear

as capacitors. Certainly the liquid crystal material itself between the two electrodes appears as a capacitor.

Q How would you describe that, that liquid crystal material acting as a capacitor?

MR. BERKOWITZ: Objection.

Q Is there a term that we can use to describe that?

MR. BERKOWITZ: Objection to form. Please let him finish the answer.

A There is a second capacitor in each pixel, a holding capacitor that is formed during the process of forming the TFTs. So there's two capacitors in parallel, and then there's an array of parasitic capacitances throughout the panel. The easiest to consider would be the crossover of a gate and a source bus at that intersection would be a parasitic capacitance.

Q Is there a term we use to describe -- or we can use to describe the capacitance resulting from the LC material?

A Clc.

Q And that would be a liquid crystal capacitance?

A Yes.

Q And then what about the hold capacitor?

MR. BERKOWITZ: Objection to form.

A That could be called -- I'd like to be consistent. Sometimes it's called S shunt. The '550 uses the Cs shunt.

Q Is that the same thing as a storage capacitor?

A Yes.

Q How is the storage capacitor charged within a frame?

A It's in parallel with the Clc.

Q How do you get a potential difference across that storage capacitor?

MR. BERKOWITZ: Objection to form, foundation.

A Through the drain of a TFT on that pixel.

Q And where does the drain get voltage to charge the storage capacitor?

MR. BERKOWITZ: Objection to form,

foundation.

A There is a voltage presented by a driver output to a source bus and a gate signal will turn on the TFT and allow charging of the parallel Clc and Cs capacitance.

Q You said just a moment ago a driver. Would that be a source driver?

MR. BERKOWITZ: Objection to form.

A The term source driver or data driver are equivalent for purposes of this patent. The driver output would generate the voltage that is present on the source bus and that output could be part of another device that's also called a driver and that driver would be a monolithic integrated circuit. So the term driver can refer to an integrated circuit or a driver can refer to a single output that is present within an integrated circuit or IC.

Q When you say output, you're talking about that analog voltage?

A A circuit that outputs the analog voltage that is presented to the TFT array.

Q And that is the analog voltage, correct, in

a video displaying LCD?

A In a display displaying video, that would be an analog voltage or stepped in increments of say 256 grade levels.

Q Did you say "or stepped in increments"?

A Yes.

Q What would be stepped in increments?

A The output voltage of a stage or a single output.

Q What is a stage?

A A driver output. There is a couple of ways of supplying the video. One would be an infinite number of combinations between two voltages. The other would be a set of commonly 256 gray levels between two voltages, but for purposes of the drivers that we're talking about, it's sort of -- driver meaning IC or driver meaning output stage, that's a level of detail that really isn't discussed in these patents.

Q You had me confused now because you've talked about a driver, a driver stage and a stage separately in all different ways. Can you clarify

the meaning among those three things?

A Well, the '550 is a little confusing. It uses drivers to mean discrete integrated circuits, and it also uses the term driver to mean an output, an output stage of which there are multiple within an integrated circuit driver.

So, yes, it is confusing as a result of the language that was used in the '550 and also generally the terminology used among technologists and the context would be obvious whether it was the IC or a single output.

Q And so when you talk about a single output, are you talking about a single output from an IC driver?

A An output could mean that, yes.

Q How have you been using the term?

A I will usually -- in the declaration I was careful to call out monolithic or chip versus output or driver output. I believe I am consistent in doing that.

Q I want to understand how you've been using it already this morning. What are you referring to

when you talk about an output?

MR. BERKOWITZ: Objection to form.

A An output is a port or a signal point that is present within an integrated circuit.

Q So there could be multiple outputs on one integrated circuit?

A There frequently are, yes.

Q And the distance between those outputs, is that measured in pitch?

MR. BERKOWITZ: Objection to form, foundation.

A The distance between them? I'd have to scratch my head. I'm not sure that's a relevant parameter for driver outputs.

There is a pitch but if I were to be buying drivers, I would look at a number of electrical characteristics and pitch would be low in consideration.

Q Do you know what pitch means in a driver context?

A I do.

Q What does that mean?

A To me it means the distance between the center line of a output pad between adjacent driver stages or driver outputs.

Q In the 2004 time frame, are you aware of what the standard pitch was for driver ICs?

MR. BERKOWITZ: Objection to form, relevance, scope.

A I don't have that number on the top of my head.

Q Did you investigate that issue when you were preparing your declaration?

MR. BERKOWITZ: Objection to form.

MR. HELGE: What's wrong with the question?

MR. BERKOWITZ: He already said he's not familiar with it.

MR. HELGE: I'm asking if he investigated it in preparation for his deposition. I'd like you to answer it.

MR. BERKOWITZ: You asked him earlier before this deposition.

MR. HELGE: And I'm asking him in preparation for his declaration.

MR. BERKOWITZ: I didn't instruct -- he can answer.

MR. HELGE: One person talking at a time, please.

Q Mr. Marentic, can I get an answer to that question, please?

A I did not concern myself with pitch during this declaration. The term pitch, although used in the art, is not in the claim language of the '550 patent, so I didn't concern myself with it.

Q We talked earlier about different terms for source driver, and I think you mentioned data driver and source driver. Is that right?

A Yes.

Q Are there other terms that we could use for that same concept, those are the most common terms? Are they ever called column drivers?

A Occasionally.

Q Is there any difference between a source driver, a data driver or a column driver, in your estimation?

MR. BERKOWITZ: Objection to form.

A For a liquid crystal display, a large area displaying video the term that I've always heard is source or data driver. Column driver could be used. It's frequently used in other display technologies like plasma or polymer dispersed liquid crystal or in film electroluminescence or super-twist nematic, STN technology.

Q So in the context of LCD technology, do you believe that a source driver and a data driver are synonymous?

A Generally, yes.

Q Is there an instance where they wouldn't be synonymous?

A If you have some test cases, I'd like to look at them.

Q I just want to understand in your experience.

A In terms of the '550 patent, the patent calls out data drivers and then the claim calls out source driver, and to me the source driver refers to the data driver. Within this ball of confusion of is it an integrated circuit or is it just a driver

output.

Q In your experience, is one of those terms better than the other, is source driver better than data driver or vice versa?

MR. BERKOWITZ: Objection to form.

A Different factories will tend to call -- use one term or the other term. The IC manufacturers will use both terms, I believe, also. In the context of larger area display displaying video with a TFT active matrix array, the source and the data driver would be equivalent terms.

Q In LCD display, do the LC molecules emit light?

A No.

Q What do they do with respect to light?

A They interact with polarized light and modulate the amount of light that passes through a liquid crystal cell. The light is generated for these types of displays by backlight, and the liquid crystal pixel modulates the amount of light that reaches the viewer's eyes.

Q Is it accurate to say that liquid crystal

molecules act as a sort of shutter to allow light passing through it?

A A variable shutter.

Q Have you heard of the term ramp retrace in the context of LCD technology?

MR. BERKOWITZ: Objection, relevance, scope.

A Sitting here today, I can't recall that term.

Q It's not familiar to you?

A I can't recall it right now.

Q How about hold drive?

MR. BERKOWITZ: Objection to form, relevance and scope.

A Well, Sharp reference uses a sample and hold method.

Q What does that mean, sample and hold?

A A video signal is sampled at a specific point in time, and that sample is held on a storage capacitor.

Q What happens if you don't have a storage capacitor in a pixel, can it hold that signal in the

pixel?

MR. BERKOWITZ: Objection to form.

A There is an additional capacitor outside the Clc and the Cs parallel combination. The sampling device will have an additional hold capacitor.

Q And so am I correct in saying that that's the third capacitor that we're talking about within a pixel region?

A It's the third discrete capacitor that we've been talking about. There's some scattered parasitics that are always present but it would be a third discrete capacitor.

Q Have you seen a hold capacitor modeled in any of the documents that you reviewed for this deposition?

MR. BERKOWITZ: Objection to the form.

A To me modeled means a spice simulation. And no, I've seen no SPICE simulation for this area of the '550 patent.

Q Have you seen any graphic representations of the hold capacitor in any of these documents that you reviewed for deposition?

MR. BERKOWITZ: I'm sorry, could you read that back.

(Pending question read.)

A The Sharp reference has some capacitors that are shown. I refer to them in my report as part of the sample hold circuit.

Q We'll have to come back to that in a little bit.

Any others that you recall?

A The Sharp reference has additional embodiments where there's extra additional capacitors.

Q Is that it?

A That's all I recall.

Q So you've been talking about what you've referred to as a sample and hold circuit. Is that right?

A That's what the Sharp reference describes, a transistor and a capacitor.

Q Do you have any professional opinion as to whether sample and hold is the same thing as a hold drive?

MR. BERKOWITZ: Objection to form. I've not really heard the term hold drive. It doesn't ring a bell.

Q In your CV you talk about Alien Technology. Do you remember we talked about that last month?

A We did.

Q It says in your CV that you were involved with the design of custom drivers. Is that right?

A That's correct.

Q What kind of drivers were those, custom drivers?

A Those were drivers designed by engineers at Alien. They were for organic LED, they were for cholesteric liquid crystal and for polymer dispersed liquid crystal. They also had the additional requirement that they be roughly square or just slightly rectangular, and Alien Technology had a method of assembling silicon dye on to a substrate called fluidic self-assembly. The driver ICs, or chips, were made on a standard wafer run through standard wafer processing. They were etched and broken and the result was their shape looked like a

truncated pyramid with the circuitry transistors diffused in at the top of the truncated pyramid. The circuits were held in a fluid and passed over a substrate with the opposite shape of a pyramid, dimples, and the dye would reliably and quickly insert themselves upside down into the dimples, and we could do tremendous number of assemblies per minute. I don't remember the number, but million kind of number. And these displays were ultralow cost and they were flexible, typically for a credit card or additional security for a chipped credit card.

Q So Alien Technology produced these custom drivers for various types of displays. Were you producing and designing these drivers according to customer specifications?

A The customer was Alien. We -- as a company Alien had a customer base -- or a prospective customer base and they needed so many digits, such a size, such an optical characteristic and that would get transferred into a couple of different departments, one that was concerned with the display

material, another department with creating the dimple substrates and the department that I worked in was the IC design group and they would design the dye which would have multiple output stages.

Q Would I be wrong to characterize those custom drivers as a source driver, a gate driver, something like that?

A There was no TFT array, so the term source and gate doesn't have meaning in that context. Those would be called more segment or row drivers and digit or column drivers. I can't remember the term we used for them, but we were consistent.

Q Do you have design experience for drivers for active matrix LCD panels?

A I have experience with the custom drivers that were being in this case going to be used by Hitachi and were being designed in Silicon Valley, and I was the technical go-between between the factory engineers and Mobara, Japan, and the Silicon Valley.

Q So that's not an Alien Technology, right, that's at Hitachi?

A That is at Hitachi. There was also at Philips we were designing a couple of ICs. One was a very low cost timing controller for source and gate drivers. The other was a complex timing controller that had some enhancement, and there may have been some source drivers that were -- source driver ICs that were being developed for one of the Philips factories.

Q What do you mean --

A Excuse me. There was also -- I was the go-between for an investment in E Ink, the electrophoretic display and the design group in Philips Semiconductor out of Zurich, Switzerland.

Q When you mentioned Hitachi and Philips, you talked about a timing controller for drivers. What do you mean by timing controller?

A That would be a circuit that would talk to a graphics chip or a motherboard processor and would also communicate retimed information to the source ICs and the gate ICs.

Q So is it accurate to say that the timing controller is separate from the source IC or a gate

IC?

MR. BERKOWITZ: Objection to form.

A It is a separate integrated circuit, yes.

Q For your work at Hitachi and Philips you were involved in designing timing controllers for these drivers -- I'll ask this question again.

In your work at Hitachi and Philips, were you ever concerned with the type of signal coming into the driver for your design work?

MR. BERKOWITZ: Objection to form.

A Yes, always concerned with signal, timing, voltage levels, integrity, of course.

Q And so you'd be concerned -- when I talk about signal coming into the driver, are we talking about digital data at that point?

MR. BERKOWITZ: Objection to form.

A In the case of Hitachi it was digital data coming into the driver IC. Is there a section of the question I didn't answer? You've got a look on your face like you're expecting more from me and I'm expecting something from you.

Q Got it. I just wanted to make sure you

were done.

What about Philips, was it also digital data coming into the driver?

A It was a wide range of projects that we worked on. We pulled R&D material from Philips research and moved it into Philips factories. It was a large amount of quick-turn projects.

My recollection is most of it was digital data going into the drivers. There may have been an analog project. There were 30 or 40 engineers that reported to me, some in the U.S., some not in the U.S. As I said, there was a lot of projects.

Q And for each project you'd need to know what type of data was coming into the driver to understand the design requirement, right?

A We would have a specification that ironed down everything that we could at the onset of the design so that when the design was complete and parts made, it could be tested against the design requirements and verified to meet them, typical engineering practice.

Q In the 2004 time frame do you know the

maximum number of signal lines that could be connected to an IC driver action area?

MR. BERKOWITZ: Objection to form.

A It would depend on what the interconnect technique was, whether it was tape automated bonding or chip on glass or discrete package that was mounted on a circuit card. Regardless of what the technology is, I don't have that number at the tip of my tongue sitting here today.

Q In your declaration you say that large-sized LCD panels with pixel dimensions of 800 by 600 had multiple driver ICs.

Do you recall that testimony?

A Yes.

Q Why would you need multiple driver ICs for that pixel dimension?

A That was a common display size around that period of time. It was a standard I believe called out initially by IBM. At the time there were management manufacturers that would make driver ICs, and these driver ICs would have some number of output stages. For instance, if a source driver IC had 200

outputs, then you would need four of them to drive 800 lines, and they would be placed along a horizontal edge.

Q In the 2004 time frame was it possible to manufacture a driver IC with 800 outputs?

A Certainly it was possible to manufacture it. The question would be was it economically viable, in which case people, factories, companies that made the ICs might not go to that large a number.

My experience is there would be a few hundred outputs at that time frame so you would need at least a couple of ICs. And usually these ICs had a very high aspect ratio. They were -- the outputs along one of the long edges and two of the shorter edges, maybe a little bit the opposing edge and then the power, the data, the clock, the service signals would come in to the middle of the side away from the panel. And if there were an 800 output IC, it would tend to have this very high aspect ratio and would tend to be fragile especially in a notebook application where there was a little bit of bending

of the lid transferring a little bit of bending to the liquid crystal display, and if there was a long slender IC mounted along the top driving all 800 outputs, it would be easy to crack. Also, in a manufacturing environment it's not unusual for ICs to be hooked up to a panel, that completed panel as it would be sold to the customer turned on and burned in at a higher temperature for a period of time and failures would develop, and they'd have to be repaired. It was easier to pull off smaller individual ICs, not damage the underlying panel structure and then reattach a smaller IC.

MR. BERKOWITZ: We have been going about an hour. Is now a good time for a break?

Q Mr. Marentic, you want a break or do you want to keep going?

A Break sounds good.

MR. HELGE: Off the record at 11:32.

(A recess was taken.)

MR. HELGE: Back on the record at 11:47.

BY MR. HELGE:

Q Mr. Marentic, earlier you were talking

about the types of connections and you used a few terms that I want to clarify. Chip on glass is COG, correct?

A It's abbreviated as COG. It's a monolithic silicon dye that's made with conventional IC fabrication technology and it's attached on the edge of the panel and the inputs and outputs bonded appropriately.

Q What are the types of bonding methods that you could use?

A You could use aluminum wedge bonding, gold ball bonding, and ACF, and anisotropic conductive film.

Q Are there different types of ACF methods?

A There's different manufacturers and they have different properties, but generically they're a thermoplastic with conductive spheres, and these spheres are at such a density so that when a bumped dye is pressed against the panel, there will be multiple spheres that are connecting the bump to the corresponding pad on the panel and yet the density of the conductive sphere is low enough that there won't

be lateral shorting.

Q Are there types of ACFs -- I'll take that away.

When you mentioned properties, different properties for different manufacturers of ACFs, is temperature one of those properties?

A The bonding temperature and pressure profile and the conductivity of the spheres.

Q And do any of those properties affect whether the IC could be removed and replaced for repair?

MR. BERKOWITZ: Objection to form, relevance.

A From a manufacturing point of view the ACFs I'm familiar with can be heated up and the silicon IC removed for repair. Should a fault or failure occur late in the process when all of the money has been invested and a single line is not functioning properly rather than throw that completed display away, it will be reworked.

Q Are there any ACFs that you're aware of where heat will actually increase the bond rather

than allowing the IC to be removed?

MR. BERKOWITZ: Read back the last question.

(Pending question read.)

MR. BERKOWITZ: Objection to relevance and scope.

A There are a number of companies making ACF and a number of applications. I don't know all of the properties of all of the ACFs, but there are clever material scientists that will put together materials for use in ACF that will suit a certain application.

Q So you're not specifically aware of the type of ACF that I was asking about?

A I wouldn't be surprised if there is any.

Q But you're not specifically aware of them?

A I can't name a manufacturer and a part number here today, no.

Q Is there any other type of bonding method that we haven't talked about for chip on glass technology?

A Those are the ones that I'm aware of that

were in volume manufacture in 2004 time frame.

Q What about wire bonding?

A I mentioned those too.

Q So the aluminum wedge and the gold ball, are those types of wire bonding?

A Yes.

Q And does wire bonding allow the removal of a damaged IC?

A Yes.

MR. BERKOWITZ: Objection to form, relevance.

Q Are there properties of the wire bonding technique that affect whether the IC could be removed and replaced?

MR. BERKOWITZ: Objection, relevance, scope.

A There's a material selection in all of this, so if there is an IC put on to the edge of the panel and wire bonded, the material set around that process would certainly include materials with properties that allow rework.

Q Is that because rework is important?

MR. BERKOWITZ: Objection to form.

A Rework is -- is important. In a theoretical point of view, in an ideal world, you don't need that. In the actual factory of making displays, as I mentioned earlier, one would not be thrown away because of a single errant line. The display assembly will be repaired, different techniques, different factories, different technologies, but there would be a method of repairing a failed line in the very last stage.

Q So the concern for a rework would have been known by a person of ordinary skill in the art in 2004. Is that right?

MR. BERKOWITZ: Objection to form, foundation.

A I believe under my definition of a person having ordinary skill in the art in 2004, they would have known about rework issues.

Q Was rework -- was the concern for rework known in 2003?

MR. BERKOWITZ: Objection to form, foundation, relevance, scope.

A I first stumbled on to rework in the late '60s. It's a vulgarity of manufacturing. Everything doesn't come out identical and perfect.

Q So somebody coming up with a design in LCD technology would have considered rework as part of that design. Is that right?

MR. BERKOWITZ: Objection to form, relevance, outside of scope.

A The design of what?

Q LCD technology, LCD driver.

A An LCD driver IC?

Q Well, I think -- we're talking about rework, let me make sure I understand.

Rework is -- includes the need to be able to replace a damaged IC with a new IC once manufacturing is substantially complete. Is that right?

A That's correct.

Q And so that need to be able to replace a damaged IC is something that's known within LCD technology since the 1960s. Is that right?

A The need for rework at multiple levels,

whether it's lines in the photolithographic process, whether it's failed backlight, a failed IC, there is an awareness that there is rework that is done. I believe your earlier question hinted at exclusively IC, and the IC designer is less concerned with the rework. They make an IC that meets certain electrical and physical specifications, and their concern is yield of that dye at electrical test.

Q And that's because if you're going to rework an IC, you're going to replace it in kind, correct?

MR. BERKOWITZ: Objection to form.

A Generally, yes.

Q And so people who are making determinations about bonding methods, they will also be concerned about rework, correct?

MR. BERKOWITZ: Objection to form, relevance, scope.

A The panel design is such that repair can be accomplished at a couple of high failure modes.

Q So the designers of that panel design will have rework in their mind. Is that right?

MR. BERKOWITZ: Objection to form, relevance, scope.

A The panel designers and manufacturers will have rework considered in the product flow and final costing.

Q What about at the design stage, will they have that in their mind at that time as well?

MR. BERKOWITZ: Objection to form.

A They should.

Q You mentioned another bonding method -- I think it's bonding -- no, actually it's not a bonding method. T-A-B, TAB, can you tell me what TAB stands for?

A Tape automated bonding.

Q So is it a bonding method?

A It's a class of packaging where the silicon dye is connected to a flexible substrate and that flexible substrate is then attached to the panel edge and the circuitry wrapped around to the opposite side of the panel.

Q And does tape automated bonding allow for rework?

MR. BERKOWITZ: Objection to form, scope, relevance.

A The TAB is usually attached with ACF, so the same scenarios of loosening the ACF, heat, solvent, shock, something. The TAB method also requires rework for an economical product to be manufactured at a factory.

Q When you were talking earlier about a hypothetical 800 output driver IC, you talked about risk of damage. Where did you acquire that knowledge about risk of damage based on such a large IC?

A I might have broken some at SAIC when we were putting high performance backlights behind display LCD panels. I was certainly aware of it at Hitachi and at Philips also.

Q Do you agree that a driver IC -- well, generally speaking, do you agree that driver ICs have been improving over time?

MR. BERKOWITZ: Objection to form.

A Driver ICs have been evolving so that they meet the panel manufacturer's requirements which meet OEM requirements and can be marketed competitively

against other OEM products.

Q How have they been evolving?

A They would have used different processes, semiconductor fab processes --

MR. BERKOWITZ: Just for clarification. Why don't you just read the question back and start over.

Q The question was how have they been evolving. He said they have been evolving.

MR. BERKOWITZ: I just want to make sure she got it down correctly.

(Pending question read.)

A -- semiconductor fabrication processes, different handling methods, different data input structures.

Q So is that in order to perform more computations?

MR. BERKOWITZ: Objection to form.

A These ICs don't perform computations.

Q Have the number of output stages for one driver IC changed over time?

A Yes.

Q How have they changed?

A It generally increased.

Q Today what's a common number of output stages for a driver IC?

A I actually don't know today.

Q You knew 2004 though, right?

A There were a few hundred.

Q More than a dozen, right?

A More than a dozen for the types of large area video displays that we're talking about.

Q How would you define large area video display, just so we understand the context of what we're discussing?

A A video display would be at least the standard definition, the one prevalent since World War II. That was 525 lines by about 400, 480 lines, so that was a standard definition. And in the early days those were a few inch diagonal. Those were unsuitable for family viewing in a living room, for instance.

The need for a living room experience said that the displays needed to be at least 16, 20, 24

inch diagonal, and the number of pixels was less expensive product SKUs, the standard definition. When the high definition standard came out, there were still multiple addressabilities that were allowed under the current TV standard, I think it's ATSC, but in that time I believe the ATSC went live 2008, 2009, but in preparation TV manufacturers were trying to get larger screens, both in physical size and in pixel addressability.

So to me a large area would be at least a thousand pixels left to right and the appropriate ratio up and down to meet the 4 by 3 or the 16 by 9 aspect ratio, and at least some diagonal of 16, 20, 24 inches that would allow for almost multiple viewers to watch it.

Q Two LCD panels of different sizes can still have the same number of pixels, right?

A Yes.

Q So the number of pixels is not always variable with the change in size, correct?

MR. BERKOWITZ: Objection to form.

A To some degree both are independent. It

relates to a particular factory's mother glass size, and that's the starting glass that goes into the factory. For a given factory they can fit so many displays on the mother glass and have a less than optimal number or size of substrate LCDs flowing through the TFT fabrication process would cause a price increase for that particular size. So each factory has optimal sizes that they're able to run.

Q And you mean optimal size based on the physical dimension of the glass, right?

A The physical dimension.

Q Is it true that there is an electrical circuit element that drives each gate line and source line?

MR. BERKOWITZ: Objection to form.

A I think I understand that. Would you repeat it?

Q Sure. Is it true that there is an electrical circuit element that drives each gate line or source line?

A There is a cluster of electrical components that drives each source line and gate line.

Q What is that cluster of components called?

MR. BERKOWITZ: Objection to form.

A That could be an output driver.

Q Is there any other term that's used for that.

A Well, we've talked about some of those earlier. Output stage, output of a driver IC.

Q What about a buffer?

A A buffer is a narrowed definition of a circuit. Typically the input equals the output. Occasionally it can be inverted, hence the term inverting buffer. Occasionally the output impedence is low, called a stiff buffer. Sometimes it just cleans up a signal and there's no particular need to have extra driving strength.

Q In a LCD panel is there a need for extra driving strength on a column line or gate line?

MR. BERKOWITZ: Objection to the form.

A The TFT array will have been modeled prior to fabrication with certain line capacitances and line resistances and target output specifications. Frequently the manufacturer of the whole LCD assembly

who designs the TFT array would have a range of suppliers that they buy from, and they would be able to give an early specification to the manufacturers to let them know what they were looking for in terms of drive characteristics. And reciprocal is also true, the manufacturers of the driver ICs would have preliminary specifications that they would send out to industry outlining the characteristics of their new driver IC. So that when it was time to deliver prototype displays to an OEM manufacturer, they would be able to have close to final display performance.

Q What would happen if you had an LCD panel that demanded a certain driving strength and a driver IC that could not provide the requisite driving strength?

MR. BERKOWITZ: Objection to form.

A The display manufacturer could search for other drivers. If the particular company had in-house capability, they could modify an existing design. And depending on what type of technology the LCD active matrix fab had available, they might be able to come up with a merged solution.

Q So you understand the hypothetical I'm presenting, right?

A I think you're arriving at -- you selected an IC, you've designed a panel, the two don't work together and you're proposing putting a buffer at each output to lower the output impedence as it appears reflected into the source lines. That's a pretty far hypothetical.

Q All right. I think you've gone a little bit further than I had intended. What I'm really thinking about is an LC panel that has a certain need for drive strength, right, you talked earlier about drive strength, and then a source driver has been provided that does not have the requisite drive strength.

Now, follow me with this hypothetical. These two components are assembled together and then tested. What would happen in the pixel region when an insufficient drive strength is provided from the driver IC, how would that affect the display?

MR. BERKOWITZ: Objection to form.

A Well, this is a hypothetical. I think I'd

want to think about that a little bit more. That's a good question.

Q Is it possible that the necessary gray scale would not be achieved within a frame under that hypothetical?

MR. BERKOWITZ: Objection to form, relevance, scope.

A Another good question. I'd like to study that closer and have some discrete numbers, what driver and what's the active matrix, input characteristics, what's the timing, what's -- what's available. Part of it is the -- I'd like to look at it. Another good scenario. It's intriguing to me. I'd like to sit down and examine it.

Q So is it correct that these sorts of things don't happen in panel manufacturing; is that right?

MR. BERKOWITZ: Objection to form.

Q I'll ask the question again.

Is it correct that source drivers and panel displays are always compatible?

MR. BERKOWITZ: Objection to form.

A The first time they're hooked up, they may

not function properly. Sometimes some compensation can be made in other portions of the process. Sometimes -- there's a range of solutions available for the -- within the factory that builds the final LCD modules, the TFT array, driver chips, the backlight, and that gets sold to an OEM that would incorporate it in a monitor, television, notebook computer.

Q So you mentioned that the first time these components are connected together they may not function properly. Is it possible that the image may decay during the frame because voltage isn't maintained?

MR. BERKOWITZ: Objection to form.

A There is a whole array of visual artifacts in displays and they're called by fairly creative terms and they're certainly not uniform across the industry. In fact, I worked at one place where within the factory there were two buildings and both buildings called visual artifacts by different names.

So your description of graying and decaying, I wouldn't even hazard a guess as to what

that would look like. The only way to look at visual artifacts is with a pair of eyeballs. Words never do it justice.

MR. BERKOWITZ: What time you think you're going to break for lunch?

MR. HELGE: That's what I was just wondering.

Q Mr. Marentic, do you want to take a break or do you want to go a little bit longer?

A Maybe another five, ten minutes.

(PREVIOUSLY MARKED Deposition Exhibit 1009 marked for identification and was attached to the transcript.)

Q Mr. Marentic, I'm going to hand to you what's already been marked as Sharp Exhibit 1009 in this case. Does this document look familiar to you?

A Yes.

Q And what is this document?

A This was Exhibit 9 in my declaration.

Q So you reviewed this document in preparation for your declaration. Is that right?

A For the declaration, yes.

Q But you didn't review it again in preparation for deposition, right?
A Correct.
Q Do you recall who found this reference when you were preparing for your declaration?
MR. BERKOWITZ: Objection to the form, relevance.
A This was provided to me by ARE.
Q Do you see three inventors listed on the cover page up near the top left?
A Yes, I do.
Q Do you know any of those inventors?
MR. BERKOWITZ: Objection, relevance.
A I don't recognize any of those three individuals.
Q Do you know Patrick Burns at Greer Burns & Crain, Ltd.?
A I don't believe I --
MR. BERKOWITZ: Objection, relevance.
Q I'm sorry, Mr. Marentic?
A I don't believe so.
Q Can you please turn to Page 10. The bottom

of Page 10, left-hand side we have Paragraph 8 which then continues up to the top of the right-hand column.

Do you see that?

A Yes.

Q If you are on the top of column 2, the right-hand side about five lines down, there's a sentence that begins with the word "especially."

Do you see that?

A Yes.

Q Do you see that that sentence -- I'm going to read a portion of this out loud: "Especially along the upsizing of the screen the number of the driver ICs will be increased."

Did I read that correctly?

A Yes.

Q Is that always the case?

MR. BERKOWITZ: Objection to form.

A We've talked earlier about increasing the screen size. This is another one of those imprecise terms. Screen size can relate to physical diagonal or the screen size can refer to the addressability,

the number of pixels by the number of pixels.

Q So, Mr. Marentic, is it true that changing the size of the screen does not necessarily require a change in the number of driver ICs?

MR. BERKOWITZ: Objection to form.

A Changing the screen physical size slightly would not require a change in the number of ICs. Changing the screen size considerably, doubling it, might require different ICs, and those different ICs may have a different number of outputs. So there would need to be a different number of driver ICs along the edge.

Q So your conclusion about the differing number of driver ICs along the edge is dependent upon the required number of outputs, right?

MR. BERKOWITZ: Objection to form.

A It's based on the matching of the output characteristics of a driver to a line -- source line of an LCD with a TFT array and, similarly, that would be the case for the gate side also.

So there's no -- my sense is you want a yes/no answer and there is no yes/no answer. These

are tradeoffs that are made based on requirements of what does the panel need, what can the IC drive.

If the -- if the panel were to grow left to right, it would be a case where extra ICs would be added and they would be the same as the ICs on the original section of the panel.

Q Why would you need those extra ICs if the number of scan line -- excuse me -- if the number of data lines has not changed?

A I assumed the number of data lines was changed so the format of the display was 800 lines left to right and that was increased to 1,024 kind of number. It would be normal to take the same IC that was driving the 800 and apply more of them so that you got to the 1024 number of driven lines, and that would be just using the same driver IC, driving the same source line, except there are additional source lines, and there would be no unexpected changes in the performance.

Q Sir, if you had two panels of different physical dimensions but both with 800 source lines, those two panels could have the same number of driver

ICs, correct?

MR. BERKOWITZ: Objection to form.

A In one case they could and in one case they might not.

Q Do you see Paragraph 6 on the left-hand side, last sentence? I'm going to read this allowed: "Therefore, in order to drive many gate bus lines and the source bus lines on the display circuit board, the plurality of the gate drivers and source drivers must be connected to the area around the liquid crystal display panel."

Do you see that?

A Yes.

Q Do you agree that if the number of source lines can be provided by one driver IC, then you wouldn't need a plurality of source drivers?

MR. BERKOWITZ: Objection to form.

A It depends what the electrical load of the TFT array is, both the source line and the gate line, and it would depend on what was available for source drivers and whether that source driver was suitable for driving each of those.

MR. HELGE: Probably good time to break. Off the record at 12:41.

(A lunch recess was taken.)

MR. HELGE: We're back on the record 1:36.

BY MR. HELGE:

Q Mr. Marentic, I'm going to hand you --

A Could I go back to the last couple of minutes prior to lunch?

Q Okay.

A We had talked about the Sekido and you read a single sentence outside of Paragraph 8, and generally this patent is for reduction in electromagnetic interference or EMI or they call it electromagnetic wave. And there is a description in Paragraph 8 that the higher resistance and capacitance and the lack of ground wiring means that when the service signals to the source drivers and gate drivers go at frequencies that are required, there's a lot of electromagnetic noise, and that's a concern with all flat panel displays. Liquid crystal displays are not unique, but the paragraph that you -- or the sentence you read, especially along the

upsizing of the screen, the number of driver ICs is increased and further the signal lines for propagation of the signal clock and control becomes longer so that power consumption in the electromagnetic wave is increased. So it generally as a display has a larger number of lines and if you define the number of lines as the display size, as more and more ICs are added, there will be more parasitic capacitance and resistance to deal with and more of the EMI.

So I think there was questions along the line of a screen and upsizing the screen, what does that mean. The upsizing the screen could be physical size or the addressable matrix size. If the one axis were to increase in size, then it would be normal to add extra driver ICs onto it and with that would come more electromagnetic interference.

There was also some discussion on the strength of the driver ICs and the requirements of the panel. There isn't a hard threshold where if you add another line suddenly the displayed performance deteriorates to unusable. It's a gradual change.

And there may be some applications where for a low cost product that might be acceptable.

So that's a long-winded explanation of -- it's a complex trade space and there's many design options that are available. If a product is late for introduction, there could be some accommodations elsewhere in the liquid crystal gap, in the liquid crystal chemistry or with some other wiring changes in the timing controller to make it meet the end customer's requirements.

Q So matching a driver IC with a panel requires compatibility of many different factors, right?

A Many different factors. However, it is common if a factory has an existing supply chain of drivers coming in and a notebook manufacturer comes to them and says we would like to have this size panel, would you be able to do it, and they'll look at it and possibly use the same drivers even though it's larger. They would add more drivers.

Q If necessary, right?

A If necessary, yeah.

Q And they would look at more than just the panel size to determine if a driver was compatible with a panel array?

A The matrix size would be of paramount importance and then the load of each source line presented to the driver would need to be considered and then also the end customer's requirements. Some customers have LCD technologists on their staff and they have a series of tests that they look for artifacts. Other display -- other OEM manufacturers will just take a display at the lowest price they can get and put it out into the marketplace. So there's a range of what OEM users will accept.

Q Mr. Marentic, why don't we take a look at Exhibit 1007 here.

(PREVIOUSLY MARKED Deposition Exhibit 1007 marked for identification and was attached to the transcript.)

Q Mr. Marentic, does this document look familiar to you?

A This is my declaration from last March on the '550 patent.

Q So if you turn to the last page of this document, that's your signature there?

A Yes, it is.

Q And you read this entire document before you signed it, right?

A Yes, I did.

Q And you read the entire document in preparation for this deposition, correct?

A I did. I concentrated principally on the arguments of obviousness of Sharp and Kamizono.

Q Why did you focus on that portion of the declaration?

A Because the Patent Trial and Review Board instituted the review based on those two prior arts.

Q You're free to reference this document if you'd like in answering the question, but what is it that's missing from Sharp that we then look to Kamizono to provide in this ground that's been instituted by the board?

MR. BERKOWITZ: Objection to form.

A I believe Sharp shows everything, also noteworthy it was ten years prior, but if an argument

is made that somehow Sharp doesn't adequately teach multiple driver ICs, then Kamizono clearly shows multiple driver ICs and describes how to mount and rework those.

Q So is it correct that we're only relying on Kamizono to provide the plurality of driver ICs; is that right?

MR. BERKOWITZ: Objection to form.

A No, I believe Sharp shows everything, but if an argument is made that it doesn't, then there's no question that Kamizono does.

Q You understand that the board did not institute on the ground based solely on Sharp, correct?

MR. BERKOWITZ: Objection to form.

A Would you ask that again, please.

Q You understand -- I'll say it one step at a time.

You understand that there was a ground presented against claims of the '550 patent based solely on Sharp, correct?

MR. BERKOWITZ: Objection to form.

A There was -- again, I'm sorry. The question again?

Q Well, you're referring to Paragraph 5 of your declaration, correct?

A Yes.

Q And do you see Paragraph 5a where there is an anticipation argument based on what's called the Sharp reference or Exhibit 1002? Do you see that?

A I do, and I was questioning whether you were including anticipation as invalidation or obviousness, and my ear wasn't attuned to it.

Q Understood, understood. So you see Paragraph A is an anticipation argument based on the Sharp reference and Paragraph B is an obviousness-based argument in view of the Sharp reference, correct?

A I do.

Q You understand that the board did not institute on those two challenges, correct?

MR. BERKOWITZ: Objection to form.

A The board did not rule that those were not good arguments. They just chose to implement on

Sharp and Kamizono. I don't see Claims 1 through 5 are invalid as obvious.

Q I'm sorry, can you explain your last sentence? You don't see that Claims 1 through 5 are obvious?

A The board ruled that this case should pursue Claims 1 through 5 invalidity as obvious in view of Sharp and Kamizono. The others, A, B and D, were just passed over.

Q Okay, that's fine.

So I want to come back to something you said earlier, which was, if an argument is made that Sharp doesn't disclose everything, then it's in Kamizono. What I want to understand is what you mean by argument.

A So, for instance, my Paragraph 130 shows that Sharp shows path to an integrated gate driver, as is required by the fifth claim, and Kamizono also shows and discusses an integrated gate driver. So both of those could be used for Claim 5.

Also, Paragraph 98, the Sharp reference anticipates Claims 1 through 3.

Q Mr. Marentic, you understand that ground has not been instituted by the board, correct?

A You're correct.

Q Can I ask you to turn to Paragraph 148 -- actually 147 as well. Do you have those there?

A I do.

Q Why don't you read through 147 and 148 to yourself and let me know when you finished.

A Okay, I've read both of those.

Q So based on those paragraphs, or any other portion of your declaration, what modification are you proposing to the Sharp reference based on Kamizono?

A It's not a modification, rather -- or an argument made that somehow Sharp shows only one source driver, Kamizono extends that to show that were it not obvious, there is documented a method of Kamizono to extend that and use multiple driver ICs.

Q So you're not proposing a modification to the Sharp reference based on Kamizono. Is that right?

MR. BERKOWITZ: Objection to form.

A I'm not suggesting that Sharp reference needs to be modified. I believe the Sharp reference shows multiple drivers, which is what's required in Claim 1 and 2 of the '550. I believe the Sharp reference teaches multiple drivers, multiple gate drivers, multiple source drivers, and that somehow if an argument was made that Sharp only taught a single driver with multiple outputs, then Kamizono would teach that you could take multiple ICs each with multiple driver outputs and put them on the edge of a panel.

Q So are you relying on Kamizono solely for the number of driver ICs that are shown?

MR. BERKOWITZ: Objection to form.

A No. If -- I believe Sharp shows multiple drivers, as required in Claims 1 and 2, but should driver be argued that is Sharp only shows one driver for some reason, I would disagree with that. Then Kamizono clearly shows that for an LCD you could have multiple drivers.

Q So are you using Kamizono solely for the definition of driver?

MR. BERKOWITZ: Objection to form, foundation.

MR. HELGE: How is that a foundation objection?

MR. BERKOWITZ: It's not clear what claim you're talking about.

MR. HELGE: I'm talking about ground 3 based on Sharp and Kamizono, which applies to all Claims 1 through 5.

Q I want to understand, Mr. Marentic, exactly why you need Kamizono. As I understand your testimony now -- and we don't have to go through it again if it's the same testimony -- but as I understand it right now, the only reason you're looking to Kamizono is for the number of drivers shown in the reference.

Is that correct or not?

MR. BERKOWITZ: Objection to form.

A No.

Q What else are you looking for from Kamizono?

A I believe Sharp shows multiple drivers --

Q You understand that the board did not institute on ground 1 based solely on Sharp, correct?

MR. BERKOWITZ: Objection to form.

A I do.

Q So what else are you relying on Kamizono for?

A There is the plural/singular of what driver, drivers, plural, means and there's also ambiguity as to what a driver means. Is a driver an output or is a driver an IC or a collection of circuitry?

So if an argument is made that somehow Sharp only shows a driver, I disagree with that, but if an argument is made that Sharp only shows a driver, then Kamizono teaches that you can put multiple drivers on a panel edge were that not obvious to a person having ordinary skill in the art in 2004, and I believe that would have been self-evident. You have more lines, you need more circuitry to drive the lines, and you can use driver chips with more outputs, you can use more driver chips. It's a design tradeoff based on cost,

performance, time to market.

Q But you're not looking to modify Sharp with Kamizono at all. Is that right?

MR. BERKOWITZ: Objection to form.

A I believe Sharp teaches everything that's necessary to invalidate Claim 1 and 2, but should an argument somehow be made that Sharp only shows a driver, then I rely upon Kamizono to demonstrate that you can have multiple drivers on a panel edge.

Q How would the Sharp reference implement multiple drivers in the panel edge?

MR. BERKOWITZ: Objection to form.

A I believe it already shows multiple drivers.

Q So it's your testimony that you don't need Kamizono to reach Claims 1 through 5?

MR. BERKOWITZ: Objection to form.

A It depends on the final resolution of what a driver is, and if a peculiar argument is made that somehow Sharp does not show multiple drivers, and I disagree with that, then I would use Sharp in combination with Kamizono to show that one having

ordinary skill in the art in 2004 would be able to very easily understand you could put multiple drivers on a glass edge and increase the addressability size of an LCD active matrix display.

Q And to put multiple drivers on the driver edge, would that look like what's in Kamizono -- in Kamizono's figures?

MR. BERKOWITZ: Objection to form.

A It could, depends what the interconnect technology is. Or in the case of 4 and 5, what the gate structure looks like.

Q Mr. Marentic, you've said a number of times that if an argument is made, you would look to Kamizono to show that you can use multiple driver ICs. Did I understand that testimony correctly?

A Yes, I believe I've tried to be consistent and say the same thing multiple times.

Q It's almost like you had it memorized.

A I feel a little stressed and I feel the need to be very precise and I like my first answer, so I see no need to deviate from it.

Q So let me ask you this. If an argument is

not made about the number of drivers in Sharp reference, is there any need to look to Kamizono?

MR. BERKOWITZ: Objection to form.

A It just adds for Claims 1, 2 and 3 an extra layer of insurance, and then for Claims 4 and 5 Kamizono was relied upon for the integrated driver and the chip on glass.

Q And the insurance that you're talking for Claims 1, 2 and 3 relates to the number of drivers only. Is that right?

A It relates to what a driver is, and there can be some future definition of what a driver is. And I believe no matter what definition, the '550 Claims 1, 2 and 3 are invalid as are 4 and 5.

Q So Mr. Marentic, I just want to make sure I understand what you're saying.

Kamizono is being used for insurance to show that multiple driver ICs could be used for Claims 1 through 3. And your testimony on that has been that if an argument is made about the number of drivers shown in Sharp. And so if no argument is made about the number of drivers in Sharp, do we need

to look to Kamizono at all --

MR. BERKOWITZ: Objection to form.

Q -- for Claims 1 through 3?

MR. HELGE: I understand that's objectionable.

MR. BERKOWITZ: I have other grounds for it but ...

A If I refer to my claim chart at the top of 56, for instance, Claim 1, the requirement is that M groups of data lines connected to source drivers and insulated with each other, and then they go through and describe this even/odd combination. So the Sharp reference discloses groups -- two groups of source bus lines connected to source driver 71.

Then reading on, the groups of the data lines are insulated with each other by being spaced apart from and parallel to each other. The first and the second source lines -- source bus lines 5 of the first group of source bus lines are respectively connected with the sources of all of the thin film transistor 7 on the even and odd rows and similarly the first and second bus lines 5 of the nth group are

respectively connected, and it goes on.

So I believe Sharp anticipates the structure that was described in the '550 patent by a long time, and then additionally Kamizono describes signal lines connected to multiple driving ICs.

So it's really the -- I'll leave it at that.

Q So in this chart for Claim 1 you rely on Kamizono for multiple scan line driving ICs and multiple signal line driving ICs, and that's all I see. Are you relying on those for anything else -- excuse me, are you relying on Kamizono for anything else?

A In Claim 1, later on the second page, yes, I'm relying on Kamizono as it's described in the claim chart to demonstrate that the '550 is anticipated by the Sharp in combination with Kamizono.

Q Is there anything that you've left out of this claim chart for your reliance on Kamizono?

MR. BERKOWITZ: Objection to form.

A I don't believe so. Both are -- actually

all three references are for larger video displaying LCDs and both the Sharp and the '550 patent relate to overcoming certain visual artifacts and both describe this even/odd gate combination, and Kamizono also describes how to apply multiple ICs in the case of the larger displays for video, television.

Q And you're not relying on Kamizono to modify Sharp reference at all. Is that right?

MR. BERKOWITZ: Objection.

A I'm relying on Kamizono to -- let's look at Kamizono, Figure 15 -- I could find it faster in Kamizono.

Kamizono shows multiple drivers should a driver be defined as an IC and each IC has multiple outputs.

Q And so are you proposing a modification to the Sharp reference based on that teaching?

MR. BERKOWITZ: Objection to form.

A I'm not suggesting that the Sharp reference be modified at all.

Q So are you relying on Kamizono to disclose what is meant by the term driver?

MR. BERKOWITZ: Objection to form.

A No. I believe -- we discussed earlier the ambiguity not only in the '550 but in the industry of precisely what a driver means.

Q And you stand by that prior testimony, right?

A I do.

Q Can you turn to Paragraph 149 of your declaration, please. It's on Page 52. You see that paragraph there?

A Yes.

Q In the second sentence you state, "Moreover, for the reasons discussed above, there was a clear motivation to combine these references."

What did you mean by "clear motivation"?

A Both were directed to larger active matrix displays that were used for video images, television, DVD playback, suitable for family viewing. There was a need in the marketplace to increase the size in 2004. In 2004 plasma was able to easily achieve larger diagonal displays. Liquid crystal industry at that time was a little behind, and as they tried to

increase the size physically and addressability, there were difficulties that were encountered. And true to the liquid crystal industry, the engineers came up with a number of techniques to overcome these.

Sharp describes one of the techniques of hooking up the TFTs in alternating rows as one technique for an apparatus to get rid of -- or help eliminate visual artifacts.

There was a market need, there was competition by plasma, there were artifacts as you increase the size of the screen in both physical size and in addressability, and those needed to be solved.

As I say in the first sentence, Kamizono teaches the use of multiple source and gate drivers, as does the Sharp reference, and the Sharp reference discloses all the other limitations of Claims 1 through 3, as shown in the above claim charts.

So, thus, to the extent that the Patent Owner argues that the Sharp reference does not teach multiple gate and multiple source drivers, which is contrary to my opinion as we've discussed here quite

a few times, I believe that, as a minimum, Claims 1 through 3 of the '550 patent are obvious over Sharp in view of Kamizono.

So there was a motivation to combine of adding extra ICs for a larger addressable display matrix size and it would have been well within a person having ordinary skill in the art in 2004 to add extra drivers, and were that not just obvious from prior work, one could look to Kamizono.

I believe that, in my experience, if you need extra lines driven, you get extra ICs. I came across that in college in the sixties and, as an example, if there was a quad NAND gate and you needed a bus of eight bits, you would use two quad NAND gates. It just was taught in school, it would have been obvious. And if some kind of argument is made that somehow Sharp does not teach multiple drivers, that somehow they teach only one driver with multiple outputs, then Kamizono, as a minimum, teaches the commonsense that you would add more drivers to extend that addressable matrix size.

Q Do you know the priority date for the Sharp

reference?

MR. BERKOWITZ: Objection to form.

A I could look through here and find it. I know I wrote about it in the reference. My recollection is it was about a decade earlier, but let's find the precise date.

Q Do you want me to give you the reference? You can just talk about Sharp if you'd like.

A Show me what paragraph --

Q Well, this is Exhibit 1002.

(PREVIOUSLY MARKED Deposition Exhibit 1002 marked for identification and was attached to the transcript.)

A There's some legal items in terms of priority date that I'm not that familiar with. I'd like to find out what I wrote in the Sharp reference.

Q Well, Mr. Marentic, I'll withdraw that question about the priority date because I'm not concerned about the legal implication. If you look at Exhibit 1002, second page, does this -- this looks like the Sharp reference to you, correct? Let's confirm that first.

A Yes, this is the Sharp reference.

Q If you look at the middle of Page 2 on the left-hand side, do you see a filing date there?

A Yes.

Q What date is that?

A That date is May 10, 1995.

Q And in the 1995 time period what was the maximum size for an LCD panel?

MR. BERKOWITZ: Objection to form.

A In the '95 time frame LCDs with TFT arrays were principally used in notebooks, the largest market share was for notebooks. There was the start of some displays getting larger and used for monitors. They cost a premium over an old CRT, and there were some of the companies showing television at technical conferences.

So there's what was manufactured in volume, what was specialty manufactured that would be used as learning so that it could ramp up later into other product lines, and then there was what was cooking in the back lab in the R&D group.

So your question of what's the largest is

kind of ill-defined.

Q Well, with those three categories that you just mentioned, basically a commercially available panel and then sort of -- I take that as being for notebook computers maybe 15 inches, do you think?

MR. BERKOWITZ: Objection to form.

A I don't recall precisely, but XGA was a very popular size.

Q And what is XGA?

A 1024 by 768.

Q That's a pixel dimension, right?

A That's an addressability dimension.

Q Would you call that a resolution?

A There were a couple of lawsuits over what's resolution with an LCD display. It is -- the best technical term is the addressability size.

Q Do you recall in the 2004 time frame how many lines were contained in your standard high definition LCD panel?

MR. BERKOWITZ: Objection to form, scope.

A I don't recall exactly but there would still be these same categories: What was sold to the

mass market still at a premium, what was sold to the enthusiasts where price is really not an object, and then what was available in the R&D facility and shown in technical conferences, and I ...

Q In the 2004 time frame were there LCD panels being manufactured with addressability numbers of 1024 by 768?

A Yes.

Q And so that number means that in 1995 an XGA panel would have the same number of scan lines and signal lines as an LCD panel in 2004 having the same addressability, correct?

MR. BERKOWITZ: Objection to form.

A In 2004 at the time of the '550 patent, there was this even/odd configuration of rows. So that would require additional drivers on the source side to drive each and every row -- I'm sorry -- additional source drivers to drive every other column or source line of the TFT array.

Q But isn't that what's shown in the Sharp reference too, even/odd --

A It is, the wiring of the pixels was the

same on the TFT array size.

Q So the number of signal lines in an XGA notebook monitor having a 1024 by 768 addressability value in 1995 would be the same as the number of signal lines in an LCD panel having 1024 by 768 addressability in 2004, correct?

MR. BERKOWITZ: Objection to the form.

A If that was for a notebook panel, yes. If it were for a video panel, it may have had additional drivers, as is disclosed in the Sharp and as the '550 wires, the TFTs.

Q How come a notebook panel is not a video panel, according to your words?

MR. BERKOWITZ: Objection to form.

A The notebook panel uses the majority of Windows or a Macintosh operating system and is for productivity enhancement, uses an office suite that includes a word processor, a presentation program, a spreadsheet, sometimes project management, and these are stationary images where the data is typed in or a window collapsed and expanded.

So there is no particular video requirement

nor an expectation that video would look really good on LCDs and notebooks.

Additionally, notebooks had a little bit different color filter, a little bit different backlight so that the battery life was increased and, as such, the color gamut wasn't as good as state-of-the-art television monitors of today.

So the expectation of showing video on a notebook is not high.

Q But a notebook display is capable of displaying video, right?

A Depending on the program, the operating system, the performance of the rest of the components in the notebook, you can display video. It would be -- one could argue what's acceptable and what's not acceptable. It would be less technically perfect when compared to 2004 state-of-the-art television monitor.

Q So based on your claim chart that addresses the combination of Sharp and Kamizono, you're relying on Kamizono for the number of source drivers and gate drivers.

Is that right?

MR. BERKOWITZ: Objection to form.

A No.

Q So you're not relying on Kamizono for the number of source drivers and gate drivers. Is that right?

MR. BERKOWITZ: Objection to form. Wait, hang on a second. You've asked this question a dozen times today. If you want to keep asking it, you have to call the board. This is a little bit out of control.

MR. HELGE: First of all, we know that today is Veterans Day. I don't think the board is open. So my question to you is: Are you going to stop the deposition because I'm asking this question?

MR. BERKOWITZ: I'm not going to stop the deposition, but this is completely inappropriate, just for the record. You've asked him at least a dozen times the same question. He's answered it. I'm not sure what else you're looking for at this point. At this point you are harassing the witness.

MR. HELGE: I totally disagree because --

MR. BERKOWITZ: Go ahead.

MR. HELGE: -- I'm trying to get a clear answer.

BY MR. HELGE:

Q You're either modifying Sharp with Kamizono or you're not?

MR. BERKOWITZ: Are you testifying?

MR. HELGE: I'm asking the question.

MR. BERKOWITZ: Again, if you want to continue this, we'll bring it up with the board later.

Q Mr. Marentic, if I ask that question again, do you have a different answer?

MR. BERKOWITZ: Let me finish. We will move to strike the rest of this. This is completely inappropriate. Go ahead.

A I believe Sharp in the paragraph we just went through that I was searching for earlier --

Q Are you referring to Paragraph 149 -- Mr. Marentic, I'll withdraw the question.

Is there any change that you would like to make right now to your declaration in the ground that

you are presenting based on Sharp reference and Kamizono?

MR. BERKOWITZ: Objection to form.

A For Claims 1 through 3, no.

Q Let's take a look at Exhibit 1002, Page 18, this is the Sharp reference.

A 18 of 40?

Q That's correct.

Do you see Figure 13 on that page?

A I see Figure 13.

Q Do you see reference numeral 120?

A I see 120.

Q Do you know what reference numeral 120 represents in the Sharp reference?

MR. BERKOWITZ: Objection, relevance, outside the scope.

A I'd search through the text and try and find 13 and around it should be ideally 120.

Q Take a look at Page 40, Paragraphs 17 and 18, which are on the top right-hand column.

A My 40 --

Q I'm sorry, Page 4 of 40, top right,

Paragraphs 17 and 18.

A Okay. Okay, I've read Paragraph 17 and 18. These refer to another embodiment that I didn't select. I believe there were eight embodiments, and the seventh embodiment was the one that was closest.

Q So you're not relying on Figure 13 for your challenge, correct?

A I don't think so.

Q So element 120, did you see what Sharp reference refers to element 120 as?

A A transfer circuit.

Q And do you see that element 120 includes a -- actually a number of triangles, one of which is referred to as element 118; you see that?

A Yes.

Q And do you know what Sharp reference uses to describe element 118, what terminology?

MR. BERKOWITZ: Objection, outside the scope, form.

A Sharp is fairly consistent in their numbering. I haven't looked at this in a while, but that 118 they call a buffer circuit, looks to be a

buffer, doesn't have a little circle on the output, so I'd say it's a non-inverting buffer.

Q Do you see what Sharp refers to as element 105? It's right below 118 in the figure.

A In this figure they call 105 source bus lines.

Q Do you understand those to be the source lines that supply voltage to the TFT matrix?

MR. BERKOWITZ: Objection to form, relevance, outside the scope.

A I'd like to read through and make sure that that is the case. Sharp disclosed a number of different ways of driving source lines in a TFT array. Some were polyphase clocks, some were, as you called out in 13, kind of a double sample hold. 9 shows another method where there's a buffer at each pixel site. There's really a number of things that they disclose.

In the case of the 105, I'd want to go through and make sure everything is similar to item 5, which is what's used in Figure 10, which is what I used in the analysis.

Q Would it make it easier if I asked you a question that dealt with item 5?

A Yes.

Q Let's take a look at Figures 8 and 9 on this same page. You just referred to Figure 9 specifically, which shows a buffer circuit 67 in the pixel region, correct?

MR. BERKOWITZ: Objection to form. Again, outside the scope.

A What I'm doing is going back and verifying that 67 is, in fact, a buffer.

Q Are you on Paragraph 124?

A No, I'm not there yet, but thank you for the help. Yes, 67 are called buffer circuits.

Q Why would there need to be a buffer circuit -- I don't want to ask that.

From your professional experience, why might there be a buffer circuit arranged in each pixel region?

MR. BERKOWITZ: Objection to form, outside the scope.

A I'll have to read through this a little bit

closer, but this looks like an embodiment for, again, a larger area display, higher pixel content, and as it increased in size there was some visual artifacts. This disclosure has eight different embodiments. The one we're looking at is embodiment 6, which is not the one that I chose for the analysis.

Q So your answer is, you don't know the answer unless you read through. Is that right?

A I'd like to read through and get comfortable, not speculate.

Q So if you answered now, it would be speculation about the purpose of a buffer circuit in each pixel region of Figure 9?

MR. BERKOWITZ: Objection to form.

A Well, if we were sitting around coffee and just talking, I'd be fine speculating or using my opinion, but since we're in a formal deposition, I'd like to be really sure of my answers, so I'd rather not answer. It's also an item that I didn't use in the analysis of invalidity, and I haven't really looked at this section closely since March.

Q Let's take a look at Figure 10 on Page 19.

Just for the record you're looking at the annotation of Figure 10 in your declaration rather than Figure 10 in Exhibit 1002, correct?

A I am. It's on my report, Page 29. It's the same figure. It used the Japanese figure. It seems to be clearer and then expanded and then it was later annotated. So I can read the numbers, the small callouts a little bit better.

Q Do you speak Japanese?

A I do not.

Q Do you read Japanese?

A I do not.

Q So you're relying solely on the English translation for the description of the Sharp reference. Is that right?

A That is correct.

Q Take a look at Figure 10. Do you see elements 77, 78, 79 and 80?

A I do see those.

Q What are those?

A I believe those are buffers.

Q Why are those included in Figure 10, why

does Sharp include those?

MR. BERKOWITZ: Objection to form.

A For the design they had they thought there should be a buffer there.

Q What purpose would those buffers provide?

MR. BERKOWITZ: Objection to form.

A Those buffers would charge up the Clc and the Cs capacitances when each particular TFT is energized, and they would help reduce a voltage change as the video image changes. They would help ensure an accurate voltage as presented to the column lines -- I think those are 5.

Q At the top of Figure 10 there are three lines going into element 10: SP, CK and /CK, maybe inverse CK?

A Bar CK.

Q What do those three elements represent?

A The drive clock is clock and bar clock, the SP -- I believe they just call it out as a signal input to the shift register.

Q What do they refer to element 10 as?

A The shift register.

Q Outputs from shift register go to element 72. Is that correct?

A 72 and 72A.

Q And what is 72?

A 72 is a AND buffer, and circuit.

Q What about 72A?

A 72A is an inverter.

Q And the output from 72 leads where?

A It leads to the two sampling transistors 19 and 20 in the case of driver 1, and AND gate 2 the output leads to sampling transistors 21 and 22.

Q Does it lead to the source of those transistors?

MR. BERKOWITZ: Objection to form.

A The gate output for the AND output is connected to the gates at those transistors.

Q Do you see line 73?

A Yes.

Q What is that?

A That's the data signals 73 and 74.

Q So the analog voltages that are being delivered to signal lines 5 are coming from where?

MR. BERKOWITZ: Objection to form.

A They're coming from the sample hold circuit 29, 24 combination, 25, 20 combination, 21 -- there's another sampling capacitor there. It's not on this figure.

Q Let's focus just on the first column and that way we don't have to worry about that second column of capacitors.

Is that okay?

A Okay.

Q So the analog voltages to signal lines 5 in the first column come from the sample and hold circuits that you just identified, including a combination of the TFT and the capacitor in each -- in each line.

Is that right?

MR. BERKOWITZ: Objection to form.

A It comes from transistor 19 and capacitor 24, it's not clear that 19 is a TFT.

Q Where does transistor 19 and capacitor 24 receive the analog voltages that are then to be applied to signal line 5?

MR. BERKOWITZ: Objection to form.

A The signal line 73 is sampled when AND gate 1 turns on, it charges capacitor 24 and then the AND output goes low, the sampling transistor turns off and the charge is held on capacitor 24.

Q Where does that charge in capacitor 24 come from during the sampling process?

A Comes from the signal input line -- or data signal line 73.

Q And what is element 75?

A 75 is -- I believe they call it again a buffer.

Q Why would there need be a buffer 75 on the signal line 73?

MR. BERKOWITZ: Objection to form.

A We don't know the output impedence that's driving the input of the buffer nor how far away that is. So it's not unusual to have a buffer circuit in that position.

Q So a designer might include a buffer circuit based on output impedence. Is that right?

MR. BERKOWITZ: Objection to form.

A They would typically model what the source is in both frequency and impedence and voltage and then look at what the load is on the 73 and 74 line and make a determination as to whether to put that in or not.

Q And here they decided to include them on each line?

A They did.

Q Are source lines usually high impedence or low impedence?

MR. BERKOWITZ: Objection to form.

A It's all relative.

Q Relative to source line 5 -- let's talk about the output of AND gate 72. Again, we'll look at just the first column here.

How would you compare the impedence of that output line running from AND gate to the gate of the transistor compared to source line 5?

MR. BERKOWITZ: Objection to form.

A The impedence of the output of AND 1 to a source line, was that your question?

Q No, to the gate of the transistor.

A Depends on how big they sized the transistor which will have input capacitance and a number of parasitic capacitances. Difficult to say what that impedence looks like. It would need to be modeled with SPICE and have an accurate voltage versus capacitance of the gate terminal.

Q You agree that AND gate does not drive an analog voltage on signal line 5, correct?

MR. BERKOWITZ: Objection to form.

A The AND gate 72 causes the analog signal on line 73 to charge up capacitor 24, and then the analog voltage is held on 24 as AND gate 1 goes low and turns off the transfer switch 19.

Q So when transistor 19 turns off, the analog voltage to be provided to source line 5 comes from capacitor 24.

Is that right?

MR. BERKOWITZ: Objection to form.

A That voltage is what will be used to -- will be present on lines 5.

Q And that will be used to drive line 5?

A Yes.

Q And the capacitor 25 will be used to drive line 5 of the second signal line in the first column.

Is that right?

A That's correct.

MR. BERKOWITZ: We've been going more than an hour and a half, so is this a good time for a break?

MR. HELGE: Off the record at 3:10.

(A recess was taken.)

MR. HELGE: Back on the record at 3:25.

BY MR. HELGE:

Q Mr. Marentic, I'm going to read a sentence to you. I'm just curious if you agree with this or not.

"The purpose of the data driver is to convert serial input into parallel output signals and provide the appropriate output signals or analog voltages on to the data lines."

Is that correct?

MR. BERKOWITZ: Objection to form, outside the scope.

A Could you point me to the reference or read

it again?

Q Sure. "The purpose of the data driver is to convert serial input into parallel output signals and provide the appropriate output signals or analog voltages on to the data lines."

MR. BERKOWITZ: Same objections.

A I think I understand that.

Q Do you agree with that sentence?

A I believe that's a sentence from the Sharp reference and without more context, I would say I believe that is the sample and hold technique that they disclose, but I'd like to look at it closer.

Do you have the reference and line number?

Q Well, I don't from the Sharp reference, but I'm trying to understand just generally if that is the purpose of a data driver.

So do you think the answer depends upon the context, whether that's accurate or not?

MR. BERKOWITZ: Objection to form.

A It could be true in certain cases, and there might be cases where it's not true.

Q Figure 10 of the Sharp reference does not

show any digital to analog converters. Is that correct?

MR. BERKOWITZ: Objection to form.

A Figure 10 of the Sharp reference does not have digital to analog converters.

Q And why is that?

MR. BERKOWITZ: Objection to form.

A Their driver circuit that they describe in a good amount of detail is a sample and hold driver scheme.

Q And that means it doesn't require a digital to analog converter?

MR. BERKOWITZ: Objection to the form.

A That may be on the left-hand side of the schematic.

Q So it's outside the picture?

A Outside of the picture. I don't know what method they used to drive signal buffers 76, maybe 75 and 76. That's somewhere upstream, not relative to the '550 and the Sharp reference because it's really about wiring of TFTs to gate, to source drivers.

Q You would agree that the signals on lines

73 and 74 are analog though, right?

MR. BERKOWITZ: Objection to form.

A The signals on 73 and 74 are described as video input.

Q Could they be digital signals?

MR. BERKOWITZ: Objection to form.

A They would not be digital signals for displaying moving TV imagery.

Q Could they be any sort of digital signals on lines 73 and 74?

MR. BERKOWITZ: Objection to form.

A They could be a stepped signal that goes in 256 steps between the voltage to ensure the LCD is off and the voltage to ensure the LCD is on, or they may be analog with an infinite number of intermediate values.

Q So the stepped signal you just described, is that an analog signal or a digital signal?

A I'd call it an analog signal with certain characteristics.

Q Looking at Figure 10, do you believe that there must be a digital to analog converter for each

signal line 5?

MR. BERKOWITZ: Objection to form, outside of scope.

A I'm not sure what is to the left of Figure 10. That's not described. In fact, I think the Sharp reference even says not shown here.

Q And you aren't relying on anything that's not described in Figure 10, are you?

MR. BERKOWITZ: Objection to form.

Q Let's turn this into a positive statement instead of a negative statement.

You're only relying on what's actually shown and described in this reference, correct?

MR. BERKOWITZ: Objection to form.

A That's correct.

Q And so --

A And described in the text, translated text of the Sharp reference.

Q Understood, understood.

We talked last time you were here about the theory of inherency and you're not relying on any sort of theory of inherency based on the Sharp

reference, are you?

MR. BERKOWITZ: Objection to form.

A I don't believe so. The inherency is an anticipation situation and this is an obvious argument.

Q When you were providing your analysis in your declaration, did you consider the burden of proof in reaching any of your opinions?

MR. BERKOWITZ: Objection to form.

A I didn't have to.

Q Why is that?

A Because it was clear-cut. There was no need to have a imaginary scale and make sure that I had 51 percent on one side and 49 on the other. It was clear-cut, straightforward.

Q Can you turn to Paragraph 64 of your declaration. Do you see that paragraph, Mr. Marentic?

A 64, yes.

Q Do you see that what you said here, "Most of the terms of Claims 1 to 5 of the '550 patent are clear to me except for the following terms"? Did I

read that correctly?

A Yes.

Q And after that you then provide some opinions on a couple of different terms, right?

A Yes.

Q Are you performing claim construction there?

MR. BERKOWITZ: Objection to form.

A I'm providing an opinion to clarify those terms.

Q And that opinion is what those terms mean to you. Is that right?

A Yes. And what they would mean to someone having an ordinary skill in the art in 2004.

Q And the standard of a person having ordinary skill in the art in 2004 is described in your Paragraph 74, correct?

A Yes.

Q And in that first sentence of Paragraph 74 you talk about a person of ordinary skill in the art having an undergraduate degree in electrical engineering or equivalent work experience, correct?

A Correct.

Q So someone with a different degree may still have work experience that then satisfies the requirement of this standard, correct?

A That's correct, or it could be someone that was in the Navy and went through a series of Navy technical training schools that would have not a conferred bachelor degree but would have enough experience to be an electrical engineer.

Q Would that equivalent work experience need to cover all facets of electrical engineering training or could it be focused on LCD technology?

MR. BERKOWITZ: Objection to form.

A It's probably varied work experience, but some of it in gaining the equivalent of an electrical engineering degree would need to be in that field, in addition to later the experience of two to five years.

So, for instance, a person would need to be able to generate a schematic, plug in values, maybe with help have parasitic values and then run SPICE simulations.

Q That's an example of equivalent work experience?

A That would be some of the -- an example of the specialized training that perhaps is not peculiar to just LCD training but to general equivalent work experience.

Q Equivalent to electrical engineering?

A To an equivalent EE degree, yes.

Q If you look at Paragraph 79, top of Paragraph 79 -- I'm sorry, top of Page 28, do you see that?

A Yes.

Q You say, "As of the filing date of the '550 patent workers in the field of LCD devices were aware of several developments."

What do you mean by workers?

A Person having ordinary skill in the art at the time of 2004, not the people that mount driver chips to the edge of an LCD.

Q Could you please turn one more page -- you're already there actually, Page 29. In this Figure 10 the drivers that you're identifying are

defined by dotted lines and shaded areas.

Is that correct?

A Correct, my copy is black and white, but the original is colored, orange and purple, red and green.

Q And those are the boundaries of the drivers that you're identifying, correct?

A Correct.

MR. HELGE: No other questions.

MR. BERKOWITZ: So let's take five minutes and see if we have anything else.

MR. HELGE: So we'll be off record, 3:41.

(A recess was taken.)

MR. HELGE: Go back on the record at 3:47.

MR. BERKOWITZ: I have no questions for the witness.

COURT REPORTER: Do you want a copy of the transcript?

MR. BERKOWITZ: Yeah, there's no rush on it, no emergency at all.

MR. HELGE: Actually, there kind of is.

MR. BERKOWITZ: We might need it, though.

MR. HELGE: We'd like it by -- we'll take a final by Friday. Are you reserving the right to have Mr. Marentic review and sign?

MR. BERKOWITZ: Yes, of course.

MR. HELGE: We are off the record at 3:48.

(Time noted: 3:48 p.m.)

_____

MICHAEL J. MARENTIC

Subscribed and sworn to
before me this ____ day
of _____, 2015.

_____

Notary Public

CERTIFICATE OF SHORTHAND REPORTER – NOTARY PUBLIC

I, Nancy Mahoney, Certified Court Reporter and Registered Professional Reporter and Notary Public within and for the State of New York do hereby certify:

That Michael J. Marentic, the witness whose deposition is hereinbefore set forth, was duly sworn by me before the commencement of such deposition and that such deposition was taken before me and is a true record of the testimony given by such witness.

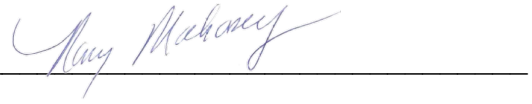
I further certify that the adverse party, Sharp Corporation, was represented by counsel at the deposition.

I further certify that the deposition of Michael J. Marentic, occurred at the offices of Amster Rothstein & Ebenstein, on Wednesday, November 11, 2015, commencing at 10:30 a.m. to 3:48 p.m.

I further certify that I am not related to any of the parties to this action by blood or marriage, I am not employed by or an attorney to any of the parties to this action, and that I am in no way interested, financially or otherwise, in the outcome of this matter.

IN WITNESS WHEREOF, I have hereunto set my hand this 12th day of November 2015.

My commission expires:
June 10, 2018



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CERTIFICATION

This is to certify that the attached translation is, to the best of my knowledge and belief, a true and accurate translation from Japanese into English of the attached Unexamined Patent Application No. H08-305322.

Mirna Turina, Project Manager
Geotext Translations, Inc.

Sworn to and subscribed before me
this 2nd day of March, 2015.

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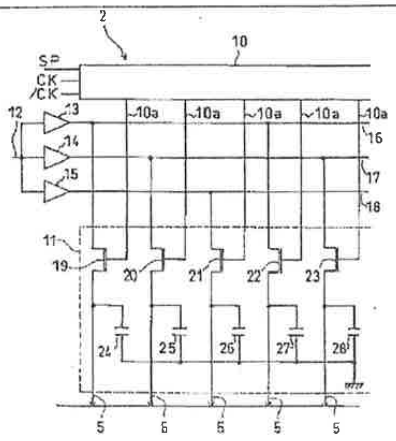
(54) [Title of the Invention] Display Device

(57) [Abstract]
[Constitution] After the same data signals from a data signal line 12 are supplied to three data signal lines 16 to 18 via buffer circuits 13 to 15, they are supplied to sampling switches 19 to 23 of a sampling hold circuit 11. The data signals sampled by the sampling hold circuit 11 are supplied to source bus lines 5....
[Effect] Because it is possible to correctly sample data signals with little corruption or noise, high-resolution display with limited decrease in the horizontal resolution and decrease in the display quality becomes possible.



[Claims]

[Claim 1] A display device provided with a plurality of data signal lines by which data signals are respectively supplied,

a plurality of sampling circuits by which the data signals supplied from the plurality of data signal lines are respectively sampled,

a plurality of data bus lines respectively connected to the plurality of sampling circuits,

a plurality of pixel units that are both connected to the plurality of data bus lines and arranged in matrix form, and

a drive circuit including the sampling circuits and that drives the data bus lines, wherein

at least two of the plurality of data signal lines have the same data signals supplied and are connected to different sampling circuits via respectively different buffer circuits.

[Claim 2] The display device according to claim 1, wherein of the plurality of sampling circuits, the sampling circuits for which the timing of the sampling is synchronized are both connected to respectively different data signal lines and have no time overlap of the ON time of the respective sampling circuits.

[Claim 3] The display device according to claim 1 or 2, wherein the buffer circuits are formed on the same substrate as the sampling circuits.

[Claim 4] A display device provided with a plurality of data signal lines by which data signals are respectively supplied,

a plurality of sampling circuits by which the data signals supplied from the plurality of data signal lines are respectively sampled,

a plurality of data bus lines respectively connected to the plurality of sampling circuits,

a plurality of pixel units that are both connected to the plurality of data bus lines and arranged in matrix form, and

a drive circuit that includes the sampling circuits and that drives the data bus lines, wherein

the data signal line is divided into a plurality in the horizontal direction of the display, and each divided signal line is connected to sampling circuits via respectively different buffer circuits.

[Claim 5] A display device provided with a plurality of data signal lines by which data signals are respectively supplied,

a plurality of sampling circuits by which the data signals supplied from the plurality of data signal lines are respectively sampled,

a plurality of data bus lines respectively connected to the plurality of sampling circuits,

a plurality of pixel units that are both connected to the plurality of data bus lines and arranged in matrix form, and

a drive circuit that includes the sampling circuits and that drives the data bus lines, wherein

of the plurality of pixel units, respectively different data bus lines are connected to the plurality of pixel units adjacent in the column direction, and the same sampling circuits are connected via the buffer circuits to these data bus lines.

[Claim 6] The display device according to claim 1, 2, 3, 4 or 5, wherein the drive circuit and the image display unit comprising the plurality of pixel units are formed monolithically on the same substrate.

[Detailed Description of the Invention]

[0001] [Field of Industrial Use] The present invention relates to a display device such as a liquid crystal display device or the like.

[0002] [Prior Art] Conventionally, display devices, for example, as shown in FIG. 12, liquid crystal display devices (hereafter called LCD) have been constituted by a display unit 101 having a plurality of pixel units 104..., and a source driver 102 and a gate driver 103 as a drive circuit for driving each pixel unit 104.

[0003] Each of the pixel units 104... is respectively arranged at a place at which a plurality of source bus lines 105... connected to the source driver 102 and a plurality of gate bus lines 106... connected to the gate driver 103 intersect orthogonally. Thus, the arrangement of the pixel units 104... is in a matrix form in the display unit 101.

[0004] Also, a pixel unit 104 is constituted by a pixel transistor 107 formed from TFT (thin film transistors), pixel capacity 108 and additional capacity 109; the gate terminals of pixel transistor 107 are connected to gate bus line 106, source terminals are connected to source bus line 105, and drain terminals are connected to pixel capacity 108 and additional capacity 109.

[0005] Source driver 102 is constituted by shift register 110, and sampling switches 111 formed from transistors, sampling capacitors 112, data signal lines 113 and the like; sampling hold circuit 114 is formed from the above sampling switches 111, sampling capacitors 112, data signal lines 113, and source bus lines 105.

[0006] Start pulses (SP) and drive clocks (CK, /CK) input to the shift register 110, and the input SP are sequentially shifted according to the CK and /CK and output to sampling hold circuit 114.

[0007] Gate driver 103 has a shift register 115 and sequentially outputs scan signals to each gate bus lines 106....

[0008] Furthermore, when the above display unit 101, source driver 102, and gate driver 103 are formed monolithically on the same substrate, there are cases when only display unit 101 is formed on the insulated substrate.

[0009] Here we will describe the operation of the displace device with the constitution noted above. First, the SP input to the shift register 110 of the source driver 102

is sequentially shifted by CK and /CK and output to sampling hold circuit 114, and become the sampling pulses for sampling hold circuit 114. Then, sampling switch 111 goes to an ON state by means of the input sampling pulse, and the data signal of data signal line 113 at the point in time that this sampling pulse is input is sampled.

[0010] Then, the data signal sampled by the sampling pulse is held in sampling capacitor 112 and output to source bus line 105 as a source bus line signal.

[0011] Meanwhile, the output of each digit of shift register 115 of gate driver 103 is output as scan signals (gate bus line signals) sequentially to gate bus lines 106...; pixel transistors 107 connected to selected gate bus lines 106 turn ON, and the source bus line signals at that point in time are sequentially written as image data to pixel capacity 108 and additional capacity 109.

[0012] Then, by driving the liquid crystal corresponding to each pixel unit 104, the desired display is achieved.

[0013] Therefore, with the LCD of the constitution noted above, as described above, source driver 102 uses the panel sample hold method by which image data is held on the display unit 101 side. With an LCD having this kind of source driver 102, when the number of pixel units 104 in the horizontal scan direction becomes high, the image data write time is different for pixel unit 104 connected to the least significant digit of the shift register 110 and the pixel unit 104 connected to the most significant digit. Because of this, it is possible to make the image data write time longer with the pixel units 104 connected to the upper digits of the shift register 110, but there is the problem that it is not possible to have sufficient image data write time with the pixel units 104 connected to the lower digits.

[0014] In light of that, to solve the problems noted above, we propose an LCD that uses a driver sample hold method source driver by which image data is held on the source driver side.

[0015] In the following, we will describe an LCD that uses the source driver of the driver sample hold method noted above. Furthermore, this LCD, with the exception of the source driver, has the same display unit 101 and gate driver 103 as that of the LCD shown in FIG. 12; therefore, in this description, we will describe only the source driver of the driver sample hold method.

[0016] The source driver of the driver sample hold method noted above has a constitution in which the output side of sampling hold circuit 114 of source driver 102 shown in FIG. 12 is connected to a transfer circuit 120 formed from transfer switch 116, hold capacitor 117, buffer circuit 118, and transfer signal line 119.

[0017] In other words, at the time point that data of one scan line has been sampled by sampling hold circuit 114, a transfer signal is output from transfer signal line 119 by transfer circuit 120, transfer switch 116 goes to an ON state, and after the data held in sampling capacitor 112 of sampling hold circuit 114 has been simultaneously transferred to hold capacitor 117, sampling of the next scan period is performed.

[0018] In other words, during the period that data of the next one scan line is being sampled, the sampling data of the previous scan line held in hold capacitor 117 is continuously applied as source bus line signals to source bus lines 105 (FIG. 12) via the buffer circuit 118.

[0019] In this way, by using the source driver of the driver sample hold method, even when there is a large number of pixel units 104 in the horizontal scan direction, it is possible to obtain sufficient write time for the image data to the respective pixel units 104.... By doing this, it is possible to make the image data write time almost the same for the pixel unit 104 connected to the least significant digit of the shift register 110 and the pixel unit 104 connected to the most significant digit.

[0020] Furthermore, when the LCD is formed monolithically by a driver on the insulated substrate, the speed at which the shift register formed using p-SiTFT operates stably is about several MHz, and with the shift register inside the source driver of the LCD with a large number of pixels in the horizontal direction which requires high speed operation, a problem occurs of having the shift register operating speed be insufficient.

[0021] In light of that, to reduce the operating speed of the shift register, for example, as shown in FIG. 14, we propose a source driver for which a plurality of systems, in this case four systems of shift registers 131 to 134, are provided, and by having the respective shift registers 131 to 134 operate at CK1 to CK4, /CK1 to /CK4 of different phases, each level of shift register 131 to 134 is operated at low speed with the overall shift speed remaining as is.

[0022] With the source driver having the four systems of shift registers 131 to 134 noted above, as shown in FIG. 15, the start pulses SP are sequentially shifted by CK1 to CK4 and /CK1 to /CK4 and sampling pulses SMP1 to SMP8 are output. Furthermore, the width of SMP1 to SMP8, which are the output of the four systems of shift registers 131 to 134, is four times that of when the shift register has one system, but the phase skew of SMP1 to SMP8 is the same as when the shift register has one system.

[0023]

[Problems the Invention Attempts to Solve] However, with the source driver having the four systems of shift registers 131 to 134 noted above, as shown in FIG. 15, each sampling pulse

SMP1 to SMP8 is in a mutually overlapping form. Because of this, when seen at a given moment, there are always eight sampling transistors 111... ON. In other words, the capacitance of eight sampling capacitors 112... has become the load via sampling transistors 111 for data signal line 113 or for the data signal output circuit. Furthermore, there is wiring resistance on data signal lines 113 and ON resistance on sampling transistors 111, and therefore the response of the data signals with each sampling capacitor 112 deteriorates with operation of a time constant of the RC integrating circuit, and the waveform becomes corrupted compared with the original data signal.

[0024] With sampling of data signals done based on this kind of corrupted waveform, the band information that the data signal originally had is lost, so the display has low horizontal resolution. Furthermore, for the scan signals as well (not illustrated), depending on the constitution, two adjacent outputs of the gate shift register are overlapping, and for the pixel part as well, the same kind of problem occurs as with the sampling unit of the source driver noted above.

[0025] To prevent this kind of problem, we propose a display device for which a video signal line is arranged for each shift register 131 to 134. In this case, for example, the Nth (SMP1) fall of the sampling pulse shown in FIG. 15 and the N $+8^{th}$ (SMP9) rise have the same timing, but in actuality, due to signal waveform corruption or delay, a phenomenon occurs of the N $+8^{th}$ sampling transistor simultaneously turning ON before the Nth sampling transistor 111 goes completely OFF.

[0026] When this kind of phenomenon occurs, as described above, even if the video signal line is divided into a plurality of parts, the sampling data of the Nth sampling hold circuit 114 of the source driver is affected not only by the N +4 sampling signal, but also by the N $+8^{th}$ sampling data, and an adverse effect is given to the display as a ghost phenomenon or noise.

[0027] Furthermore, the phenomenon described above can also occur in the same manner with the display unit. Because of this, for example, the present applicant, in Patent Application No. H05-300537, proposed a display device for which the same video signal line is branched into a plurality of parts external to the drive circuit. In this way, by branching the same video signal line into a plurality of parts external to the drive circuit, having a plurality of sampling circuits connected to one video signal line turning on simultaneously is eliminated, and as a result, corruption of the signal in each video signal line is reduced, and the resolution of the display device is improved.

[0028] However, even when the same video signal line is simply divided into a plurality of parts, when divided into a plurality of parts on the same substrate as the panel, by means of contact resistance with a flexible substrate or the like, wiring resistance, and also output impedance of the video signal supply source, it is possible to increase the time constant, but it is not possible to totally inhibit the occurrence of ghosts. Also, even when the same video signal line is simply divided into a plurality outside the panel, by means of the aforementioned contact resistance with a flexible substrate or the like, wiring resistance, and also output impedance of the video signal supply source, it is possible to increase the time constant, but it is not possible to totally inhibit the occurrence of ghosts.

[0029] Also, when we look at sampling circuits connected to the same data signal lines constituting the source driver, there is OFF resistance in the sampling transistor; however, when it is not possible to make the OFF resistance of the sampling transistor sufficiently large, the problem occurs of the sampling data written to the sampling capacitor going through the OFF resistance of the transistors and the data signal lines and having crosstalk with each other.

[0030] The present invention was created in light of the problem points noted above, and its objective is to provide a display device that reduces data signal corruption or data signal noise due to adjacent transistors being ON simultaneously and that reduces crosstalk due to insufficient or decreased transistor OFF characteristics, thus preventing a ghost phenomenon and also being able to realize high resolution display for which a decrease in horizontal resolution and a decrease in display quality due to crosstalk are inhibited.

[0031]

[Means for Solving the Problems] The display device of claim 1 is equipped with a plurality of data signal lines by which data signals are respectively supplied, a plurality of sampling circuits by which the data signals supplied from the plurality of data signal lines are respectively sampled, a plurality of data bus lines respectively connected to the plurality of sampling circuits, a plurality of pixel units connected to the plurality of data bus lines and arranged in matrix form, and a drive circuit including the sampling circuits for driving the data bus lines, wherein at least two of the plurality of data signal lines have the same data signals supplied, and are connected to different sampling circuits via respectively different buffer circuits.

[0032] The display device of claim 2 is the display device according to claim 1, wherein of the plurality of sampling circuits, the sampling circuits for which the timing of the sampling is synchronized are connected to respectively different data signal lines, and there is no time overlap of the ON time of the respective sampling circuits.

[0033] The display device of claim 3 is the display device according to claim 1 or 2, wherein the buffer circuits are formed on the same substrate as the sampling circuits.

[0034] The display device of claim 4 is equipped with a plurality of data signal lines by which data signals are respectively supplied, a plurality of sampling circuits by which the data signals supplied from the plurality of data

signal lines are respectively sampled, a plurality of data bus lines respectively connected to the plurality of sampling circuits, a plurality of pixel units connected to the plurality of data bus lines and arranged in matrix form, and a drive circuit including the sampling circuits for driving the data bus lines, wherein the data signal line is divided into a plurality in the horizontal direction of the display, and each divided signal line is connected to sampling circuits via respectively different buffer circuits.

[0035] The display device of claim 5 is equipped with a plurality of data signal lines by which data signals are respectively supplied, a plurality of sampling circuits by which the data signals supplied from the plurality of data signal lines are respectively sampled, a plurality of data bus lines respectively connected to the plurality of sampling circuits, a plurality of pixel units connected to the plurality of data bus lines and arranged in matrix form, and a drive circuit including the sampling circuits for driving the data bus lines, wherein of the plurality of pixel units, respectively different data bus lines are connected to the plurality of pixel units adjacent in the column direction, and the same sampling circuits are connected via the buffer circuits to these data bus lines.

[0036] The display device of claim 6 is the display device according to claim 1, 2, 3, 4 or 5, wherein the drive circuit and the image display unit consisting of a plurality of pixel units are formed monolithically on the same substrate.

[0037]

[Operation] With the constitution of claim 1, by means of at least two of the plurality of data signal lines having the same data signals supplied, and being connected to different sampling circuits via respectively different buffer circuits, it is possible to have sparse electrical connections of adjacent sampling circuits by which the same data signals are supplied.

[0038] By doing this, even when adjacent sampling circuits for which the same data signals are supplied are in an ON state simultaneously, the other adjacent sampling circuits to which the same data signals are supplied are not affected by noise that occurs at this time. In other words, incorrect data signals due to the noise noted above are not sampled.

[0039] Also, since adjacent sampling circuits are not connected to the same data signal line, it is possible to reduce the load of one data signal line, so it is possible to reduce data signal corruption.

[0040] Therefore, with adjacent sampling circuits, there is no erroneous sampling due to data signal corruption, and there is no effect when mutually turning ON and OFF, so correct data signals are always sampled. Because it is possible to supply the sampled data signals to the data bus line, it is possible to reduce the crosstalk due to ON and OFF characteristic defects of sampling signals with the pixel units. Thus, it is possible to have a high-resolution display in which a decrease in display quality due to crosstalk is inhibited.

[0041] With the constitution of claim 2, sampling circuits for which the sampling timing is synchronized are connected to respectively different data signal lines, and by means of the ON period of the respective sampling circuits not overlapping, it is possible to reduce the noise due to other adjacent sampling circuits going to an ON state at the moment that another single sampling circuit goes to an OFF state.

[0042] With the constitution of claim 3, by means of the buffer circuits connected to the sampling circuits being formed on the same substrate as the sampling circuits, it is possible to suppress degradation of data signals caused by such things as wiring resistance and contact resistance of the flexible substrate or the like that connects the buffer circuits and the sampling circuits. It is also possible to suppress an increase in connection terminals for connecting the buffer circuits and the sampling circuits and possible to improve reliability with mounting.

[0043] With the constitution of claim 4, the data signal lines are divided into a plurality in the display horizontal direction and each divided signal line is connected to sampling circuits via respectively different buffering circuits, so it is possible to reduce the load on the data signal line. By doing this, it is possible to reduce the resistance and capacitance of the data signal lines, so degradation of the data signals on the data signal line is further reduced, and it is possible to reduce noise during sampling.

[0044] With the constitution of claim 5, of the plurality of pixel units, respectively different data bus lines are connected to the plurality of pixel units adjacent in the column direction, and by the same sampling circuits being connected via the buffer circuits to these data bus lines, it is possible to inhibit interference of pixel units adjacent in the column direction. By doing this, it is possible to reduce crosstalk between pixel units with each other, and possible to improve display quality.

[0045] With the constitution of claim 6, by means of an image display unit constituted from a plurality of pixel units being formed monolithically on the same substrate as the image display unit, it is possible to increase the pixel transistor drive force accompanying an increase in screen size, to reduce mounting costs of the drive IC, and the like.

[0046]

[Embodiments]

[Embodiment 1] Following is a description of an embodiment of the present invention based on FIG. 1 through FIG. 3. In this embodiment, we will describe a liquid crystal display device (hereafter called LCD) as the display device, and the same is also true for the other embodiments described later.

[0047] As shown in FIG. 2, the LCD of this embodiment is constituted from a display unit 1 having a plurality of pixel units 4 arranged in a matrix form, and a source driver 2 and a gate driver 3 as the drive circuit for driving each pixel unit 4.

[0048] On display unit 1, the following are arranged: a

plurality of source lines 5... connected to the source driver 2, and a plurality of gate bus lines 6... connected to the gate driver 3, arranged so as to intersect orthogonally, and pixel units 4 arranged at the intersecting parts of the source bus lines 5 and the gate bus lines 6. In other words, display unit 1 drives pixel units 4 by data signals such as video signals or the like from source driver 2 and scan signals from gate driver 3, and the desired image is displayed by changing the liquid crystal orientation state of a liquid crystal layer (not illustrated).

[0049] The aforementioned pixel units 4 are constituted by a pixel transistor 7 consisting of a TFT (Thin film transistor), a pixel capacity 8, and an additional capacity 9; the gate terminals of the pixel transistors 7 are connected to gate bus lines 6, the source terminals to source bus lines 5, and the drain terminals to pixel capacity 8 and additional capacity 9. In other words, when pixel transistors 7 are turned ON by the scan signal, the source bus line signals (video signals) from source bus line 5 are written to pixel capacity 8 and additional capacity 9.

[0050] The following are provided on source driver 2: a source shift register 10, and a sampling hold circuit 11 for sampling data signals from a data signal line 12 by sampling pulses from source shift register 10. The aforementioned data signal line 12 is branched into three within source driver 2 and connects to three data signal lines 16 to 18 via buffer circuits 13 to 15. Furthermore, in this embodiment, the aforementioned buffer circuits 13 to 15 are provided inside source driver 2, but the invention is not limited to this, and these can also be provided externally. In other words, instead of being branched on the inside of source driver 2, data signal line 12 can also be branched outside source driver 2.

[0051] Start pulses (SP) and drive clocks (CK, /CK) are input to the aforementioned source shift register 10, and the input SP are sequentially shifted according to the CK and /CK and output as sampling pulses to sampling hold circuit 11.

[0052] As shown in FIG. 1, data signals from data signal line 12 are supplied to sampling hold circuit 11 from three data signal lines 16 to 18 connected via buffer circuits 13 to 15, and the aforementioned data signals are sampled according to sampling pulses from the aforementioned source shift register 10. In other words, the same data signal is branched into three, and the respective signals are sampled individually.

[0053] The aforementioned sampling hold circuit 11 has sampling switches 19 to 23 formed from TFT for sequentially sampling data signals according to sampling pulses of source shift register 10, and hold capacitors 24 to 28 for holding the sampled data. One sampling circuit is constituted from one sampling switch and one sampling capacitor connected to that.

[0054] Output lines 10a... from the aforementioned source shift register 10 are respectively connected to the gate terminals of the aforementioned sampling switches 19 to 23, and data signal lines 16 to 18 branched from one data signal line 12 are respectively connected to the source terminal. In other words, data signal line 16 is connected to the source terminal of sampling switch 19, data signal line 17 is connected to the source terminal of sampling switch 20, data signal line 18 is connected to the source terminal of sampling switch 21, and data signal line 16 is again connected to the source terminal of sampling switch 19, and following, data signal lines 16 to 18 are repeatedly connected in sequence.

[0055] As described above, sampling switches 19 to 23 are connected so that sampling switches connected to the same data signal line, for example the sampling switch 19 and the sampling switch 22 connected to the data signal line 16, do not go to an ON state simultaneously. In other words, there are sparse mutual electrical connections of sampling switches 19 to 23.

[0056] Here, we will explain the operation of the LCD of the constitution noted above while referring to the operation timing chart of FIG. 3.

[0057] First, for one scan period, the SP input to source shift register 10 of source driver 2 are sequentially shifted by CK, /CK and output to sampling hold circuit 11, and these become the sampling pulses of sampling hold circuit 11. Then, each sampling switch 19 to 23 is set to an ON state by the input sampling pulses, and the data signals of data signal lines 16 to 18 are sampled at the point in time that these sampling pulses are input.

[0058] Then, each data signal sampled by the sampling pulses is output to the source bus lines 5 as the source bus line signals held by the hold capacitors 24 to 28.

[0059] Meanwhile, the output of each row in gate driver 3 is output sequentially to gate bus lines 6 as scan signals (gate bus line signals), pixel transistor 7 connected to selected gate bus lines 6... is turned on, and at that point in time, the source bus line signals from the aforementioned source bus line 5 of one scan period are sequentially written as image data to pixel capacity 8 and additional capacity 9.

[0060] Then, the desired display is created by driving liquid crystal corresponding to each pixel unit 4.

[0061] In the next scan period, source bus line signals for which the voltage polarity is inverted are written as image data to pixel capacity 8 and additional capacity 9. In this way, each time the scan period switches, the voltage polarity of the source bus line signal is reversed and this is written as image data to pixel capacity 8 and additional capacity 9, and each time, the desired display is created by driving the liquid crystal corresponding to each pixel unit 4.

[0062] Therefore, as shown in FIG. 3, with the aforementioned source driver 2, when the SP are input, the phase is skewed by ½ only by the input timing of CK and /CK, and sampling pulses SMP1 to SMP5 are output. By doing this, each sampling pulse SMP1 to SMP5 has a time overlap, so two adjacent sampling switches are always in an ON state.

[0063] However, in this embodiment, the aforementioned sampling switches 19 to 23 have sparse mutual electric connections. In other words, two adjacent sampling switches are not connected to the same data signal line, so the load of one data signal line can be reduced from two sampling capacitors to one. As a result, it is possible to reduce data signal corruption caused by data signal line load.

[0064] Furthermore, each sampling pulse is skewed by a half phase each, so, as shown in FIG. 3, the sampling pulse SMP1 fall and the sampling pulse SMP3 rise have a time overlap. In actuality, there is an occurrence of time for which the sampling transistor 18 and the sampling transistor 21 are in an ON state simultaneously due to sampling pulse corruption or delay.

[0065] In such a case, if sampling transistor 19 and sampling transistor 21 are connected to the same data signal line, when the sampling transistor 19 goes OFF, there are cases when there is an effect of noise that occurs when sampling transistor 21 turns ON, so incorrect data signals are sampled.

[0066] However, with this embodiment, as shown in FIG. 1, sampling transistor 19 and sampling transistor 21 are connected to respectively different data signal lines, so it is possible to sample correct data signals without having an effect of noise due to the aforementioned kind of sampling pulse corruption or delay.

[0067] In this way, without being affected by mutual ON and OFF times between adjacent sampling transistors, it is possible to always supply correct data signals as source bus line signals to source bus line 5, so it is possible to reduce the ghost phenomenon.

[0068] Thus, the LCD of this embodiment is capable of doing high-resolution display for which a decrease in display quality due to the ghost phenomenon caused by data signal corruption or noise is inhibited.

[0069] With this embodiment, so as to have the electrical connections be as sparse as possible for sampling switches 19 to 23, after data signal line 12 is branched into three, data signals are supplied to sampling switches 19 to 23 from data signal lines 16 to 18 via buffer circuits 13 to 15.

[0070] However, the invention is not limited to the aforementioned going via buffer circuits 13 to 15, and it is also possible, for example, to not provide buffer circuits 13 to 15, and after branching the data signal line 12 into three, to supply data signals directly to sampling switches 19 to 23. In this case, compared to when going via buffer circuits 13 to 15, it is more difficult to have electrical sparseness for sampling switches 19 to 23, so the effect is reduced by half.

[0071] Also, with this embodiment, the sampling method in source driver 2 is the panel sample hold method by which image data as data signals are held on the display unit 1 side, but this can be similarly applied also with a source driver of the driver sample hold method by which image data is held on the source driver side, and the same effect can be obtained. In this case, by using the source driver of the driver sample hold method, it is possible to have sufficient image data write time with pixel units connected to the source driver.

[0072] [Embodiment 2] Following is an explanation of another embodiment of the present invention based on FIG. 4. For convenience of the explanation, the same code numbers are given to members having the same function as those of embodiment 1, and their description will be omitted. The same is true for each embodiment hereinafter. Also, with this embodiment, we will describe a case of applying the constitution applied to source driver 2 of embodiment 1 to display unit 1 of the LCD.

[0073] With the LCD of this embodiment, as shown in FIG. 4, source bus lines 5 connected to source driver 2 of embodiment 1 are branched into three in front of display unit 1, and these are connected respectively to source bus lines 34 to 36 via three buffer circuits 31 to 33. In FIG. 4, the lateral direction is the row direction, and the vertical direction is the column direction.

[0074] The source terminals of pixel transistors 7 arranged in the column direction are connected to the aforementioned source bus lines 34 to 36 such that pixel transistors 7 adjacent in the column direction are not connected to the same source bus line.

[0075] The operation of the LCD of this embodiment is the same as that of the LCD of embodiment 1 other than that the source bus line signals supplied to the display unit 1 are supplied branched into three.

[0076] In the constitution noted above, pixel transistors 7 adjacent in the column direction are connected to mutually independent source bus lines, so there is no mutual effect even when pixel transistors 7 are turned ON and OFF. Because of this, adjacent pixel units 4... are not affected by noise that occurs when mutually adjacent pixel transistors 7 are turned ON and OFF, so it is possible to obtain a high-resolution image without the ghost phenomenon.

[0077] It is also possible to constitute the aforementioned source driver 2 as shown in FIG. 1 of embodiment 1. In this case, it is possible to supply data signals without corruption or delay to display unit 1, and in fact in display unit 1, data signals are written without corruption or delay, so it is possible to provide an LCD with further improved display quality.

[0078] [Embodiment 3] Following is an explanation of yet another embodiment of the present invention based on FIG. 5 and FIG. 6.

[0079] The display device of this embodiment is equipped with a source driver 41 as shown in FIG. 5, instead of the source driver 2 shown in FIG. 1 of embodiment 1

[0080] As shown in FIG. 5, source driver 41 is constituted from four systems of shift registers 42 to 45, AND circuits 46 to 50 for obtaining an AND operation based on the output from these shift registers 42 to 45, and sampling hold circuit 11 for which sampling pulses are supplied from AND circuits 46 to 50.

[0081] The aforementioned AND circuits 46 to 50 are connected to inverters 46a to 50a that respectively invert the output from the shift register of one digit later, and a logical product of the output of shift registers 42 to 45 and the inverted signals of the output of one digit later is obtained; the logical product obtained is supplied as the sampling pulse to sampling hold circuit 11.

[0082] In addition to sampling pulses, data signals such as video signals and the like from data signal line 51 are supplied to sampling hold circuit 11.

[0083] The aforementioned data signal line 51, after being branched into two either inside the display unit 1 or outside source driver 41, is connected to data signal lines 54 and 55 via the buffer circuits 52 and 53. Data signal line 54 is connected to each source terminal of sampling switches 19, 21, and 23, and data signal line 54 is connected to each source terminal of sampling switches 20 and 22. By doing this, sampling switches 19 to 23 are connected alternately to data signal lines 54 and 55, and there are sparse mutual electrical connections.

[0084] Here, we will describe the operation of source driver 41 with the constitution noted above. As shown in FIG. 6, the aforementioned four systems of shift registers 42 to 45 have SP input by CK and /CK of respectively different phases. At this time, the output signals SR1 to SR9 of each shift register 42 to 45 are pulses made to have the phase shifted by 1/8 each.

[0085] The aforementioned shift register output SRi and inversion signal of the shift register output SRi+1 one digit later are input to AND circuits 46 to 50. Then, the logical products obtained with AND circuits 46 to 50 are input as sampling pulses SMP1 to 3 to sampling switches 19 to 23 of sampling hold circuit 11.

[0086] Meanwhile, the data signals supplied from data signal line 51 are respectively input via alternately connected data signal lines 54 and 55 to sampling switches 19 to 23.

[0087] Also, the data signals sampled by sampling pulses SMP1 to SMP3 are output to source bus lines 5... as source bus line signals held by the hold capacitors 24 to 28.

[0088] With the constitution noted above, as shown in FIG. 6, sampling pulses SMP1 to 3 are short pulses for which there is no mutual time overlap with AND circuits 46 to 50 for the output SRi of the shift registers 42 and 43. By doing this, two or more sampling pulses do not go in an ON state simultaneously.

[0089] In that way, of sampling switches 19 to 23, only one is always in an ON state, so the load seen from data signal lines 54 and 55 is that of one sampling capacitor. Therefore, compared to the source driver constituted by four systems of shift registers not using an AND circuit, for example the source driver shown in the prior art, it is possible to reduce the load of the data signal line to 1/8, so it is possible to reduce data signal corruption. Also, the since it is possible to reduce the load of the data signal line to 1/8, it is possible to also reduce the time constant of the output CR from the shift register to 1/8, so it is possible to make the data signal corruption smaller than conventionally.

[0090] However, for sampling pulses SMP1 to 3, in actuality, due to delay, corruption or the like of the data signal, the SMPi (i = an integer) fall and the SMPi +1 rise are not simultaneous, and a period occurs when there is a slight overlap. However, with this embodiment, adjacent sampling switches are connected to different data signal lines 54 and 55, so it is possible to not be affected by noise of the data signal lines 54 and 55 that occurs from adjacent sampling switches being in an ON state simultaneously.

[0091] Therefore, with the LCD of this embodiment, it is possible to reduce data signal corruption due to the data signal line load, and also possible to reduce the ghost phenomenon due to data signal noise due to adjacent transistors being in an ON state simultaneously.

[0092] Thus, it is possible to have high-resolution display for which the decrease in display quality due to the ghost phenomenon that occurs caused by data signal corruption and data signal noise is inhibited.

[0093] Furthermore, in this embodiment, we explained a case with four systems for the shift registers, but the invention is not limited to this, and it is sufficient to have at least two systems.

[0094] Also, with this embodiment, AND circuits were used to obtain logical products from the shift register output, but the invention is not limited to this, and for example, it is also possible to use a NOR circuit or the like, and furthermore, when using an AND of SRi and SRi + 7, it is not particularly necessary to have an inverter connected at the input level of the AND circuit.

[0095] Furthermore, with this embodiment, so as to be as electrically sparse as possible for sampling switches 19 to 23 in source driver 41, after data signal line 51 is branched into two, data signals are supplied to sampling switches 19 to 23 from data signal lines 54 and 55 via buffer circuits 52 and 53.

[0096] However, this is not limited to the aforementioned going via the buffer circuits 52 and 53, and for example, it is also possible to supply data signals directly to sampling switches 19 to 23 after branching data signal line 51 into two without providing buffer circuits 52 and 53. In such a case, it is more difficult to be electrically sparse for sampling switches 19 to 23 than in the case of going via buffer circuits 52 and 53, and therefore the effect is reduced by half.

[0097] Also, with this embodiment, the sampling method in source driver 41 is the panel sample hold method by which image data is held as data signals on the display unit 1 side; however, it is possible to similarly apply this to the source driver of the driver sample hold method by which image data is held on the source driver side, and it is possible to obtain the same effects. In such a case, by using the source driver of the driver sample hold method, it is possible to have sufficient write time for image data with the pixel units connected to the source driver.

[0098] [Embodiment 4] In the following, we will explain yet another embodiment of the present invention based on FIG. 7. In this embodiment, we will explain a case of applying the constitution applied to the source driver 41 of embodiment 3 to the signal input with display unit 1 of the LCD.

[0099] In the LCD of this embodiment, as shown in FIG. 7, source bus lines 5... connected to source driver 41 of embodiment 3 are divided into two in front of display unit 1, and the constitution is such that connection is done to the respective source bus lines 58 and 59 via two buffer circuits 56 and 57. In FIG. 7, the lateral direction is the row direction and the vertical direction is the column direction.

[0100] The source terminals of pixel transistors 7 arranged in the column direction are connected to source bus lines 58 and 59 such that pixel transistors 7 adjacent to each other in the column direction are not connected to the same source bus line.

[0101] Also, gate bus lines 6... are connected via AND circuits 60... to gate driver 3, and inverters 60a... that invert the signal output to AND circuit 60 of the respective one row later are connected to those AND circuits 60.... By means of the above-mentioned AND circuit 60, the AND operation of the output of gate driver 3 and the inverted signal of the output from gate driver 3 to AND circuit 60 of one row later is obtained, and the obtained logical product is output to gate bus lines 6 as gate signals.

[0102] The operation of the LCD in this embodiment is the same as the operation of source driver 41 of embodiment 3 except that the source bus line signal supplied to display unit 1 is branched into two, and furthermore, the gate signals supplied from gate driver 3 are output via the AND circuit.

[0103] In the constitution noted above, the gate signals that control whether the pixel transistors 7 are ON or OFF are output to gate bus line 6 via AND circuit 60, so the gate signals do not have time overlap. By doing this, the adjacent pixel units 4... are not affected by noise due to mutually adjacent pixel transistors 7 being ON or OFF, and it is possible to obtain a high-resolution image with no ghost phenomenon.

[0104] Source driver 51 can also be constituted as shown in FIG. 1 of embodiment 1. In such a case, it is possible to supply data signals with no corruption or delay to display unit 1, and with the display unit 1, because data signals are written with no corruption or delay, it is possible to provide an LCD with even better display quality.

[0105] [Embodiment 5] Following is an explanation of yet another embodiment of the present invention based on FIG. 8.

[0106] The LCD of this embodiment is equipped with a source driver 61 as shown in FIG. 8, instead of the source driver 2 shown in FIG. 1 of embodiment 1.

[0107] As shown in FIG. 8, source driver 61 is constituted equipped with source shift register 10, sampling hold circuit 11, and data signal line 12.

[0108] Buffer circuits 62 to 66 are connected to data signal line 12, and the output side of these buffer circuits 62 to 66 are connected to the respective source terminals of sampling switches 19 to 23 of sampling hold circuit 11. In other words, the data signals output from data signal line 12 are supplied to sampling switches 19 to 23 via buffer circuits 62 to 66, and are respectively held in sampling capacitors 24 to 27.

[0109] By doing this, because sampling switches 19 to 23 are connected via data signal line 12 and buffer circuits 62 to 66, here are sparse electrical connections by means of these buffer circuits 62 to 66.

[0110] Here we will explain the operation of source driver 61 with the constitution noted above. The SP input to the aforementioned source shift register 10 is sequentially shifted according to the CK and /CK input to the source shift register 10 and output. Then, the output pulses of each digit are sequentially input as sampling pulses to the gate terminals of the respective sampling switches 19 to 23 in sampling hold circuit 11.

[0111] Meanwhile, data signals from data signal line 12 are input to the source terminals of sampling switches 19 to 23 via buffer circuits 62 to 66.

[0112] Therefore, sampling switches 19 to 23 are made to go to an ON state by the sampling pulses supplied from the aforementioned source shift register 10, and the data signals output from data signal line 12 are held in the sampling capacitors 24 to 27.

[0113] However, by means of buffer circuits 13 to 15 and buffer circuits 52 and 53 arranged in source driver 2 and source driver 41 described in embodiments 1 and 3, the load is matched with the data signal line wiring load and the sampling capacitor load, so it is necessary to have the buffer circuit be a circuit of a size that can handle the aforementioned load.

[0114] However, buffer circuits 62 to 66 of this embodiment are respectively connected to one each of sampling capacitors 24 to 27 is, so the load for one of buffer circuits 62 to 66 is only one sampling capacitor. Because of that, it is possible to make the circuit smaller than for buffer circuits 13 to 15 and buffer circuits 52 and 53 described in embodiments 1 and 3.

[0115] Also, in embodiments 1 and 3, when failure occurs with one buffer circuit, data signals are not supplied for each one of three or one per two source bus lines. Because of this, the problem occurs of having a display defect for 1/3 or ½ of the overall display in display unit 1.

[0116] However, with this embodiment, when failure occurs with buffer circuits 62 to 66, data signals stop being supplied only to the source bus lines connected to the buffer circuit where failure has occurred; therefore, it is also possible to suppress display defects to be only for source bus lines connected to buffer circuits for which failure has occurred.

[0117] Furthermore, for adjacent sampling switches 19 to 23, there is sparse electrical connection by buffer circuits 62 to 66, so for example, even when the OFF resistance of sampling transistors 19 to 23 is decreased by irradiation of light from outside, it is possible to prevent crosstalk of data signals held in sampling transistors 24 to 27 via the OFF resistance of the mutually adjacent sampling switches 19 to 23 connected to the same data signal line 12.

[0118] Typically, inside the source driver, a plurality of signal wires are arranged in addition to the data signal lines, so there is a decrease in the precision of the sampling data due to noise riding via the wiring capacitance of each signal wiring, or via the capacitance of the intersecting part of wires that intersect, or other parasitic capacitance.

[0119] However, with source driver 61 of this embodiment, there is only one data signal line 12, so it is possible to reduce the effect of noise riding on data signal line 12.

[0120] In this way, with mutually adjacent sampling transistors, there is no effect when mutual turning ON and Off, and it is possible to always supply accurate data signals to source bus lines 5 as source bus line signals.

[0121] Therefore, with the LCD of this embodiment, it is possible to have a high-resolution display for which there is a reduction in the ghost phenomenon due to corruption of the data signal waveform caused by the load on data signal line 12 or to data signal noise caused by adjacent transistors being in an ON state simultaneously, and to suppress a decrease in display quality due to crosstalk that occurs due to the occurrence of insufficiency or a decrease in the OFF characteristics of the sampling transistors.

[0122] Furthermore, with this embodiment, the sampling method in source driver 61 was the panel sample hold method for which image data is held as data signals on the display unit 1 side; however, it is also possible to similarly apply this with the source driver of the driver sample hold method for which image data is held on the source driver side, and possible to obtain the same effects. In such a case, by using the source driver of the driver sample hold method, it is possible to obtain sufficient write time for the image data with the pixel units connected to the source driver.

[0123] [Embodiment 6] In the following we will explain yet another embodiment of the present invention based on FIG. 9. In this embodiment, we will explain a case in which the constitution used for source driver 61 of embodiment 5 is applied to the signal input with display unit 1 of the LCD.

[0124] As shown in FIG. 9, the LCD of this embodiment has buffer circuits 67... connected to source bus lines 5... that are connected to source driver 61; the source terminals of the pixel transistors 7 are connected to the output side of these buffer circuits 67.... In FIG. 9, the lateral direction is the row direction and the vertical direction is the column direction.

[0125] In other words, a plurality of pixel transistors 7 are connected in the column direction to the same source bus line 5, but the respective pixel transistors 7 are connected to the source bus line 5 so as to be mutually electrically sparse by means of buffer circuit 67.

[0126] Furthermore, the operation of the LCD of this embodiment is the same as the operation of source driver 41 of embodiment 5 except that the source bus line signals are supplied to pixel transistors 7 of the display unit 1 via the buffer circuits 67....

[0127] In the constitution noted above, the source bus line signals from the source bus lines 5 are respectively supplied via the buffer circuits 67... to the plurality of pixel transistors 7... connected on the same source bus line 5, so the source bus line signals

do not interfere with each other. Therefore, the adjacent pixel units 4 are not affected by noise that occurs when pixel transistors 7 are mutually in an ON state, and in fact it is possible to obtain a high-resolution image for which crosstalk due to the OFF resistance of the pixel transistors is inhibited.

[0128] It is also possible to constitute the aforementioned source driver 61 as shown in FIG. 1 of embodiment 1. In this case, it is possible to supply data signals without corruption or delay to display unit 1, and in display unit 1 as well, data signals are written without corruption or delay, so it is possible to provide an LCD with even better display quality.

[0129] [Embodiment 7] In the following we explain yet another embodiment of the present invention based on FIG. 10. For convenience of the explanation, elements having the same function as each of the previously noted embodiments are given the same code numbers, and their description is omitted.

[0130] As shown in FIG. 10, the LCD of this embodiment is constituted by a display unit 1 having a plurality of pixel units 4..., and a source driver 71 and the gate driver 3 that act as the drive circuit that drives the pixel unit 4. In FIG. 10, the lateral direction is the row direction, and the vertical direction is the column direction.

[0131] The above-mentioned source driver 71 is constituted by source shift register 10, AND circuits 72 and 72 for obtaining the logical product of the output from this source shift register 10, data signal lines 73 and 74 for supplying data signals of different polarities (video signals), and sampling hold circuit 11 for sampling data signals according to the output from source shift register 10.

[0132] Inverters 72a and 72a are connected to the above-mentioned AND circuits 72 and 72 so that the output of the next digit of the source shift register 10 is inverted and input. In other words, AND circuits 72 obtain the logical product of the output of source shift register 10 and the inverted signal of the output input to AND circuit 72 of the next digit inverted by inverter 72a, and this logical product is output to sampling hold circuit 11 as sampling pulses.

[0133] Also, data signals 73 and 74 have mutually different polarities and data signals for which the polarity has been inverted for each field are supplied via buffer circuits 75 and 76 from a data signal generating circuit (not illustrated).

[0134] The above-mentioned data signal line 73 is connected to the source terminals of sampling switches 19 and 21 of the sampling hold circuit 11, and data signal line 74 is connected to the source terminals of the sampling switches 20 and 22 of sampling hold circuit 11.

[0135] Therefore, sampling pulses from the same AND circuit 72 are supplied to the source terminals of the above-mentioned sampling switches 19 and 20, and sampling pulses from the same AND circuit 72 are supplied to the source terminals of sampling switches 21 and 22. Furthermore, AND circuits 72 supply output from source shift register 10 to sampling hold circuit 11 using a pulse width so as to have no time overlap.

[0136] In the following we will explain the operation of source driver 71 of the constitution noted above. The SP input to the source shift register 10 noted above is sequentially shifted according to the drive clocks CK and /CK input to the source shift register 10 and output. Then, the output pulse of each digit is input to AND circuit 72. Subsequently, the logical product of the output of source shift register 10 and the inverted signal of the next digit output Sri + 1 is obtained in AND circuit 72, and the value of this logical operation is output as sampling pulses to sampling hold circuit 11.

[0137] The output from the above-mentioned AND circuit 72 is sequentially input as sampling pulses to the respective gate terminals of sampling switches 19 to 23 in sampling hold circuit 11.

[0138] Meanwhile, the data signals from data signal line 12 are input to the source terminals of sampling switches 19 to 23 via buffer circuits 62 to 66.

[0139] Therefore, when the sampling pulse output from the above-mentioned source shift register 10 is input to the gate terminals of sampling switches 19 to 23, the data signal output from the data signal line 12 is held in sampling capacitors 24 to 27.

[0140] The held data signals are input to the alternately connected pixel transistors 7... for every other gate bus line 6... via the buffer circuit 77 from source bus lines 5 arranged at the left and right sides of pixel units 4....

[0141] With source driver 61 of the constitution noted above, because the output from source shift register 10 is input to the sampling hold circuit 11 via AND circuits 72..., there is a relationship between the sampling pulse width being small and there not being any mutual time overlap. Because of this, the load sent from data signal lines 73 and 74 is smaller than in the prior art, so it is possible to make the data signal corruption smaller than in the prior art.

[0142] Also, gate driver 3 is constituted by a gate shift register 3a, AND circuits 81... for obtaining the logical product from the output of this gate shift register 3a.

[0143] In the above-mentioned AND circuits 81..., inverters 81a... are connected so that the output of the next row of the gate shift register 3a is inverted and input. In other words, an AND circuit 81 obtains the logical product of the output of gate shift register 3a and the inversion signals obtained by inverting at inverter 81a the output input to AND circuit 81 of the next row, and supplies this logical product as a gate signal (scan signal) to the gate bus lines 6.... The AND circuit 81 makes the output from the gate shift register 3a have a pulse width so as not to have time overlap, and supplies this to the pixel transistors 7....

[0144] Therefore, because the gate signals input to pixel transistors 7... of display unit 1 from the gate driver 3 are the logical products obtained from the output of the gate shift register 3a, there is a relationship of the gate signals not having mutual time overlap. Because of this, it is possible to prevent the effect of noise due to pixel transistors 7... adjacent in the column direction being ON simultaneously.

[0145] Also, by means of pixel transistors 7... adjacent in the column direction being connected to different source bus lines 5..., even if there is a period for which the gate bus line signal Gi and the gate bus line signal Gi +1 of the next row are in an ON state simultaneously due to signal delay or corruption, a decrease in the precision of the source bus line signals sampled at pixel capacity 8... and additional capacity 9... caused noise that occurs when pixel transistors 7... adjacent in the column direction are ON simultaneously is prevented.

[0146] Typically, the signals applied to source bus line 5 have the polarity of the applied voltage inverted for every scan period to prevent a decrease in reliability due to DC voltage being applied to the liquid crystal. In such a case, if there is a period when pixel transistors 7... adjacent in the column direction are in an ON state simultaneously, a problem occurs of the decrease in the precision of the source bus line data sampled at the pixel capacity 8... becoming even greater.

[0147] However, with this embodiment, the pixel transistors 7... adjacent in the column direction have the source bus line signals supplied via different source bus lines 5... provided at both sides of the respective pixel units 4..., so it is possible to eliminate a period when pixel transistors 7... adjacent in the column direction are in an ON state simultaneously, and as a result, it is possible to prevent a decrease in the precision of the source bus line data sampled at the pixel capacity 8....

[0148] Also, typically, when the polarity of the voltage applied to source bus lines 5 is inverted every scan period, a source bus line 5 charged during a certain scan period has to be charged to the reverse polarity at the next scan period, and so a large drive force is required to drive the source bus lines 5.... As a result, the problem occurs of an increase in the overall power consumption of the source driver due to the power required to drive the source bus lines 5....

[0149] However, with this embodiment, data signals with different polarity set in advance are alternately supplied to source bus lines 5..., so it is sufficient to supply data signals with the same polarity to source bus lines 5... arranged at both sides of pixel units 4, so that it is not necessary to supply signals of reverse polarity to the polarity supplied to the source bus line 5... every scan period. By doing this, it is possible to reduce the power required for driving the source bus lines 5..., so it is possible to reduce the overall power consumption of the source driver 61.

[0150] With this embodiment, two source bus lines 5... are arranged at both sides of the pixel units 4..., but the invention is not limited to this, and for example, it is also possible to have two source bus lines 5 and 5 arranged at one side of the pixel units 4. However, in such a case, the form will be such that the source bus lines 5 and the pixel transistors 7 are connected with the source bus lines 5 intersecting every other gate bus line 6..., resulting in an effect of noise from the parasitic capacitance of the intersecting part and the like, and the effect of this is to be unable to exhibit the same level of effect as when the source bus lines 5 and 5 are arranged at both sides of the pixel units 4.

[0151] [Embodiment 8] In the following we will explain yet another embodiment of the present invention based on FIG. 11. The LCD of this embodiment has the same constitution for the display unit and the gate driver as for the other embodiments, so we will describe the source driver.

[0152] As shown in FIG. 11, in the source driver of the LCD of this embodiment, there are data signal lines 82... for supplying data signals of a plurality of video signals or the like, and source terminals of sampling switches 86... consisting of transistors such as TFT or the like of sampling hold circuit 85 that are connected to those data signal lines 82....

[0153] A sampling timing control circuit 84 for controlling the sampling timing of the data signals is connected to the gate terminals of the sampling switches 86.

[0154] Data signal lines 82 are connected to the data signal generating circuit (not illustrated) via the buffer circuit 83. These data signal lines 82 are connected one each to sampling switch 86. By doing this, because the load on data signal lines 82... is only one sampling switch 86, it is possible to lower the impedance of the data signal line before dividing even more than when a plurality of sampling switches 86... are connected to one data signal line 82.

[0155] In other words, by dividing data signals output from the above-mentioned data signal generating circuit into a plurality in the display horizontal direction, it is possible to lower the impedance of the data signal line before dividing, particularly the capacitance component, to about 1/N (N: number of divisions). By doing this, it is possible to significantly improve the time constant of the data signal line, so it is possible to suppress the occurrence of crosstalk.

[0156] Furthermore, because it is possible to input to display unit 1 the input of the data signals to the display unit 1 from the vicinity of the sampling hold circuit 85, it is possible to significantly improve the time constant by doing this as well.

[0157] This embodiment can be applied to each of the embodiments noted above, and by doing this, it is possible to have a display with even less occurrence of crosstalk and higher resolution.

[0158] Above, by means of embodiments 1 through 8, the respective basic configurations were shown; it is also possible to change the circuit configuration, for example, to change when constituting in a so-called decoder type circuit without using the shift register described previously for the sampling pulse generating circuit.

[0159] Also, for example, when the capacity of the sampling capacitor connected to the sampling transistor is small, it is possible to supply the same data signals via the buffer circuit to each shift register system.

[0160] Furthermore, with embodiments 1 to 8 noted above, it is also possible to monolithically form on the same substrate the source driver and the gate driver as the drive circuit including the sampling circuits, and the display unit consisting of pixel units or the like as the image display unit. In such a case, it is possible to improve the drive force of the pixel transistor that accompanies larger screen size, and to reduce the drive IC mounting costs and the like.

[0161]

[Effect of the Invention] The display device of the invention of claim 1, as described above, has a constitution equipped with a plurality of data signal lines by which data signals are respectively supplied, a plurality of sampling circuits by which the data signals supplied from the plurality of data signal lines are respectively sampled, a plurality of data bus lines respectively connected to the plurality of sampling circuits, a plurality of pixel units connected to the plurality of data bus lines and arranged in matrix form, and a drive circuit including the sampling circuits for driving the data bus lines, wherein at least two of the plurality of data signal lines have the same data signals supplied, and are connected to different sampling circuits via respectively different buffer circuits.

[0162] By doing this, by means of adjacent sampling circuits, there is no effect during mutual turning ON and OFF, and it is possible to reduce the ghost phenomenon by always sampling correct data signals. It is also possible to reduce crosstalk due to the OFF resistance of the transistors of the pixel unit and the sampling circuit unit.

[0163] Therefore, an effect is exhibited of it being possible to have a high-resolution display for which a decrease in display quality due to ghosts and crosstalk is inhibited.

[0164] The display device of the invention of claim 2, as described above, is the display device according to claim 1, wherein of the plurality of sampling circuits, the sampling circuits for which the timing of the sampling is synchronized are connected to respectively different data signal lines, and there is no time overlap of the ON time of the respective sampling circuits.

[0165] By doing this, in addition to the effects of claim 1, the effect is exhibited of it being possible to reduce the noise that occurs due to another sampling circuit being in an ON state at the moment that the sampling circuit goes to the OFF state.

[0166] The display device of the invention of claim 3, as described above, is the display device according to claim 1 or 2, wherein the buffer circuits are formed on the same substrate as the sampling circuits.

[0167] By doing this, it is possible to suppress the degradation of data signals related to contact resistance due to the flexible substrate or the like that connects the buffer circuits and the sampling circuits. It is also possible to suppress an increase in the connection terminals for connecting the buffer circuits and the sampling circuits, exhibiting an effect of being able to improve reliability with mounting.

[0168] The display device of the invention of claim 4, as described above, is equipped with a plurality of data signal lines by which data signals are respectively supplied, a plurality of sampling circuits by which the data signals supplied from the plurality of data signal lines are respectively sampled, a plurality of data bus lines respectively connected to the plurality of sampling circuits, a plurality of pixel units connected to the plurality of data bus lines and arranged in matrix form, and a drive circuit including the sampling circuits for driving the data bus lines, wherein the data signal line is divided into a plurality in the horizontal direction of the display, and each divided signal line is connected to sampling circuits via respectively different buffer circuits.

[0169] By doing this, it is possible to reduce data signal line resistance and capacitance, thus making it possible to further reduce degradation of the data signals with the data signal line and to reduce noise during sampling.

[0170] The display device of the invention of claim 5, as described above, is equipped with a plurality of data signal lines by which data signals are respectively supplied, a plurality of sampling circuits by which the data signals supplied from the plurality of data signal lines are respectively sampled, a plurality of data bus lines respectively connected to the plurality of sampling circuits, a plurality of pixel units connected to the plurality of data bus lines and arranged in matrix form, and a drive circuit including the sampling circuits for driving the data bus lines, wherein of the plurality of pixel units, respectively different data bus lines are connected to the plurality of pixel units adjacent in the column direction, and the same sampling circuits are connected via the buffer circuits to these data bus lines.

[0171] By doing this, it is possible to inhibit interference of pixel units adjacent in the column direction, so it is possible to reduce crosstalk between pixel units, and as a result, an effect is exhibited of being able to improve the display quality.

[0172] The display device of the invention of claim 6, as described above, is the display device according to claim 1, 2, 3, 4 or 5, wherein a drive circuit and an image display unit consisting of the plurality of pixel units are formed monolithically on the same substrate.

[0173] By doing this, an effect is exhibited of being able to improve the drive force of the pixel transistors accompanying larger screen size, and to reduce the drive IC mounting cost and the like.

[Brief Description of the Drawings]
[FIG. 1] is a schematic constitution block diagram of the source driver of the LCD of an embodiment of the present invention.
[FIG. 2] is a schematic constitution block diagram of an LCD equipped with the source driver shown in FIG. 1.
[FIG. 3] is an operation timing chart of the source driver shown in FIG. 1.
[FIG. 4] is a schematic constitution block diagram of an LCD of another embodiment of the present invention.
[FIG. 5] is a schematic constitution block diagram of the source driver of an LCD of yet another embodiment of the present invention.
[FIG. 6] is an operation timing chart of the source driver shown in FIG. 5.
[FIG. 7] is a schematic constitution block diagram of an LCD of yet another embodiment of the present invention.
[FIG. 8] is a schematic constitution block diagram of the source driver of an LCD of yet another embodiment of the present invention.
[FIG. 9] is a schematic constitution block diagram of LCD of yet another embodiment of the present invention.
[FIG. 10] is a schematic constitution block diagram of an LCD of yet another embodiment of the present invention.
[FIG. 11] is a schematic constitution block diagram of the source driver of an LCD of yet another embodiment of the present invention.
[FIG. 12] is a schematic constitution block diagram of a prior art LCD.
[FIG. 13] is a schematic constitution block diagram of a source driver equipped with the LCD shown in FIG. 12.
[FIG. 14] is a schematic constitution block diagram of another prior art source driver.
[FIG. 15] is an operation timing chart of the source driver shown in FIG. 14.

[Explanation of Codes]

1	Display unit (image display unit)
2	Source driver (driver circuit)
3	Gate driver (driver circuit)
4	Pixel unit
5	Source bus line (drive circuit)
6	Gate bus line (drive circuit)
10	Source shift register
11	Sampling hold circuit
12	Data signal line
13 to 15	Buffer circuit
16 to 18	Data signal line
19 to 23	Sampling switch (sampling circuit)
24 to 28	Sampling capacitor (sampling circuit)
41	Source driver (drive circuit)
51	Data signal line
52, 53	Buffer circuit
54, 55	Data signal line
61	Source driver (drive circuit)
62 to 66	Buffer circuit
54, 55	Data signal line
73, 74	Data signal line
75 to 80	Buffer circuit

FIG. 11

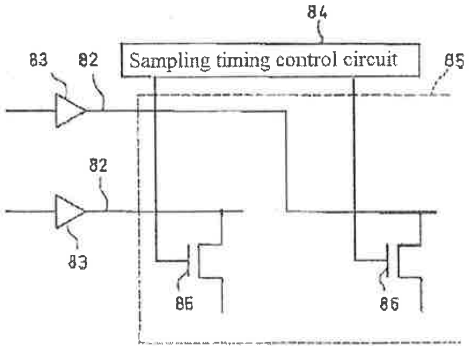


FIG. 1

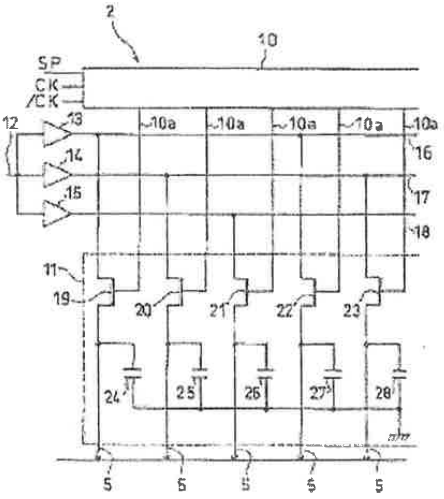


FIG. 2

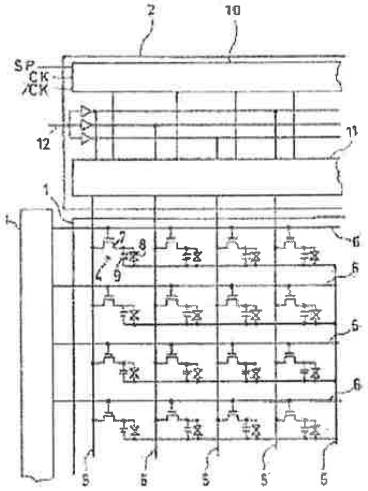


FIG. 3

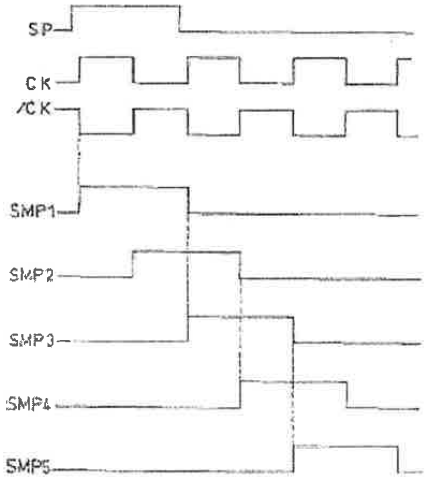


FIG. 4

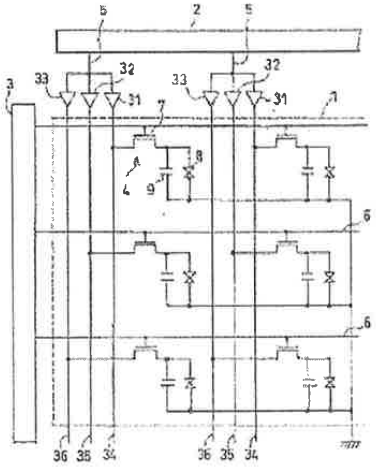


FIG. 5

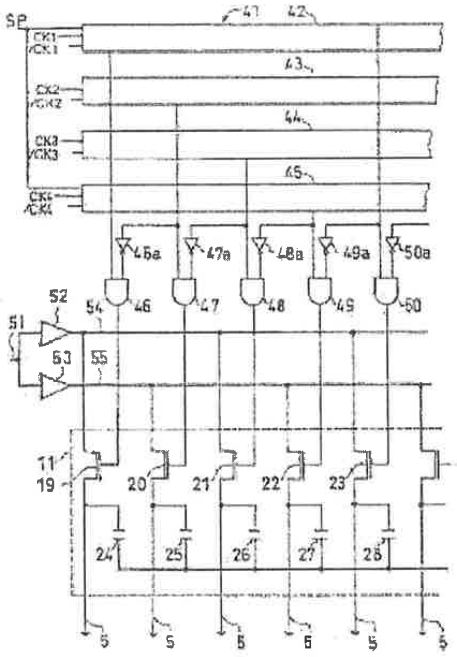


FIG. 6

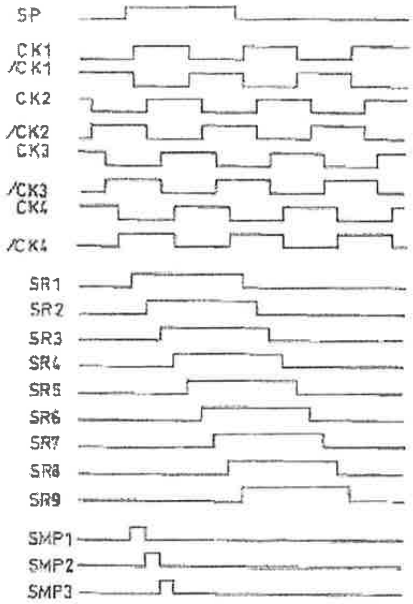


FIG. 7

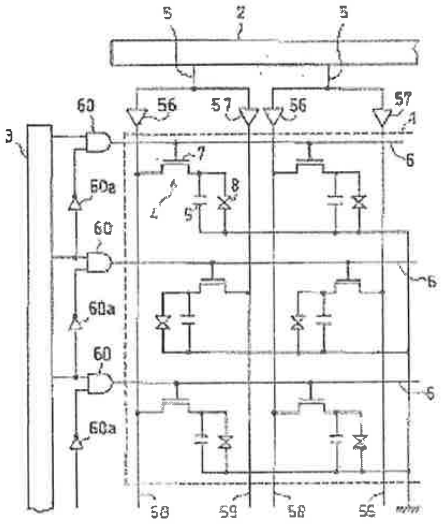


FIG. 8

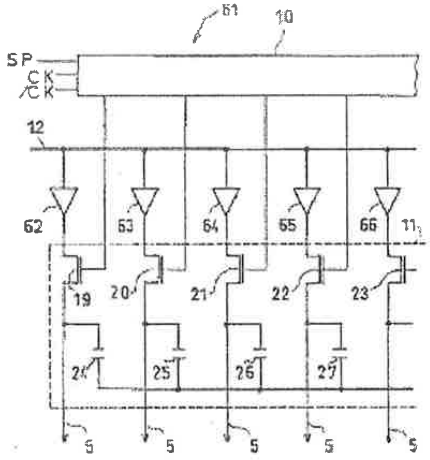


FIG. 9

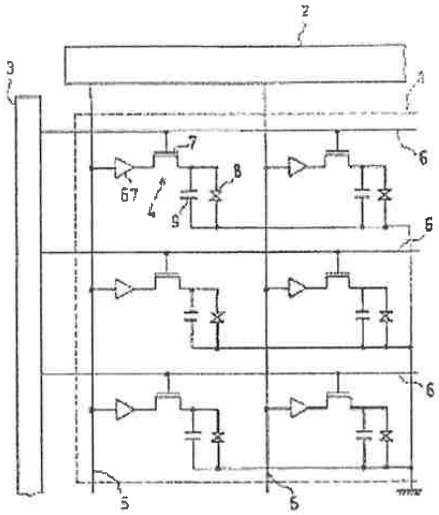


FIG. 13

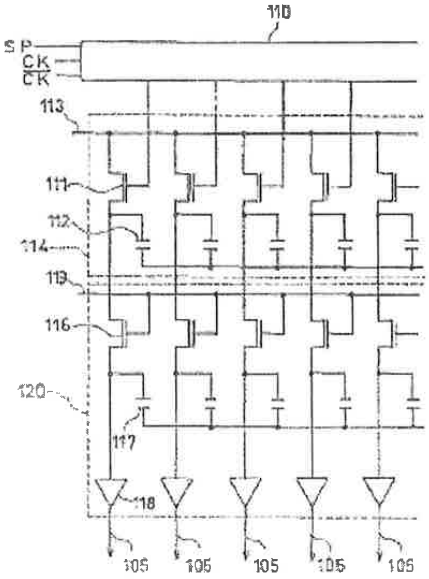


FIG. 14

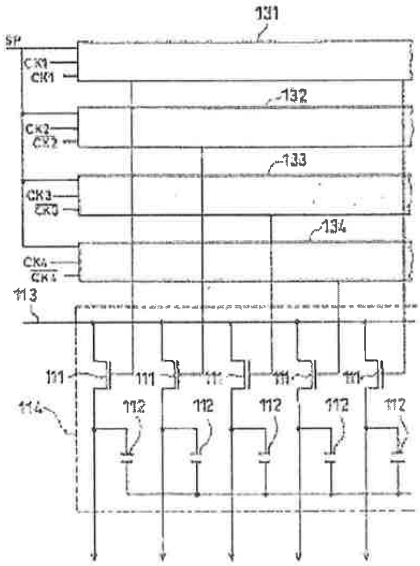


FIG. 10

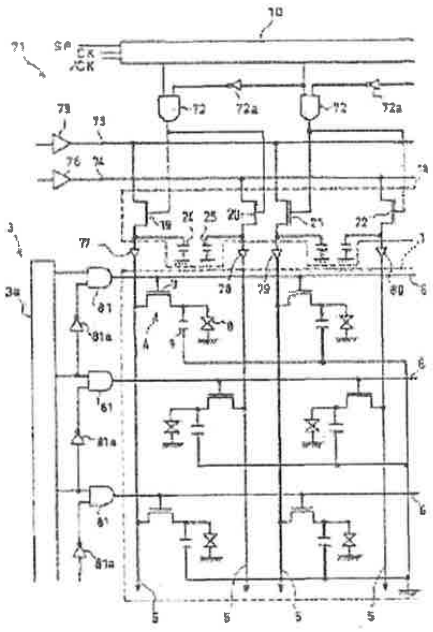


FIG. 12

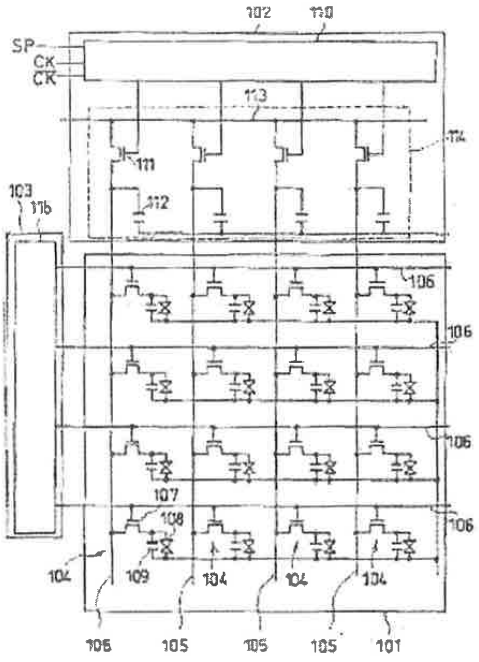
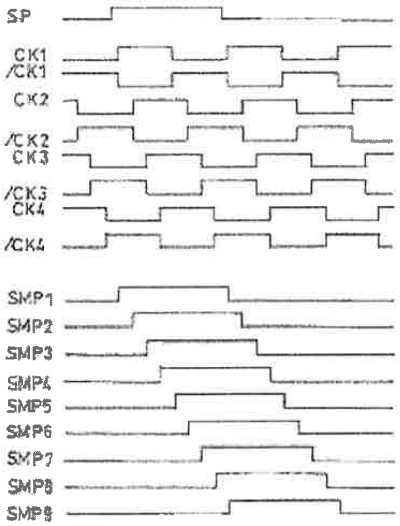


FIG. 15



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(51)Int.Cl.[6]		識別記号	庁内整理番号	ＦＩ			技術表示箇所
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Ｇ０２Ｆ	1/133	５０５		Ｇ０２Ｆ	1/133	５０５	
		５５０				５５０	
Ｈ０４Ｎ	5/66	１０２		Ｈ０４Ｎ	5/66	１０２Ｂ	

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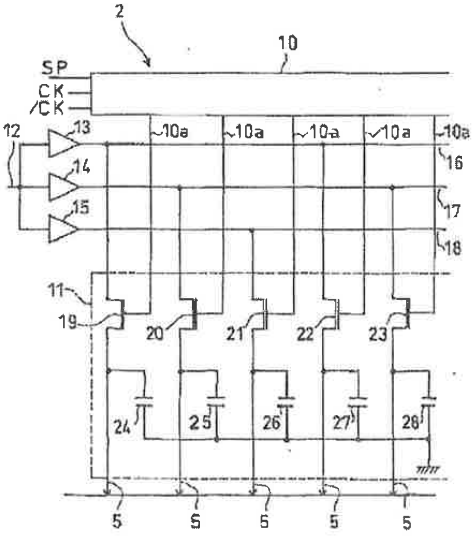
(54)【発明の名称】　表示装置

(57)【要約】

【構成】　データ信号線１２からの同一のデータ信号が、バッファ回路１３～１５を介して３本のデータ信号線１６～１８に供給された後、サンプルホールド回路１１のサンプリングスイッチ１９～２３に供給される。サンプルホールド回路１１にてサンプリングされたデータ信号は、ソースバスライン５…に供給される。

【効果】　なまりやノイズの少ないデータ信号を正確にサンプリングすることができるので、水平解像度の低下および表示品位の低下を抑えた高解像度の表示が可能となる。



【特許請求の範囲】
【請求項１】データ信号がそれぞれ供給される複数のデータ信号線と、
上記複数のデータ信号線から供給されるデータ信号をそれぞれサンプリングする複数のサンプリング回路と、
上記複数のサンプリング回路にそれぞれ接続される複数のデータバスラインと、
上記複数のデータバスラインに接続されると共に、マトリクス状に配された複数の絵素部と、
上記サンプリング回路を含み、上記データバスラインを駆動する駆動回路とを備え、
上記複数のデータ信号線の少なくとも２本は、同一データ信号が供給されると共に、それぞれが異なるバッファ回路を介して異なるサンプリング回路に接続されていることを特徴とする表示装置。
【請求項２】上記複数のサンプリング回路のうち、サンプリングのタイミングが同期するサンプリング回路は、それぞれ異なるデータ信号線に接続されると共に、それぞれのサンプリング回路のＯＮ期間が時間的に重なりを持たないことを特徴とする請求項１記載の表示装置。
【請求項３】上記バッファ回路は、上記サンプリング回路と同一の基板上に形成されていることを特徴とする請求項１または２記載の表示装置。
【請求項４】データ信号がそれぞれ供給される複数のデータ信号線と、
上記複数のデータ信号線から供給されるデータ信号をそれぞれサンプリングする複数のサンプリング回路と、
上記複数のサンプリング回路にそれぞれ接続される複数のデータバスラインと、
上記複数のデータバスラインに接続されると共に、マトリクス状に配された複数の絵素部と、
上記サンプリング回路を含み、上記データバスラインを駆動する駆動回路とを備え、
上記データ信号線は、表示の水平方向で複数に分断されると共に、分断された各々の信号線は、それぞれ異なるバッファ回路を介してサンプリング回路に接続されていることを特徴とする表示装置。
【請求項５】データ信号がそれぞれ供給される複数のデータ信号線と、
上記複数のデータ信号線から供給されるデータ信号をそれぞれサンプリングする複数のサンプリング回路と、
上記複数のサンプリング回路にそれぞれ接続される複数のデータバスラインと、
上記複数のデータバスラインに接続されると共に、マトリクス状に配された複数の絵素部と、
上記サンプリング回路を含み、上記データバスラインを駆動する駆動回路とを備え、
上記複数の絵素部のうち、列方向に隣接する複数の絵素部には、それぞれ異なるデータバスラインが接続されると共に、これらデータバスラインには、バッファ回路を介して同一のサンプリング回路が接続されていることを特徴とする表示装置。
【請求項６】上記駆動回路と、上記複数の絵素部からなる画像表示部とが同一基板上にモノリシックに形成されていることを特徴とする請求項１、２、３、４または５記載の表示装置。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、液晶表示装置等の表示装置に関するものである。
【０００２】
【従来の技術】従来より、表示装置として、例えば液晶表示装置（以下、ＬＣＤと称する）は、図１２に示すように、複数の絵素部１０４…を有する表示部１０１と、各絵素部１０４を駆動する駆動回路としてのソースドライバ１０２およびゲートドライバ１０３とで構成されている。
【０００３】上記各絵素部１０４…は、ソースドライバ１０２に接続された複数のソースバスライン１０５…とゲートドライバ１０３に接続された複数のゲートバスライン１０６…との直交する部分にそれぞれ配置されている。よって、各絵素部１０４…の配置は、表示部１０１上でマトリクス状となる。
【０００４】また、絵素部１０４は、ＴＦＴ(Thin film transistor)からなる絵素トランジスタ１０７と、絵素容量１０８と、付加容量１０９とで構成され、絵素トランジスタ１０７のゲート端子はゲートバスライン１０６に、ソース端子はソースバスライン１０５に、ドレイン端子は絵素容量１０８および付加容量１０９に接続されている。
【０００５】ソースドライバ１０２は、シフトレジスタ１１０と、トランジスタからなるサンプリングスイッチ１１１、サンプリングコンデンサ１１２、データ信号線１１３等で構成され、上記サンプリングスイッチ１１１、サンプリングコンデンサ１１２、データ信号線１１３およびソースバスライン１０５からサンプルホールド回路１１４を形成している。
【０００６】上記シフトレジスタ１１０には、スタートパルス（ＳＰ）、駆動クロック（ＣＫ、／ＣＫ）が入力され、入力されたＳＰは、ＣＫ、／ＣＫに応じて順次シフトしてサンプルホールド回路１１４に出力される。
【０００７】ゲートドライバ１０３は、シフトレジスタ１１５を有し、各ゲートバスライン１０６…に走査信号を順次出力するようになっている。
【０００８】尚、上記表示部１０１、ソースドライバ１０２およびゲートドライバ１０３は、同一基板上にモノリシックに形成されている場合と、表示部１０１のみが絶縁基板上に形成されている場合とがある。
【０００９】ここで、上記構成の表示装置の動作について以下に説明する。まず、ソースドライバ１０２のシフ

トレジスタ１１０に入力されたＳＰは、ＣＫ、／ＣＫにより順次シフトしてサンプルホールド回路１１４に出力され、サンプルホールド回路１１４でのサンプリングパルスとなる。そして、入力されたサンプリングパルスによってサンプリングスイッチ１１１がＯＮ状態となり、このサンプリングパルスが入力された時点でのデータ信号線１１３のデータ信号がサンプリングされる。

【００１０】そして、サンプリングパルスによりサンプリングされたデータ信号は、サンプリングコンデンサ１１２にホールドされソースバスライン信号としてソースバスライン１０５に出力される。

【００１１】一方、ゲートドライバ１０３のシフトレジスタ１１５における各桁の出力は、走査信号（ゲートバスライン信号）として順次ゲートバスライン１０６…に出力され、選択されたゲートバスライン１０６に繋がる絵素トランジスタ１０７をＯＮし、その時点でのソースバスライン信号を画像データとして絵素容量１０８および付加容量１０９に順次書き込んでいく。

【００１２】そして、各絵素部１０４に対応した液晶を駆動させることにより所望する表示を行うようになっている。

【００１３】したがって、上記構成のＬＣＤでは、上述したように、ソースドライバ１０２は、表示部１０１側で画像データを保持するパネルサンプルホールド方式となっている。このようなソースドライバ１０２を有するＬＣＤにおいては、水平走査方向の絵素部１０４が多くなるとシフトレジスタ１１０の最下位桁に繋がる絵素部１０４と最上位桁とに繋がる絵素部１０４とでは、画像データの書込時間が異なる。このため、シフトレジスタ１１０の上位桁に繋がる絵素部１０４では画像データの書込時間を長くすることができるが、下位桁に繋がる絵素部１０４では画像データの書込時間が十分にとれなくなるという問題が生じる。

【００１４】そこで、上記の問題を解決するために、ソースドライバ側で画像データを保持するドライバサンプルホールド方式のソースドライバを使用したＬＣＤが提案されている。

【００１５】以下に、上記ドライバサンプルホールド方式のソースドライバを使用したＬＣＤについて説明する。尚、このＬＣＤでは、ソースドライバ以外は図１２に示すＬＣＤと同様の表示部１０１およびゲートドライバ１０３を有するものとし、ここでの説明は、ドライバサンプルホールド方式のソースドライバについてのみ行う。

【００１６】上記ドライバサンプルホールド方式のソースドライバは、図１２に示すソースドライバ１０２のサンプルホールド回路１１４の出力側に、図１３に示すように、トランスファースイッチ１１６、ホールドコンデンサ１１７、バッファ回路１１８、トランスファー信号線１１９からなるトランスファー回路１２０が接続された構成となっている。

【００１７】即ち、サンプルホールド回路１１４にて１走査線分のデータがサンプリングされた時点で、トランスファー回路１２０にてトランスファー信号線１１９からトランスファー信号が出力され、トランスファースイッチ１１６がＯＮ状態となり、サンプルホールド回路１１４のサンプリングコンデンサ１１２に保持されたデータが一斉にホールドコンデンサ１１７に転送された後、次の走査期間のサンプリングが行われる。

【００１８】つまり、次の１走査線分のデータをサンプリングしている期間、ホールドコンデンサ１１７に保持された前回の１走査線分のサンプリングデータがソースバスライン信号として、バッファ回路１１８を介してソースバスライン１０５（図１２）に印加され続ける。

【００１９】このように、ドライバサンプルホールド方式のソースドライバを使用することで、水平走査方向の絵素部１０４の数が多くなっても、それぞれの絵素部１０４…への画像データの書込時間が十分にとれる。これによって、シフトレジスタ１１０の最下位桁に繋がる絵素部１０４と最上位桁に繋がる絵素部１０４との間において、画像データの書込時間をほぼ同じにすることができる。

【００２０】さらに、上記ＬＣＤが絶縁基板上にドライバモノリシックで形成されている場合、ｐ－ＳｉＴＦＴを用いて形成されるシフトレジスタを安定して動作させる速度は数ＭＨｚ程度であり、高速動作が要求される水平方向の絵素数が多いＬＣＤのソースドライバ内のシフトレジスタでは、シフトレジスタの動作速度が不足するといった不具合が生じる。

【００２１】そこで、シフトレジスタの動作速度を低減するために、例えば図１４に示すように、複数系統、この場合４系統のシフトレジスタ１３１～１３４を設けて、それぞれのシフトレジスタ１３１～１３４には、位相の異なるＣＫ１～ＣＫ４、／ＣＫ１～／ＣＫ４で動作させることにより、全体のシフト速度はそのままで、各段のシフトレジスタ１３１～１３４を低速で動作させるソースドライバが提案されている。

【００２２】上記４系統のシフトレジスタ１３１～１３４を有するソースドライバでは、図１５に示すように、スタートパルスＳＰをＣＫ１～ＣＫ４、／ＣＫ１～／ＣＫ４によって順次シフトし、サンプリングパルスＳＭＰ１～ＳＭＰ８を出力するようになっている。尚、４系統のシフトレジスタ１３１～１３４の出力であるＳＭＰ１～ＳＭＰ８の幅は、シフトレジスタが１系統の時の４倍となっているが、各ＳＭＰ１～ＳＭＰ８の位相のずれはシフトレジスタが１系統の時と同じである。

【００２３】

【発明が解決しようとする課題】ところが、上記４系統のシフトレジスタ１３１～１３４を有するソースドライバでは、図１５に示すように、各サンプリングパルスＳ

ＭＰ１～ＳＭＰ８が互いにオーバーラップする形となる。このため、ある瞬間をみた場合、常に８個のサンプリングトランジスタ１１１…がＯＮとなっている。つまり、データ信号線１１３、或いはデータ信号出力回路に対しては、サンプリングトランジスタ１１１…を介して８個のサンプリングコンデンサ１１２…の容量がその負荷となる。さらに、データ信号線１１３には配線抵抗が、また、サンプリングトランジスタ１１１にはＯＮ抵抗が存在するため、各サンプリングコンデンサ１１２でのデータ信号はＲＣ積分回路の時定数の作用で応答が悪化し、元のデータ信号と比べて波形のなまったものとなる。

【００２４】このようになまった波形をもとになされるデータ信号のサンプリングでは、元々データ信号が有する帯域情報が失われているので、水平解像度の低い表示となる。さらに、走査信号においても（図示しない）、構成によってはゲートシフトレジスタの隣接する２つの出力がオーバーラップしており絵素部分についても上記したソースドライバのサンプリング部と同様の不具合を生じる。

【００２５】このような不具合を防ぐために、各シフトレジスタ１３１～１３４毎に、映像信号線を配設した表示装置が提案されている。この場合、例えば、図１５に示すサンプリングパルスのＮ番目（ＳＭＰ１）の立ち下がりと、Ｎ＋８番目（ＳＭＰ９）の立ち上がりとが同一のタイミングとなっているが、実際には信号波形のなまりや遅延により、Ｎ番目のサンプリングトランジスタ１１１が完全にＯＦＦとなる前にＮ＋８番目のサンプリングトランジスタ１１１が同時にＯＮする現象が生じる。

【００２６】このような現象が生じると、上述のように、映像信号線を複数に分けたとしても、ソースドライバのＮ番目のサンプルホールド回路１１４のサンプリングデータはＮ＋４のサンプリング信号のみならず、Ｎ＋８番目のサンプリングデータによっても影響を受けることになり、ゴースト現象或いはノイズとして表示に悪影響を与えることになる。

【００２７】さらに、上述の現象は、表示部でも同様に起こり得る。このため、例えば、本件出願人は、特願平５－３００５３７号において、同一の映像信号線を駆動回路の外部で複数に分岐した表示装置を提案している。このように、同一の映像信号線を駆動回路の外部で複数に分岐することで、一本の映像信号線に接続されたサンプリング回路が同時に複数個ＯＮとなることがなく、これによって、各映像信号線中の信号のなまりを小さくし、表示装置の解像度を向上させている。

【００２８】ところで、同一の映像信号線を単に複数に分割しても、パネルと同一基板上で複数に分割している場合には、フレキシブル基板等との接触抵抗、配線抵抗、更には映像信号供給源の出力インピーダンスにより、時定数を大きくはできるが、ゴーストの発生を完全に抑えることはできない。また、パネル外部で同一の映像信号線を単に複数に分割しても、上記したフレキシブル基板等との接触抵抗、配線抵抗、更には映像信号供給源の出力インピーダンスにより、時定数を大きくはできるが、ゴーストの発生を完全に抑えることはできない。

【００２９】また、ソースドライバを構成する同一のデータ信号線に繋がるサンプリング回路についてみてみると、サンプリングトランジスタにはＯＦＦ抵抗が存在するが、サンプリングトランジスタのＯＦＦ抵抗が十分に大きくないと、サンプリングコンデンサに書き込まれているサンプリングデータがトランジスタのＯＦＦ抵抗、データ信号線を通してお互いにクロストークするという不具合が生じる。

【００３０】本発明は、上記の各問題点に鑑みなされたものであって、その目的は、隣接するトランジスタが同時にＯＮすることによる、データ信号のなまりや、データ信号のノイズを低減させると共に、トランジスタのＯＦＦ特性の不足および低下によるクロストークを低減し、ゴースト現象を防止すると共に、水平解像度の低下やクロストークによる表示品位の低下を抑えた高解像度の表示を実現し得る表示装置を提供することにある。

【００３１】

【課題を解決するための手段】請求項１の表示装置は、データ信号がそれぞれ供給される複数のデータ信号線と、上記複数のデータ信号線から供給されるデータ信号をそれぞれサンプリングする複数のサンプリング回路と、上記複数のサンプリング回路にそれぞれ接続される複数のデータバスラインと、上記複数のデータバスラインに接続されると共に、マトリクス状に配された複数の絵素部と、上記サンプリング回路を含み、上記データバスラインを駆動する駆動回路とを備え、上記複数のデータ信号線の少なくとも２本は、同一データ信号が供給されると共に、それぞれが異なるバッファ回路を介して異なるサンプリング回路に接続されていることを特徴としている。

【００３２】請求項２の表示装置は、請求項１記載の表示装置において、複数のサンプリング回路のうち、サンプリングのタイミングが同期するサンプリング回路は、それぞれ異なるデータ信号線に接続されると共に、それぞれのサンプリング回路のＯＮ期間が時間的に重なりを持たないことを特徴としている。

【００３３】請求項３の表示装置は、請求項１または２記載の表示装置において、バッファ回路は、サンプリング回路と同一の基板上に形成されていることを特徴としている。

【００３４】請求項４の表示装置は、データ信号がそれぞれ供給される複数のデータ信号線と、上記複数のデータ信号線から供給されるデータ信号をそれぞれサンプリングする複数のサンプリング回路と、上記複数のサンプリング回路にそれぞれ接続される複数のデータバスライ

ンと、上記複数のデータバスラインに接続されると共に、マトリクス状に配された複数の絵素部と、上記サンプリング回路を含み、上記データバスラインを駆動する駆動回路とを備え、上記データ信号線は、表示の水平方向で複数に分断されると共に、分断された各々の信号線は、それぞれ異なるバッファ回路を介してサンプリング回路に接続されていることを特徴としている。

【００３５】請求項５の表示装置は、データ信号がそれぞれ供給される複数のデータ信号線と、上記複数のデータ信号線から供給されるデータ信号をそれぞれサンプリングする複数のサンプリング回路と、上記複数のサンプリング回路にそれぞれ接続される複数のデータバスラインと、上記複数のデータバスラインに接続されると共に、マトリクス状に配された複数の絵素部と、上記サンプリング回路を含み、上記データバスラインを駆動する駆動回路とを備え、上記複数の絵素部のうち、列方向に隣接する複数の絵素部には、それぞれ異なるデータバスラインが接続されると共に、これらデータバスラインには、バッファ回路を介して同一のサンプリング回路が接続されていることを特徴としている。

【００３６】請求項６の表示装置は、請求項１、２、３、４または５記載の表示装置において、駆動回路と、複数の絵素部からなる画像表示部とが同一基板上にモノリシックに形成されていることを特徴としている。

【００３７】

【作用】請求項１の構成によれば、複数のデータ信号線の少なくとも２本は、同一データ信号が供給されると共に、それぞれが異なるバッファ回路を介して異なるサンプリング回路に接続されていることで、同一データ信号が供給される隣接するサンプリング回路の電気的な繋がりを疎にすることができる。

【００３８】これにより、同一データ信号が供給される隣接するサンプリング回路が同時にＯＮ状態となっても、このときに発生するノイズによって、同一データ信号が供給される他の隣接するサンプリング回路に影響を与えないようになる。即ち、上記ノイズによって誤ったデータ信号がサンプリングされないようになる。

【００３９】また、隣接するサンプリング回路が同一データ信号線に接続されていないことから、一本のデータ信号線の負荷を低減することができるので、データ信号のなまりを低減することができる。

【００４０】したがって、隣接するサンプリング回路では、データ信号のなまりによる誤サンプリングが無く、且つ互いにＯＮ・ＯＦＦ時の影響を受ず、常に正確なデータ信号をサンプリングし、サンプリングしたデータ信号をデータバスラインに供給することができるので、絵素部でのサンプリング回路のＯＮ・ＯＦＦ特性の不良によるクロストークを低減させることができる。よって、クロストークによる表示品位の低下を抑えた高解像度の表示を可能としている。

【００４１】請求項２の構成によれば、サンプリングのタイミングが同期するサンプリング回路が、それぞれ異なるデータ信号線に接続されると共に、それぞれのサンプリング回路のＯＮ期間が重ならないことで、一つのサンプリング回路がＯＦＦ状態となる瞬間に他のサンプリング回路がＯＮ状態となることにより生じるノイズの低減を図ることができる。

【００４２】請求項３の構成によれば、サンプリング回路に接続されたバッファ回路が、サンプリング回路と同一の基板上に形成されていることで、バッファ回路とサンプリング回路とを接続するフレキシブル基板等の接触抵抗、配線抵抗等によるデータ信号の劣化を抑制することができる。また、バッファ回路とサンプリング回路とを接続するための接続端子の増加を抑制でき、実装に伴う信頼性を向上させることができる。

【００４３】請求項４の構成によれば、データ信号線は、表示の水平方向で複数に分断されると共に、分断された各々の信号線は、それぞれ異なるバッファ回路を介してサンプリング回路に接続されていることで、データ信号線に対する負荷を低減することができる。これにより、データ信号線の抵抗および容量を低減することができるので、よりデータ信号線におけるデータ信号の劣化を低減させ、サンプリング時のノイズの低減を図ることができる。

【００４４】請求項５の構成によれば、複数の絵素部のうち、列方向に隣接する複数の絵素部には、それぞれ異なるデータバスラインが接続されると共に、これらデータバスラインには、バッファ回路を介して同一のサンプリング回路が接続されていることで、列方向に隣接する絵素部の干渉を抑えることができる。これにより、絵素部同士のクロストークを低減することができるので、表示品位を向上させることができる。

【００４５】請求項６の構成によれば、駆動回路と、複数の絵素部からなる画像表示部とが同一基板上にモノリシックに形成されていることで、大画面化に伴う画素トランジスタの駆動力向上や、駆動ＩＣの実装コストの低減等を図ることができる。

【００４６】

【実施例】

〔実施例１〕本発明の一実施例について図１ないし図３に基づいて説明すれば、以下の通りである。尚、本実施例では、表示装置として液晶表示装置（以下、ＬＣＤと称する）について説明し、後述する他の実施例においても同様とする。

【００４７】本実施例に係るＬＣＤは、図２に示すように、マトリクス状に配された複数の絵素部４…を有する表示部１と、各絵素部４…を駆動する駆動回路としてのソースドライバ２およびゲートドライバ３とから構成されている。

【００４８】表示部１には、ソースドライバ２に接続さ

れた複数のソースバスライン５…と、ゲートドライバ３に接続された複数のゲートバスライン６…とが直交するように配置されており、ソースバスライン５とゲートバスライン６との交差部に絵素部４が配置されている。即ち、表示部１は、ソースドライバ２からの映像信号等のデータ信号とゲートドライバ３からの走査信号とによって絵素部４を駆動させ、図示しない液晶層の液晶の配向状態を変化させて所望する画像を表示するようになっている。

【００４９】上記絵素部４は、ＴＦＴ(Thin film transistor)からなる絵素トランジスタ７と、絵素容量８と、付加容量９とで構成され、絵素トランジスタ７のゲート端子はゲートバスライン６に、ソース端子はソースバスライン５に、ドレイン端子は絵素容量８および付加容量９に接続されている。即ち、絵素トランジスタ７は、走査信号によってＯＮされると、絵素容量８および付加容量９にソースバスライン５からのソースバスライン信号（映像信号）が書き込まれるようになっている。

【００５０】ソースドライバ２には、ソースシフトレジスタ１０と、ソースシフトレジスタ１０からのサンプリングパルスによってデータ信号線１２からのデータ信号をサンプリングするサンプルホールド回路１１とが設けられている。尚、上記データ信号線１２は、ソースドライバ２内で３つに分岐され、バッファ回路１３～１５を介して３つのデータ信号線１６～１８に接続されている。尚、本実施例では、上記バッファ回路１３～１５をソースドライバ２内に設けたが、これに限定されるものでなく、外部に設けても良い。即ち、データ信号線１２をソースドライバ２内で分岐するのではなく、ソースドライバ２の外部で分岐しても良い。

【００５１】上記ソースシフトレジスタ１０には、スタートパルス（ＳＰ）、駆動クロック（ＣＫ、／ＣＫ）が入力され、入力されたＳＰは、ＣＫ、／ＣＫに応じて順次シフトし、サンプリングパルスとしてサンプルホールド回路１１に出力される。

【００５２】サンプルホールド回路１１には、図１に示すように、データ信号線１２からのデータ信号がバッファ回路１３～１５を介して接続された３つのデータ信号線１６～１８から供給され、上記ソースシフトレジスタ１０からのサンプリングパルスに応じて上記データ信号をサンプリングするようになっている。即ち、同一データ信号が３つに分岐され、それぞれの信号が別々にサンプリングされる。

【００５３】上記サンプルホールド回路１１は、ソースシフトレジスタ１０のサンプリングパルスに応じてデータ信号を順次サンプリングするＴＦＴからなるサンプリングスイッチ１９～２３と、サンプリングしたデータを保持するホールドコンデンサ２４～２８とを有している。尚、一つのサンプリングスイッチと、それに接続された一つのサンプリングコンデンサとで一つのサンプリング回路を構成している。

【００５４】上記サンプリングスイッチ１９～２３のゲート端子には、上記ソースシフトレジスタ１０からの出力線１０ａ…がそれぞれ接続され、ソース端子には、一本のデータ信号線１２から分岐されたデータ信号線１６～１８がそれぞれ接続されている。つまり、サンプリングスイッチ１９のソース端子には、データ信号線１６が接続され、サンプリングスイッチ２０のソース端子には、データ信号線１７が接続され、サンプリングスイッチ２１のソース端子には、データ信号線１８が接続され、再びサンプリングスイッチ１９のソース端子には、データ信号線１６が接続され、以下、順番にデータ信号線１６～１８が繰り返して接続される。

【００５５】以上のように、上記サンプリングスイッチ１９～２３は、同一のデータ信号線に繋がるサンプリングスイッチ、例えばデータ信号線１６に繋がるサンプリングスイッチ１９とサンプリングスイッチ２２とが同時にＯＮ状態とならないように接続されている。つまり、各サンプリングスイッチ１９～２３は、互いに電気的な繋がりが疎になっている。

【００５６】ここで、上記構成のＬＣＤの動作について、図３の動作タイミングチャートを参照しながら以下に説明する。

【００５７】まず、１走査期間について、ソースドライバ２のソースシフトレジスタ１０に入力されたＳＰは、ＣＫ、／ＣＫにより順次シフトしてサンプルホールド回路１１に出力され、サンプルホールド回路１１でのサンプリングパルスとなる。そして、入力されたサンプリングパルスによって各サンプリングスイッチ１９～２３がＯＮ状態となり、このサンプリングパルスが入力された時点でのデータ信号線１６～１８のデータ信号がサンプリングされる。

【００５８】そして、サンプリングパルスによりサンプリングされた各データ信号は、各ホールドコンデンサ２４～２８で保持されソースバスライン信号としてソースバスライン５…に出力される。

【００５９】一方、ゲートドライバ３における各行の出力は、走査信号（ゲートバスライン信号）として順次ゲートバスライン６…に出力され、選択されたゲートバスライン６に繋がる絵素トランジスタ７をＯＮし、その時点で、１走査期間の上記ソースバスライン５からのソースバスライン信号を画像データとして絵素容量８および付加容量９に順次書き込んでいく。

【００６０】そして、各絵素部４に対応した液晶を駆動させることにより所望する表示を行う。

【００６１】次の走査期間では、電圧極性を反転させたソースバスライン信号を画像データとして絵素容量８および付加容量９に書き込む。このようにして、走査期間が切り替わる毎に、ソースバスライン信号の電圧極性を反転させて画像データとして絵素容量８および付加容量

９に書き込んでいき、その都度、各絵素部４に対応した液晶を駆動させることにより所望する表示を行う。

【００６２】したがって、上記ソースドライバ２は、図３に示すように、ＳＰが入力されると、ＣＫ、／ＣＫの入力タイミングによって、１／２だけ位相がずれるようにしてサンプリングパルスＳＭＰ１～ＳＭＰ５を出力するようになっている。これにより、各サンプリングパルスＳＭＰ１～ＳＭＰ５は、時間的な重なりを有するので、隣接する２つのサンプリングスイッチが常にＯＮ状態となっている。

【００６３】ところが、本実施例では、上記サンプリングスイッチ１９～２３は、互いに電気的な繋がりが疎になっている。即ち隣接する２つのサンプリングスイッチが同一データ信号線に接続されていないので、一本のデータ信号線の負荷を、サンプリングコンデンサ２つ分から１つ分に低減することができる。この結果、データ信号線の負荷によるデータ信号のなまりを低減することができる。

【００６４】さらに、各サンプリングパルスは１／２ずつ位相がずれているので、図３に示すように、サンプリングパルスＳＭＰ１の立ち下がりと、サンプリングパルスＳＭＰ３の立ち上がりとは時間的に重なりがないようになっている。実際には、サンプリングパルスのなまりや遅延によって、サンプリングトランジスタ１９とサンプリングトランジスタ２１とが同時にＯＮ状態となる時間が生じている。

【００６５】この場合、サンプリングトランジスタ１９とサンプリングトランジスタ２１とが同一のデータ信号線に接続されていれば、サンプリングトランジスタ１９がＯＦＦとなる時に、サンプリングトランジスタ２１がＯＮとなる時に生じるノイズの影響を受けて誤ったデータ信号がサンプリングされることになる。

【００６６】しかしながら、本実施例では、図１に示すように、サンプリングトランジスタ１９とサンプリングトランジスタ２１とが、それぞれ異なるデータ信号線に接続されているので、上記したようなサンプリングパルスのなまりや遅延により生じるノイズの影響を受けずに、正確なデータ信号をサンプリングすることが可能となる。

【００６７】このように、隣接するサンプリングトランジスタ同士において、互いにＯＮ・ＯＦＦ時の影響を受ず、常に正確なデータ信号をソースバスライン信号としてソースバスライン５に供給することができるので、ゴースト現象を低減できる。

【００６８】よって、本実施例のＬＣＤは、データ信号のなまりやノイズが原因のゴースト現象による表示品位の低下を抑えた高解像度の表示を可能としている。

【００６９】尚、本実施例では、ソースドライバ２における各サンプリングスイッチ１９～２３ができるだけ電気的な繋がりが疎になるように、データ信号線１２を３つに分岐した後、バッファ回路１３～１５を介してデータ信号線１６～１８から、データ信号を各サンプリングスイッチ１９～２３に供給している。

【００７０】しかしながら、上記したバッファ回路１３～１５を介することに限定されず、例えばバッファ回路１３～１５を設けないでデータ信号線１２を３つに分岐した後、データ信号を直接各サンプリングスイッチ１９～２３に供給しても良い。この場合、バッファ回路１３～１５を介した場合よりも、各サンプリングスイッチ１９～２３は電気的に疎になり難いので、その効果は半減する。

【００７１】また、本実施例では、ソースドライバ２におけるサンプリング方式は、表示部１側でデータ信号としての画像データを保持するパネルサンプルホールド方式となっているがソースドライバ側で画像データを保持するドライバサンプルホールド方式のソースドライバにおいても同様に適用でき、同様の効果を得ることができる。この場合、ドライバサンプルホールド方式のソースドライバを使用することで、ソースドライバに繋がる絵素部では画像データの書込時間を十分にとることができる。

【００７２】〔実施例２〕本発明の他の実施例について図４に基づいて説明すれば、以下の通りである。尚、説明の便宜上、前記実施例１と同一の機能を有する部材には、同一の符号を付記し、その説明を省略する。以下の各実施例についても同様とする。また、本実施例では、上記実施例１のソースドライバ２に適用した構成をＬＣＤの表示部１に適用した場合について説明する。

【００７３】本実施例に係るＬＣＤは、上記実施例１のソースドライバ２に接続されたソースバスライン５…が、図４に示すように、表示部１の手前で、３つに分岐し、３つのバッファ回路３１～３３を介してそれぞれソースバスライン３４～３６に接続されている。図４において、左右方向を行方向、上下方向を列方向とする。

【００７４】上記ソースバスライン３４～３６には、列方向に配置された絵素トランジスタ７のソース端子が、列方向に隣接する絵素トランジスタ７同士が同一のソースバスラインに繋がらなように接続されている。

【００７５】尚、本実施例におけるＬＣＤの動作は、表示部１に供給されるソースバスライン信号が３つに分岐されて供給される他は、上記実施例１のＬＣＤと同様である。

【００７６】上記の構成において、列方向に隣接した絵素トランジスタ７同士は、互いに別のソースバスラインに接続されているので、絵素トランジスタ７がＯＮ・ＯＦＦしても、互いに影響を及ぼし合わない。これによって、隣接する絵素部４…は、互いに隣接する絵素トランジスタ７がＯＮ・ＯＦＦするときに生じるノイズの影響を受けないので、ゴースト現象の無い高解像度の画像を得ることができる。

【００７７】また、上記ソースドライバ２を、上記実施例１の図１に示すように構成しても良い。この場合、なまりや遅延の無いデータ信号を表示部１に供給でき、しかも、表示部１において、データ信号をなまりや遅延なく書き込めるので、さらに表示品位の向上したＬＣＤを提供することができる。

【００７８】〔実施例３〕本発明のさらに他の実施例について図５および図６に基づいて説明すれば、以下の通りである。

【００７９】本実施例の表示装置は、前記実施例１の図１に示すソースドライバ２に代えて、図５に示すように、ソースドライバ４１を備えている。

【００８０】ソースドライバ４１は、図５に示すように、４系統のシフトレジスタ４２～４５と、このシフトレジスタ４２～４５からの出力に基づいて論理積を得るためのＡＮＤ回路４６～５０と、ＡＮＤ回路４６～５０からのサンプリングパルスが供給されるサンプルホールド回路１１とから構成されている。

【００８１】上記ＡＮＤ回路４６～５０は、それぞれ一つ後の桁のシフトレジスタからの出力を反転するインバータ４６ａ～５０ａが接続されており、各シフトレジスタ４２～４５の出力と、一つ後の桁の出力の反転信号との論理積を得て、得られた論理積をサンプリングパルスとしてサンプルホールド回路１１に供給するようになっている。

【００８２】サンプルホールド回路１１には、サンプリングパルスの他に、データ信号線５１からの映像信号等のデータ信号が供給されるようになっている。

【００８３】上記データ信号線５１は、表示部１内部あるいはソースドライバ４１外部にて２つに分岐された後、バッファ回路５２・５３を介してデータ信号線５４・５５に接続されている。データ信号線５４は、サンプリングスイッチ１９・２１・２３の各ソース端子に接続され、また、データ信号線５４は、サンプリングスイッチ２０・２２の各ソース端子に接続されている。これにより、サンプリングスイッチ１９～２３は、交互にデータ信号線５４・５５に接続され、互いに電気的な繋がりが疎となっている。

【００８４】ここで、上記構成のソースドライバ４１の動作について以下に説明する。上記の４系統のシフトレジスタ４２～４５には、図６に示すように、ＳＰ、それぞれ位相の異なるＣＫ、／ＣＫが入力される。このとき、各シフトレジスタ４２～４５の出力信号ＳＲ１～ＳＲ９は、位相が１／８ずつずれてシフトするようなパルスとなっている。

【００８５】上記シフトレジスタ出力ＳＲｉと、そのひとつ後の桁のシフトレジスタ出力ＳＲｉ＋１の反転信号とは、ＡＮＤ回路４６～５０に入力される。そして、ＡＮＤ回路４６～５０にて得られた論理積をサンプリングパルスＳＭＰ１～３としてサンプルホールド回路１１の各サンプリングスイッチ１９～２３に入力される。

【００８６】一方、上記サンプリングスイッチ１９～２３には、データ信号線５１から供給されたデータ信号が交互に接続されたデータ信号線５４・５５を介してそれぞれ入力される。

【００８７】そして、サンプリングパルスＳＭＰ１～ＳＭＰ３によりサンプリングされた各データ信号は、各ホールドコンデンサ２４～２８で保持されソースバスライン信号としてソースバスライン５…に出力される。

【００８８】上記の構成において、上記サンプリングパルスＳＭＰ１～３は、図６に示すように、シフトレジスタ４２～４３の出力ＳＲｉをＡＮＤ回路４６～５０にて互いに時間的に重なりのない短いパルスとなっている。これにより、同時に２つ以上のサンプリングパルスがＯＮ状態とならない。

【００８９】このように、常にサンプリングスイッチ１９～２３のうち、一つのみがＯＮ状態となっているので、データ信号線５４・５５からみた負荷は、サンプリングコンデンサ一つ分である。したがって、ＡＮＤ回路を用いずに４系統のシフトレジスタ構成したソースドライバ、例えば従来の技術に示したソースドライバに比べて、データ信号線の負荷を１／８に低減できるので、データ信号のなまりを低減することができる。また、データ信号線の負荷を１／８に低減できることから、シフトレジスタからの出力ＣＲの時定数も１／８にすることができるので、データ信号のなまりを従来よりも小さくできる。

【００９０】ところで、各サンプリングパルスＳＭＰ１～３は、実際にはデータ信号の遅延やなまり等により、ＳＭＰｉ（ｉ＝整数）の立ち下がりとＳＭＰｉ＋１の立ち上がりとが同時ではなく、若干オーバーラップする期間が生じている。しかしながら、本実施例では、隣合うサンプリングスイッチが異なるデータ信号線５４・５５に接続されているので、隣合うサンプリングスイッチが同時にＯＮ状態となることから生じるデータ信号線の５４・５５のノイズの影響を受けなくすることができる。

【００９１】したがって、本実施例のＬＣＤは、データ信号線の負荷によるデータ信号のなまりを低減することができると共に、隣接するトランジスタが同時にＯＮ状態となることによるデータ信号のノイズによるゴースト現象の低減ができる。

【００９２】よって、データ信号のなまり、データ信号のノイズが原因で起こるゴースト現象による表示品位の低下を抑えた高解像度の表示を可能としている。

【００９３】尚、本実施例では、シフトレジスタが４系統である場合について説明したが、これに限定されるものではなく、少なくとも２系統以上であれば良い。

【００９４】また、本実施例では、シフトレジスタの出力から論理積を得るために、ＡＮＤ回路を用いたが、これに限定されるものではなく、例えばＮＯＲ回路等を用

いても良く、さらに、ＳＲｉとＳＲｉ＋７のＡＮＤをとる場合、ＡＮＤ回路の入力段に接続されたインバータも特に必要としない。

【００９５】さらに、本実施例では、ソースドライバ４１における各サンプリングスイッチ１９～２３ができるだけ電気的に疎になるように、データ信号線５１を２つに分岐した後、バッファ回路５２・５３を介してデータ信号線５４・５５から、データ信号を各サンプリングスイッチ１９～２３に供給している。

【００９６】しかしながら、上記したバッファ回路５２・５３を介することに限定されず、例えばバッファ回路５２・５３を設けないでデータ信号線５１を２つに分岐した後、データ信号を直接各サンプリングスイッチ１９～２３に供給しても良い。この場合、バッファ回路５２・５３を介した場合よりも、各サンプリングスイッチ１９～２３は電気的に疎になり難いので、その効果は半減する。

【００９７】また、本実施例では、ソースドライバ４１におけるサンプリング方式は、表示部１側でデータ信号としての画像データを保持するパネルサンプルホールド方式となっているがソースドライバ側で画像データを保持するドライバサンプルホールド方式のソースドライバにおいても同様に適用でき、同様の効果を得ることができる。この場合、ドライバサンプルホールド方式のソースドライバを使用することで、ソースドライバに繋がる絵素部では画像データの書込時間を十分にとることができる。

【００９８】〔実施例４〕本発明のさらに他の実施例について図７に基づいて説明すれば、以下の通りである。尚、本実施例では、上記実施例３のソースドライバ４１に適用した構成をＬＣＤの表示部１での信号入力に適用した場合について説明する。

【００９９】本実施例に係るＬＣＤは、図７に示すように、上記実施例３のソースドライバ４１に接続されたソースバスライン５…が、表示部１の手前で、２つに分岐し、２つのバッファ回路５６・５７を介してそれぞれソースバスライン５８・５９に接続された構成となっている。図７において、左右方向を行方向、上下方向を列方向とする。

【０１００】上記ソースバスライン５８・５９には、列方向に配置された絵素トランジスタ７のソース端子が、列方向に隣接する絵素トランジスタ７同士が同一のソースバスラインに繋がらなように接続されている。

【０１０１】また、ゲートドライバ３には、ＡＮＤ回路６０…を介してゲートバスライン６…に接続され、これらＡＮＤ回路６０…には、それぞれ一つ後の行のＡＮＤ回路６０に出力される信号を反転するインバータ６０ａ…が接続されている。上記ＡＮＤ回路６０では、ゲートドライバ３の出力と、一つ後の行のＡＮＤ回路６０へのゲートドライバ３からの出力の反転信号との論理積を得て、得られた論理積をゲート信号としてゲートバスライン６に出力するようになっている。

【０１０２】尚、本実施例におけるＬＣＤの動作は、表示部１に供給されるソースバスライン信号が２つに分岐されて供給され、さらに、ゲートドライバ３から供給されるゲート信号がＡＮＤ回路を介して出力される他は、上記実施例３のソースドライバ４１の動作と同様である。

【０１０３】上記の構成において、絵素トランジスタ７のＯＮ・ＯＦＦを制御するゲート信号がＡＮＤ回路６０を介してゲートバスライン６に出力されるので、各ゲート信号は時間的な重なりを持たないようになる。これにより、隣接する絵素部４…は、互いに隣接する絵素トランジスタ７がＯＮ・ＯＦＦすることによるノイズの影響を受けないので、ゴースト現象の無い高解像度の画像を得ることができる。

【０１０４】また、上記ソースドライバ４１を、上記実施例１の図１に示すように構成しても良い。この場合、なまりや遅延の無いデータ信号を表示部１に供給でき、しかも、表示部１において、データ信号をなまりや遅延なく書き込めるので、さらに表示品位の向上したＬＣＤを提供することができる。

【０１０５】〔実施例５〕本発明のさらに他の実施例について図８に基づいて説明すれば、以下の通りである。

【０１０６】本実施例に係るＬＣＤは、前記実施例１の図１に示すソースドライバ２に代えて、図８に示すように、ソースドライバ６１を備えている。

【０１０７】ソースドライバ６１は、図８に示すように、ソースシフトレジスタ１０と、サンプルホールド回路１１と、データ信号線１２とを備えた構成となっている。

【０１０８】データ信号線１２には、バッファ回路６２～６６が接続されており、これら各バッファ回路６２～６６の出力側は、それぞれサンプルホールド回路１１のサンプリングスイッチ１９～２３の各ソース端子に接続されている。即ち、データ信号線１２から出力されるデータ信号は、バッファ回路６２～６６を介してサンプリングスイッチ１９～２３に供給され、サンプリングコンデンサ２４～２７にそれぞれホールドされるようになっている。

【０１０９】これにより、サンプリングスイッチ１９～２３は、データ信号線１２とバッファ回路６２～６６を介して接続されているので、このバッファ回路６２～６６によって電気的な繋がりが疎になっている。

【０１１０】ここで、上記構成のソースドライバ６１の動作について以下に説明する。上記のソースシフトレジスタ１０に入力されたＳＰは、ソースシフトレジスタ１０に入力されるＣＫ、／ＣＫに応じて順次シフトして出力されていく。そして、出力された各桁のパルスは、サンプルホールド回路１１におけるそれぞれのサンプリン

グスイッチ１９～２３のゲート端子にサンプリングパルスとして順次入力される。

【０１１１】一方、データ信号線１２からのデータ信号は、バッファ回路６２～６６を介してサンプリングスイッチ１９～２３のソース端子に入力される。

【０１１２】したがって、上記ソースシフトレジスタ１０から供給されるサンプリングパルスによってサンプリングスイッチ１９～２３がＯＮ状態となり、データ信号線１２から出力されたデータ信号を各サンプリングコンデンサ２４～２７に保持するようになっている。

【０１１３】ところで、前記実施例１および３に記載のソースドライバ２およびソースドライバ４１に配されたバッファ回路１３～１５、バッファ回路５２・５３では、その負荷はデータ信号線の配線負荷とサンプリングコンデンサの負荷とが合わさったものであるので、バッファ回路を上記負荷に対応し得る大きさの回路にする必要がある。

【０１１４】しかしながら、本実施例のバッファ回路６２～６６では、それぞれにサンプリングコンデンサ２４～２７が一つずつ接続されているので、バッファ回路６２～６６一つに対する負荷は一つのサンプリングコンデンサのみである。このため、前記実施例１および３に記載のバッファ回路１３～１５、バッファ回路５２・５３よりも小さな回路にすることができる。

【０１１５】また、前記実施例１および３では、一つのバッファ回路に不良が生じると、ソースバスラインの３本に１本、或いは２本に１本毎にデータ信号が供給されないようになる。このため、表示部１における全表示の１／３或いは１／２が表示欠陥となる不具合を生じる。

【０１１６】しかしながら、本実施例では、バッファ回路６２～６６に不良が生じた場合、不良発生のバッファ回路に接続されたソースバスラインのみにデータ信号が供給されなくなるだけであるので、表示欠陥も不良発生したバッファ回路に接続されたソースバスラインにのみに抑えることができる。

【０１１７】さらに、隣接する各サンプリングスイッチ１９～２３は、バッファ回路６２～６６によって電気的な繋がりが疎になっているので、例えば外部からの光の照射によってサンプリングトランジスタ１９～２３のＯＦＦ抵抗が低下する場合においても、同一データ信号線１２に繋がる相互に隣接したサンプリングスイッチ１９～２３のＯＦＦ抵抗を介して、各サンプリングトランジスタ２４～２７に保持したデータ信号がクロストークするのを防止することができる。

【０１１８】一般に、ソースドライバ内には、データ信号線以外にも信号配線が複数本配置されているため、各信号配線がその配線容量を介したり、交差する配線の交差部分の容量やその他の寄生容量を介して、ノイズが乗ることによりサンプリングデータの精度が低下することになる。

【０１１９】ところが、本実施例のソースドライバ６１では、データ信号線１２一本のみであるので、データ信号線１２に乗るノイズの影響を低減することができる。

【０１２０】このように、隣接するサンプリングトランジスタ同士において、互いにＯＮ・ＯＦＦ時の影響を受けず、常に正確なデータ信号をソースバスライン信号としてソースバスライン５に供給することができる。

【０１２１】したがって、本実施例のＬＣＤは、データ信号線１２に対する負荷によるデータ信号波形のなまり、或いは隣接するトランジスタが同時にＯＮ状態となることによるデータ信号のノイズが原因のゴースト現象の低減、及び、サンプリングトランジスタのＯＦＦ特性の不足および低下によって生じるクロストークによる表示品位の低下を抑えた高解像度の表示を可能としている。

【０１２２】尚、本実施例では、ソースドライバ６１におけるサンプリング方式は、表示部１側でデータ信号としての画像データを保持するパネルサンプルホールド方式となっているがソースドライバ側で画像データを保持するドライバサンプルホールド方式のソースドライバにおいても同様に適用でき、同様の効果を得ることができる。この場合、ドライバサンプルホールド方式のソースドライバを使用することで、ソースドライバに繋がる絵素部では画像データの書込時間を十分にとることができる。

【０１２３】〔実施例６〕本発明のさらに他の実施例について図９に基づいて説明すれば、以下の通りである。尚、本実施例では、上記実施例５のソースドライバ６１に適用した構成をＬＣＤの表示部１での信号入力に適用した場合について説明する。

【０１２４】本実施例に係るＬＣＤは、図９に示すように、ソースドライバ６１に接続されたソースバスライン５…にバッファ回路６７…が接続され、このバッファ回路６７…の出力側に、絵素トランジスタ７のソース端子が接続されている。図９において、左右方向を行方向、上下方向を列方向とする。

【０１２５】つまり、同一のソースバスライン５に列方向に複数の絵素トランジスタ７が接続されているが、バッファ回路６７によってそれぞれの絵素トランジスタ７は互いに電気的に疎となるようにソースバスライン５に繋がっている。

【０１２６】尚、本実施例におけるＬＣＤの動作は、ソースバスライン信号がバッファ回路６７…を介して表示部１の絵素トランジスタ７に供給される他は、上記実施例５のソースドライバ４１の動作と同様である。

【０１２７】上記の構成において、ソースバスライン５からのソースバスライン信号が、同一ソースバスライン５上に接続された複数の絵素トランジスタ７…にそれぞれバッファ回路６７…を介して供給されるので、各ソースバスライン信号はお互いに影響を及ぼさない。したが

って、隣接する絵素部４…は、互いに絵素トランジスタ７がＯＮ状態となったときに生じるノイズの影響を受けず、しかも絵素トランジスタのＯＦＦ抵抗によるクロストークを抑えた高解像度の画像を得ることができる。

【０１２８】また、上記ソースドライバ６１を、上記実施例１の図１に示すように構成しても良い。この場合、なまりや遅延の無いデータ信号を表示部１に供給でき、しかも、表示部１においても、データ信号をなまりや遅延なく書き込めるので、さらに表示品位の向上したＬＣＤを提供することができる。

【０１２９】〔実施例７〕本発明のさらに他の実施例について図１０に基づいて説明すれば、以下の通りである。尚、説明の便宜上、前記の各実施例と同一機能を有する部材には、同一番号を付記し、その説明を省略する。

【０１３０】本実施例に係るＬＣＤは、図１０に示すように、複数の絵素部４…を有する表示部１と、上記絵素部４を駆動する駆動回路としてのソースドライバ７１およびゲートドライバ３とで構成されている。図１０において、左右方向を行方向、上下方向を列方向とする。

【０１３１】上記ソースドライバ７１は、ソースシフトレジスタ１０と、このソースシフトレジスタ１０からの出力の論理積を得るためのＡＮＤ回路７２・７２と、異なる極性のデータ信号（映像信号）を供給するためのデータ信号線７３・７４と、ソースシフトレジスタ１０からの出力に応じてデータ信号をサンプリングするサンプルホールド回路１１とで構成されている。

【０１３２】上記ＡＮＤ回路７２・７２には、ソースシフトレジスタ１０の次の桁の出力が反転して入力されるようにインバータ７２ａ・７２ａが接続されている。即ち、ＡＮＤ回路７２は、ソースシフトレジスタ１０の出力と次の桁のＡＮＤ回路７２に入力される出力をインバータ７２ａにて反転された反転信号との論理積を得て、この論理積をサンプリングパルスとしてサンプルホールド回路１１に出力するようになっている。

【０１３３】また、データ信号線７３・７４には、お互いに極性が異なり、フィールド毎に極性の反転するデータ信号が、図示しないデータ信号生成回路からバッファ回路７５・７６を介して供給されている。

【０１３４】上記データ信号線７３は、サンプルホールド回路１１のサンプリングスイッチ１９・２１のソース端子に接続され、データ信号線７４は、サンプルホールド回路１１のサンプリングスイッチ２０・２２のソース端子に接続されている。

【０１３５】したがって、上記サンプリングスイッチ１９・２０のソース端子には、同一のＡＮＤ回路７２からサンプリングパルスが供給され、また、上記サンプリングスイッチ２１・２２のソース端子には、同一のＡＮＤ回路７２からサンプリングパルスが供給されるようになっている。尚、ＡＮＤ回路７２は、ソースシフトレジスタ１０からの出力を時間的に重ならないようなパルス幅にしてサンプルホールド回路１１に供給するようになっている。

【０１３６】ここで、上記構成のソースドライバ７１の動作について以下に説明する。上記のソースシフトレジスタ１０に入力されたＳＰは、ソースシフトレジスタ１０に入力される駆動クロックＣＫ、／ＣＫに応じて順次シフトして出力されていく。そして、出力された各桁のパルスは、ＡＮＤ回路７２に入力される。次いで、ＡＮＤ回路７２にて、ソースシフトレジスタ１０の出力ＳＲｉと次の桁の出力ＳＲｉ＋１の反転信号とで論理積が求められ、この論理積の値をサンプリングパルスとしてサンプルホールド回路１１に出力される。

【０１３７】上記ＡＮＤ回路７２からの出力は、サンプルホールド回路１１におけるそれぞれのサンプリングスイッチ１９～２３のゲート端子にサンプリングパルスとして順次入力される。

【０１３８】一方、データ信号線１２からのデータ信号は、バッファ回路６２～６６を介してサンプリングスイッチ１９～２３のソース端子に入力される。

【０１３９】したがって、上記ソースシフトレジスタ１０から出力されたサンプリングパルスがサンプリングスイッチ１９～２３のゲート端子に入力されると、データ信号線１２から出力されたデータ信号が各サンプリングコンデンサ２４～２７に保持される。

【０１４０】保持されたデータ信号は、絵素部４…の左右両側に配したソースバスライン５からバッファ回路７７を介してゲートバスライン６…の１本おきに、交互に接続されている絵素トランジスタ７…に入力される。

【０１４１】上記構成のソースドライバ６１によれば、ソースシフトレジスタ１０からの出力は、ＡＮＤ回路７２…を介してサンプルホールド回路１１に入力されるようになるので、サンプリングパルスの幅が小さくなり、互いに時間的な重なりを持たない関係となっている。このため、各データ信号線７３・７４からみた負荷は、従来に比べて小さくなっているので、データ信号のなまりを従来よりも小さくすることができる。

【０１４２】また、ゲートドライバ３は、ゲートシフトレジスタ３ａと、このゲートシフトレジスタ３ａの出力から論理積を得るためのＡＮＤ回路８１…とで構成されている。

【０１４３】上記ＡＮＤ回路８１…は、ゲートシフトレジスタ３ａの次の行の出力が反転して入力されるようにインバータ８１ａ…が接続されている。即ち、ＡＮＤ回路８１は、ゲートシフトレジスタ３ａの出力と次の行のＡＮＤ回路８１に入力される出力をインバータ８１ａにて反転して得られる反転信号との論理積を得て、この論理積をゲート信号（走査信号）としてゲートバスライン６…に供給するようになっている。尚、ＡＮＤ回路８１は、ゲートシフトレジスタ３ａからの出力を時間的に重

ならないようなパルス幅にして絵素トランジスタ７…に供給するようになっている。

【０１４４】したがって、ゲートドライバ３から表示部１の各絵素トランジスタ７…に入力されるゲート信号は、ゲートシフトレジスタ３ａの出力から得た論理積であるので、各ゲート信号はお互いに時間的な重なりを持たない関係となる。このため、列方向に隣接する絵素トランジスタ７…が同時にＯＮ状態となることによるノイズの影響を防止できる。

【０１４５】また、列方向に隣接する絵素トランジスタ７…は、異なるソースバスライン５…に接続されていることで、ゲートバスライン信号Ｇｉと次の行のゲートバスライン信号Ｇｉ＋１とが信号の遅延やなまりによって同時にＯＮ状態となる期間があったとしても、列方向に隣接する絵素トランジスタ７…が同時にＯＮ状態となることで生じるノイズにより絵素容量８…および付加容量９…にサンプリングされるソースバスライン信号の精度が低下するのを防止している。

【０１４６】一般に、ソースバスライン５に印加される信号は、液晶にＤＣ電圧が印加されることによる信頼性の低下を防止するため、印加する電圧極性を１走査期間毎に反転させている。この場合、列方向に隣接する絵素トランジスタ７…が同時にＯＮ状態となる期間が存在すれば、絵素容量８…にサンプリングされるソースバスラインデータの精度の低下をさらに大きくするという不具合が生じることになる。

【０１４７】しかしながら、本実施例では、列方向に隣接する絵素トランジスタ７…は、それぞれ絵素部４…の両側に設けられた異なるソースバスライン５…を介して、ソースバスライン信号が供給されるようになっているので、列方向に隣接する絵素トランジスタ７…が同時にＯＮ状態となる期間を無くすことができ、この結果、絵素容量８…にサンプリングされるソースバスラインデータの精度の低下を防止できる。

【０１４８】また、一般に、１走査期間毎にソースバスライン５に印加する電圧の極性を反転する場合、ある走査期間に充電したソースバスライン５を、次の走査期間には逆の極性に充電しなくてはならないため、ソースバスライン５…を駆動するために大きな駆動力が必要となる。この結果、ソースバスライン５…の駆動に必要とされる電力によって、ソースドライバ全体の消費電力が増大するという問題が生じている。

【０１４９】ところが、本実施例では、予め極性の異なるデータ信号が、ソースバスライン５…に対して交互に供給されているので、同一極性のデータ信号が、絵素部４の両側に配されたソースバスライン５…に供給すればよいので、１走査期間毎にソースバスライン５に供給した極性と逆極性の信号を供給する必要がなくなる。これによって、ソースバスライン５…の駆動に必要とされる電力を低減することができるので、ソースドライバ６１全体の消費電力を低減させることができる。

【０１５０】尚、本実施例では、各絵素部４…の両側に２本のソースバスライン５…を配しているが、これに限定されるものではなく、例えば絵素部４の片側に２本のソースバスライン５・５を配しても良い。しかしながら、この場合、ゲートバスライン６…の１本おきにソースバスライン５を交差してソースバスライン５と絵素トランジスタ７とが接続される形となり、交差部分の寄生容量等からのノイズの影響を受けることになり、その効果は、ソースバスライン５・５を絵素部４の両側に配した場合ほどの効果を奏することができない。

【０１５１】〔実施例８〕本発明のさらに他の実施例について図１１に基づいて説明すれば、以下の通りである。尚、本実施例のＬＣＤは、前記の各実施例と表示部、ゲートドライバを同一の構成とし、ソースドライバについて説明する。

【０１５２】本実施例に係るＬＣＤのソースドライバは、図１１に示すように、複数の映像信号等のデータ信号を供給するためのデータ信号線８２…と、それぞれのデータ信号線８２…にはサンプルホールド回路８５のＴＦＴ等のトランジスタからなるサンプリングスイッチ８６…のソース端子が接続されている。

【０１５３】上記サンプリングスイッチ８６…のゲート端子には、上記データ信号のサンプリングのタイミングを制御するサンプリングタイミング制御回路８４が接続されている。

【０１５４】データ信号線８２は、バッファ回路８３を介して図示しないデータ信号生成回路に接続されている。このデータ信号線８２は、１本ずつサンプリングスイッチ８６に接続されているようになっている。これにより、データ信号線８２…における負荷は、一つのサンプリングスイッチ８６のみとなるので、一本のデータ信号線８２に複数のサンプリングスイッチ８６…が接続される場合よりも分断される前のデータ信号線のインピーダンスを下げることができる。

【０１５５】つまり、上記データ信号生成回路から出力されるデータ信号を表示の水平方向で複数に分断することで、分断される前のデータ信号線のインピーダンス、特に容量成分を１／Ｎ（Ｎ：分断数）程度に下げることができる。これにより、データ信号線の時定数を大幅に改善することができるので、クロストークの発生を抑制することができる。

【０１５６】尚、表示部１へのデータ信号の入力をサンプルホールド回路８５近傍より、表示部１に入力することができるので、これによっても、時定数を大幅に改善することができる。

【０１５７】本実施例は、前記した各実施例においても適用することができ、それによって、さらにクロストークの発生の少ない解像度の高い表示装置にすることができる。

【０１５８】以上、上記した実施例１～８では、それぞれ基本的な構成を示しており、回路構成の変更、例えばサンプリングパルス生成回路が前述のシフトレジスタによらず、所謂デコーダ方式の回路で構成された場合に変更しても良い。

【０１５９】また、例えば、サンプリングトランジスタに繋がるサンプリングコンデンサの容量が小さい場合には、同一のデータ信号をバッファ回路を介してシフトレジスタの系列毎に供給することも可能である。

【０１６０】さらに、上記した実施例１～８において、サンプリング回路を含む駆動回路としてのソースドライバおよびゲートドライバと、画像表示部としての絵素部等からなる表示部とを同一基板上にモノリシックに形成しても良い。この場合、大画面化に伴う画素トランジスタの駆動力向上や、駆動ＩＣの実装コストの低減等を図ることができる。

【０１６１】

【発明の効果】請求項１の発明の表示装置は、以上のように、データ信号がそれぞれ供給される複数のデータ信号線と、上記複数のデータ信号線から供給されるデータ信号をそれぞれサンプリングする複数のサンプリング回路と、上記複数のサンプリング回路にそれぞれ接続される複数のデータバスラインと、上記複数のデータバスラインに接続されると共に、マトリクス状に配された複数の絵素部と、上記サンプリング回路を含み、上記データバスラインを駆動する駆動回路とを備え、上記複数のデータ信号線の少なくとも２本は、同一データ信号が供給されると共に、それぞれが異なるバッファ回路を介して異なるサンプリング回路に接続されている構成である。

【０１６２】これにより、隣接するサンプリング回路では、互いにＯＮ・ＯＦＦ時の影響を受けず、常に正確なデータ信号をサンプリングすることでゴースト現象を低減できる。また、絵素部およびサンプリング回路部のトランジスタのＯＦＦ抵抗によるクロストークを低減させることができる。

【０１６３】したがって、ゴースト及びクロストークによる表示品位の低下を抑えた高解像度の表示を可能とすることができるという効果を奏する。

【０１６４】請求項２の発明の表示装置は、以上のように、請求項１記載の表示装置において、複数のサンプリング回路のうち、サンプリングのタイミングが同期するサンプリング回路は、それぞれ異なるデータ信号線に接続されると共に、それぞれのサンプリング回路のＯＮ期間が時間的に重なりを持たない構成である。

【０１６５】これにより、請求項１の効果に加えて、サンプリング回路がＯＦＦ状態となる瞬間に他のサンプリング回路がＯＮ状態となることにより生じるノイズの低減を図ることができるという効果を奏する。

【０１６６】請求項３の発明の表示装置は、以上のように、請求項１または２記載の表示装置において、バッファ回路は、サンプリング回路と同一の基板上に形成されている構成である。

【０１６７】これにより、バッファ回路とサンプリング回路とを接続するフレキシブル基板等による接触抵抗にかかわるデータ信号の劣化を抑制することができる。また、バッファ回路とサンプリング回路とを接続するための接続端子の増加を抑制でき、実装に伴う信頼性を向上させることができるという効果を奏する。

【０１６８】請求項４の発明の表示装置は、以上のように、データ信号がそれぞれ供給される複数のデータ信号線と、上記複数のデータ信号線から供給されるデータ信号をそれぞれサンプリングする複数のサンプリング回路と、上記複数のサンプリング回路にそれぞれ接続される複数のデータバスラインと、上記複数のデータバスラインに接続されると共に、マトリクス状に配された複数の絵素部と、上記サンプリング回路を含み、上記データバスラインを駆動する駆動回路とを備え、上記データ信号線は、表示の水平方向で複数に分断されると共に、分断された各々の信号線は、それぞれ異なるバッファ回路を介してサンプリング回路に接続されている構成である。

【０１６９】これにより、データ信号線の抵抗および容量を低減することができるので、よりデータ信号線におけるデータ信号の劣化を低減させることができると共に、サンプリング時のノイズの低減を図ることができるという効果を奏する。

【０１７０】請求項５の発明の表示装置は、以上のように、データ信号がそれぞれ供給される複数のデータ信号線と、上記複数のデータ信号線から供給されるデータ信号をそれぞれサンプリングする複数のサンプリング回路と、上記複数のサンプリング回路にそれぞれ接続される複数のデータバスラインと、上記複数のデータバスラインに接続されると共に、マトリクス状に配された複数の絵素部と、上記サンプリング回路を含み、上記データバスラインを駆動する駆動回路とを備え、上記複数の絵素部のうち、列方向に隣接する複数の絵素部には、それぞれ異なるデータバスラインが接続されると共に、これらデータバスラインには、バッファ回路を介して同一のサンプリング回路が接続されている構成である。

【０１７１】これにより、列方向に隣接する絵素部の干渉を抑えることができるので、絵素部同士のクロストークを低減することができ、この結果、表示品位を向上させることができるという効果を奏する。

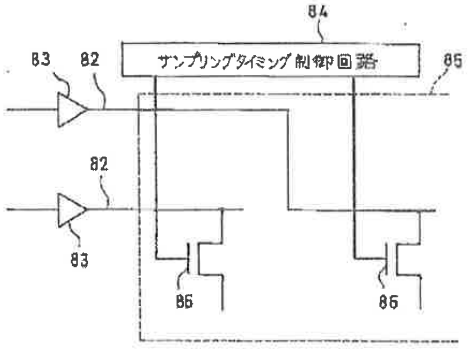
【０１７２】請求項６の発明の表示装置は、以上のように、請求項１、２、３、４または５記載の表示装置において、駆動回路と、複数の絵素部からなる画像表示部とが同一基板上にモノリシックに形成されている構成である。

【０１７３】これにより、大画面化に伴う画素トランジスタの駆動力向上や、駆動ＩＣの実装コストの低減等を図ることができるという効果を奏する。

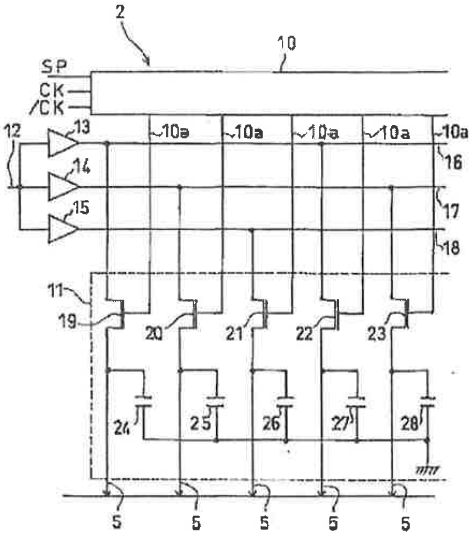
【図面の簡単な説明】
【図１】本発明の一実施例のＬＣＤのソースドライバの概略構成ブロック図である。
【図２】図１に示すソースドライバを備えたＬＣＤの概略構成ブロック図である。
【図３】図１に示すソースドライバの動作タイミングチャートである。
【図４】本発明の他の実施例のＬＣＤの概略構成ブロック図である。
【図５】本発明のさらに他の実施例のＬＣＤのソースドライバの概略構成ブロック図である。
【図６】図５に示すソースドライバの動作タイミングチャート図である。
【図７】本発明のさらに他の実施例のＬＣＤの概略構成ブロック図である。
【図８】本発明のさらに他の実施例のＬＣＤのソースドライバの概略構成ブロック図である。
【図９】本発明のさらに他の実施例のＬＣＤの概略構成ブロック図である。
【図１０】本発明のさらに他の実施例のＬＣＤの概略構成ブロック図である。
【図１１】本発明のさらに他の実施例のＬＣＤのソースドライバの概略構成ブロック図である。
【図１２】従来のＬＣＤの概略構成ブロック図である。
【図１３】図１２に示すＬＣＤに備えられたソースドライバの概略構成ブロック図である。
【図１４】従来の他のソースドライバの概略構成ブロック図である。
【図１５】図１４に示すソースドライバの動作タイミングチャートである。
【符号の説明】

１	表示部（画像表示部）
２	ソースドライバ（駆動回路）
３	ゲートドライバ（駆動回路）
４	絵素部
５	ソースバスライン（駆動回路）
６	ゲートバスライン（駆動回路）
１０	ソースシフトレジスタ
１１	サンプルホールド回路
１２	データ信号線
１３～１５	バッファ回路
１６～１８	データ信号線
１９～２３	サンプリングスイッチ（サンプリング回路）
２４～２８	サンプリングコンデンサ（サンプリング回路）
４１	ソースドライバ（駆動回路）
５１	データ信号線
５２・５３	バッファ回路
５４・５５	データ信号線
６１	ソースドライバ（駆動回路）
６２～６６	バッファ回路
５４・５５	データ信号線
７３・７４	データ信号線
７５～８０	バッファ回路

【図１１】



【図1】



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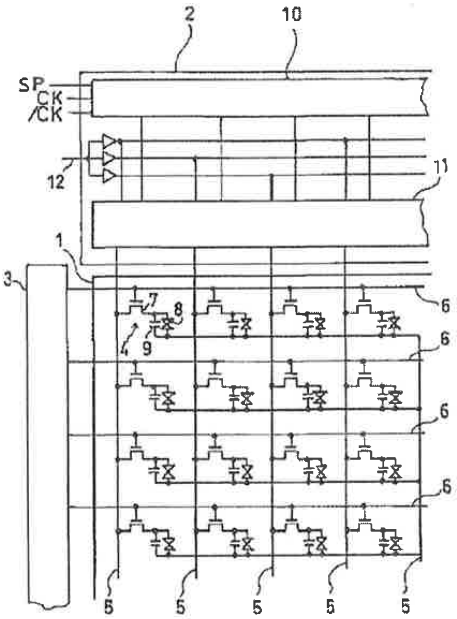

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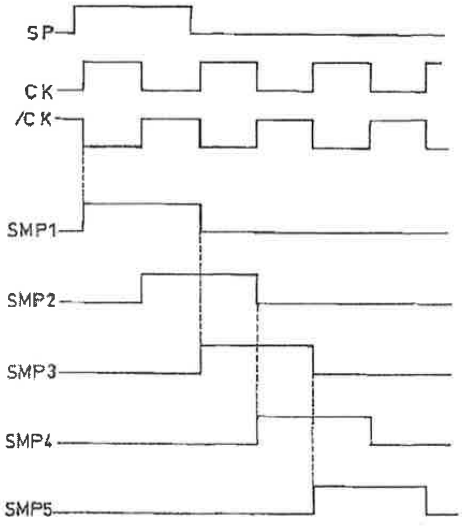

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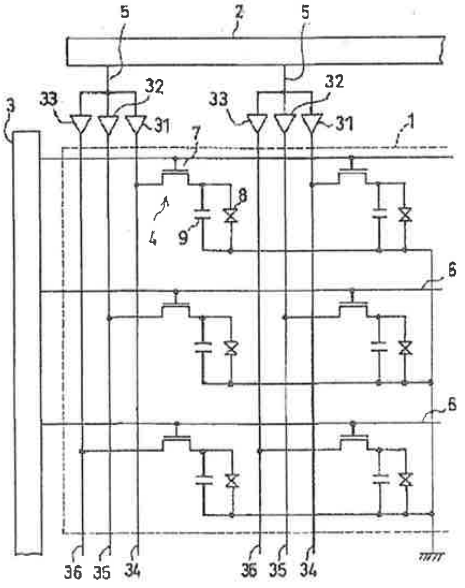

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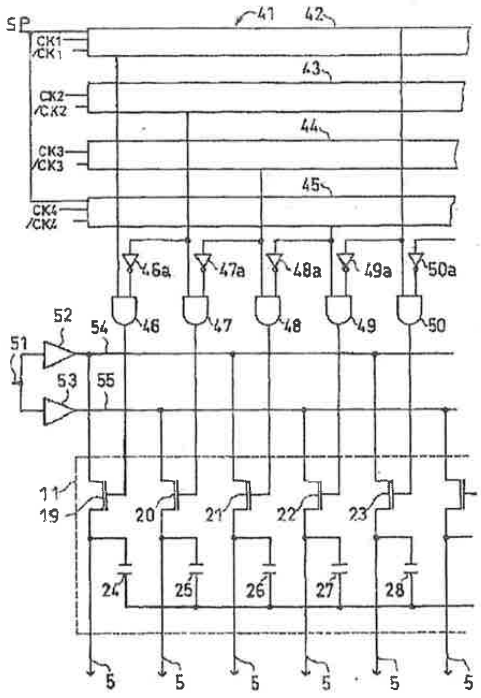

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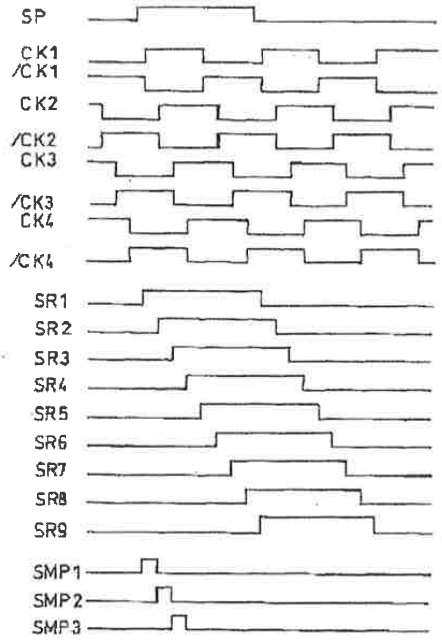

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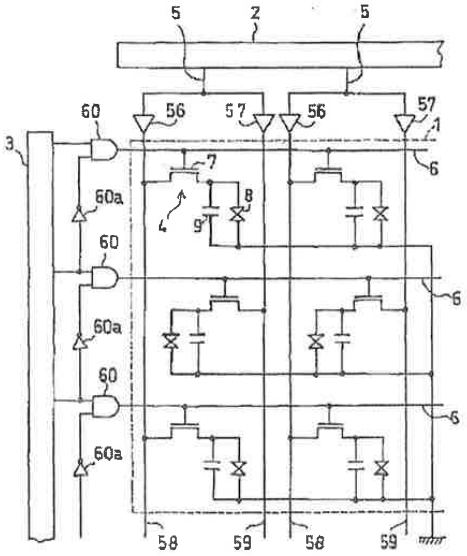
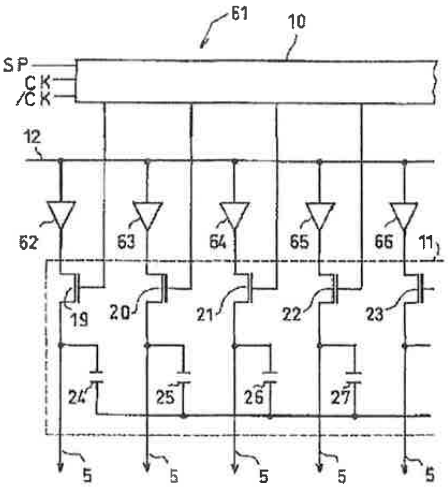


【図８】



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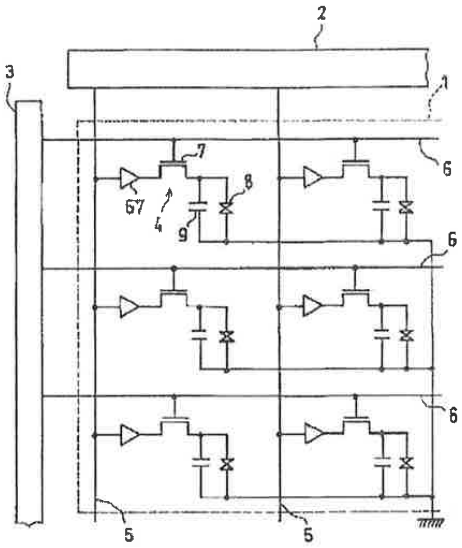
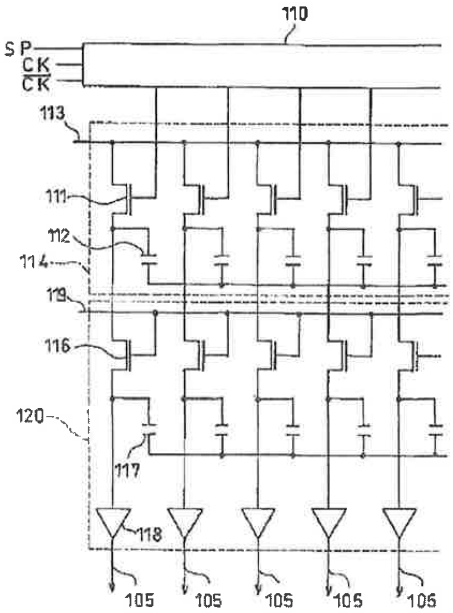
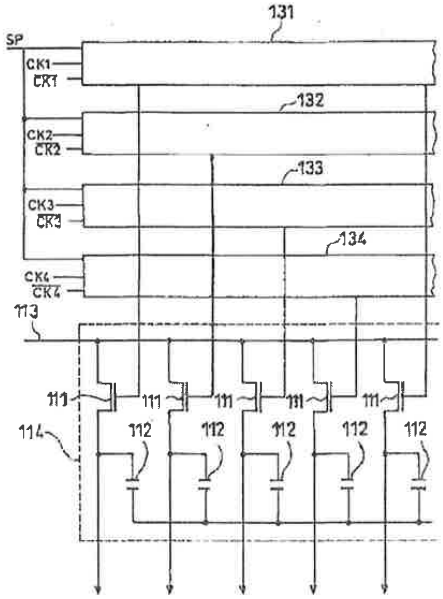


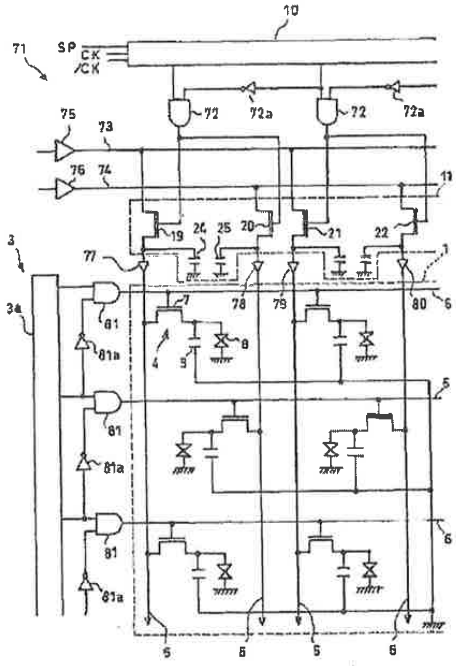
【図１３】



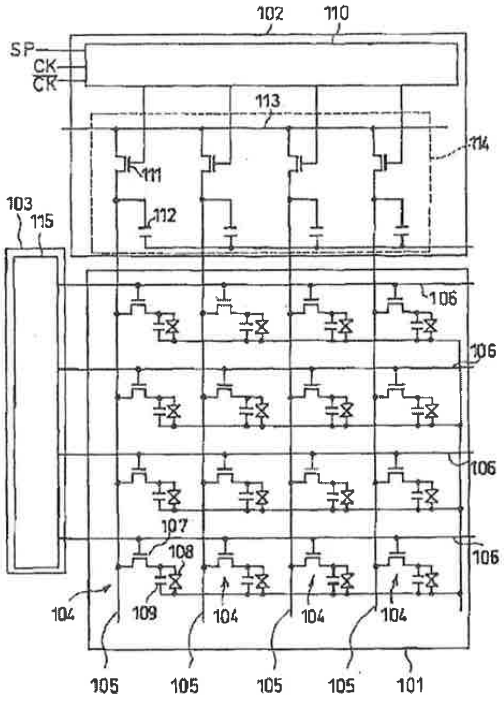
【図１４】



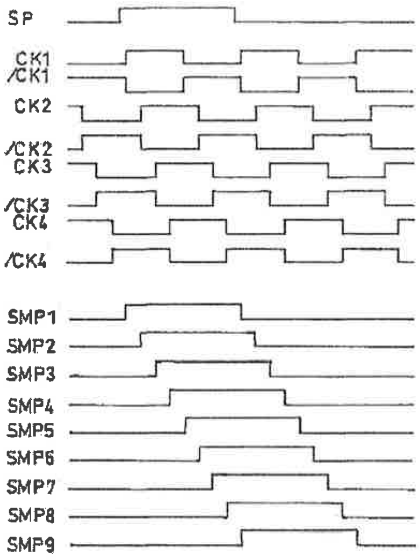
【図１０】



【図１２】



【図15】



UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SHARP CORPORATION, SHARP ELECTRONICS CORPORATION, and SHARP ELECTRONICS MANUFACTURING COMPANY OF AMERICA, INC.,
Petitioners

v.

SURPASS TECH INNOVATION LLC,
Patent Owner

Case IPR2015-_____
Patent No. 7,420,550

DECLARATION OF MICHAEL J. MARENTIC IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,420,550

1. I, Michael J. Marentic, make this declaration in connection with the Petition for *Inter Partes* Review submitted by Sharp Corporation, Sharp Electronics Corporation, and Sharp Electronics Manufacturing Company of America, Inc. (collectively "Petitioners" or "Sharp") for review of Claims 1 through 5 of U.S. Patent No. 7,420,550 to Yuh-Ren et al. ("the '550 Patent"), which is assigned to Surpass Tech Innovation LLC ("Patent Owner" or "Surpass").

2. Throughout this declaration, I refer to exhibit numbers that correspond to the exhibits to the Petition for *Inter Partes* Review for which I provide this declaration.

Scope of My Assignment

3. I have been requested by counsel for Sharp to study the '550 Patent, including its claims and prosecution history, as well as the references specifically referred to in this declaration. I have also been requested by counsel for Sharp to provide my expert opinion regarding the invalidity of Claims 1-5 of the '550 Patent. I further expect to offer an additional declaration in response to any declaration submitted by any expert for the Patent Owner.

Summary of My Opinions

4. It is my opinion that Claims 1-3 of the '550 Patent are invalid as anticipated under 35 U.S.C.§ 102(b) and Claims 4-5 are obvious to a person of ordinary skill in the art under 35 U.S.C. §103(a). Moreover, it is my opinion that in addition to being anticipated, Claims 1-3 are also rendered obvious over prior art.

5. Specifically, I believe that the following are grounds to find Claims 1-5 of the '550 Patent invalid:

a. Claims 1-3 are invalid under 35 U.S.C. § 102(b) as anticipated by Japanese Patent Application Publication No. H08-305322 (Ex. 1002, "the Sharp Reference").

b. Claims 1-3 and 5 are also invalid under 35 U.S.C. § 103(a) as obvious over the Sharp Reference.

c. Claims 1-5 are also invalid under 35 U.S.C. § 103(a) as obvious over the Sharp Reference in view of U.S. Patent No. 6,407,795 to Kamizono, et al. (Ex. 1004, "Kamizono").

d. Claims 1-5 are also invalid under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 6,081,250 to Shimada et al. (Ex. 1003, "Shimada") in view of Kamizono.

Summary of My Professional Background and Qualifications

6. Exhibit 1008 is my *curriculum vitae* which sets forth my professional background and qualifications. A list of publications that I have authored or co-authored is included.

7. I have many years of experience in the flat panel display industry. I first became involved in the flat panel display industry in 1973, when I began working at the University of Illinois Coordinated Science Laboratories where the AC Plasma Display Panel

("PDP") was invented. During my studies at the University, I was employed as an intern working in the area of plasma display construction and gas discharge physics characterization. I received a B.S. degree in Engineering Physics from the University of Illinois.

8. Upon entering graduate school, I continued my work on the characterization of the gas discharge in the pixels. I received an M.S. degree in Electrical Engineering from the University of Illinois, and wrote my master's thesis on measuring the electron density in an AC PDP.

9. One of my engineering positions was with Interstate Electronics Corporation (IEC) as a design electrical engineer. IEC designed drive electronics, mechanically packaged the display modules, and incorporated them into terminals for harsh, military environments. I designed several distinct versions of drive electronics for PDPs, including one using packaged silicon integrated circuits on flexible circuits, or "chip-on-flex." During this time, I was awarded several patents relating to PDP technologies. I also investigated LCDs and thin film electroluminescent displays for incorporation into military applications.

10. I later formed Plasma Displays, Inc., a single proprietorship consulting corporation. I worked for several clients, one being Bell Laboratories and AT&T at their joint Reading, Pennsylvania facility. This facility was where the original picture phone was developed, the first commercial light emitting diodes ("LEDs") were manufactured, and

AT&T's PDPs were developed and manufactured. I worked on PDP drive electronic design, driver-to-panel interconnect reliability, driver circuit characterization, and yield improvement.

11. I was a founder and Vice President of Plasmaco, a company that acquired IBM's PDP production line in New York. Plasmaco manufactured several types of PDPs, including VGA panels with 640x480 pixels for early notebook computers. Such a panel had 5 driver ICs with 32 outputs per driver for 640 data lines. I also developed larger sized VGA panels with 1280x1024 pixels. Because of the increase in size, we used the same type of driver IC chips but doubled the number of driver ICs (i.e., using 10 driver ICs) in the display. When changing the panel design to increase the size of the panel and/or the number of pixels, it was a common practice to keep the same type of driver IC as the smaller panel, but it was necessary to increase the number of driver ICs to accommodate the added pixels in the larger display.

12. While at Plasmaco, I also developed and manufactured driver chip-on-glass ("COG") technology that passed extreme militarized environmental testing specifications. COG technology put electrode driver integrated circuits onto the glass edges of the PDP. The benefits of using COG technology were that it reduced the physical size and weight of a notebook computer display and increased the operational reliability of the display.

13. At Science Applications International Corporation, I worked on efficient backlights for LCDs, some for direct viewing in sunlight. Commercially available LCDs were

disassembled and repackaged with these backlights. The finished displays were used in cockpit avionics, medical, banking, and FAA towers.

14. At Hitachi, from 1995 to 1999, I managed a technology center that developed technologies relating to the interface between the motherboard and the LCD driver chips for flat panel monitors and notebook displays. I reported directly to the LCD design and manufacturing center in Japan. I had access to future LCD technical details and specifications, and facilitated technology transfer between Silicon Valley firms and Japan management. The Video Electronics Standards Association ("VESA") writes and publishes video standards for the electrical interfacing for displays. I was the chairman of the VESA flat panel display committee, a member of the board of directors, and later the president of the board of directors.

15. While at Philips, from 1999 to 2001, I managed a group of engineers that designed electronics for flat panel displays. My group designed interface timing ICs and video processing circuit boards for monitors and televisions utilizing LCDs. My group also worked with an IC design firm to develop the design of source and gate driver ICs for enhanced performance LCDs having various sizes. The enhanced performance LCDs were developed to provide high brightness and used multiple driver ICs, as well as the COG technology.

16. Philips invested in a tiled LCD display company, and I participated in the technology development using Philips panels. My group designed circuits and assisted with their incorporation into commercial products within Philips' worldwide subsidiaries.

17. Philips purchased the LCD factory of the Korean company LG, and later formed a joint venture called LG-Philips LCD. I was a member of the group of technical advisors that performed the due diligence for Philips for the purchase.

18. At Alien Technology, I was a member of the integrated design team that produced custom drivers made for cholesteric LCD displays, organic LEDs, and polymer dispersed LCDs. My responsibilities were IC product definition for the drivers and system architecture. Driver ICs were fabricated at silicon foundries and formed into small die for mass assembly utilizing Alien's fluidic assembly onto flexible, very low cost displays. Since Alien's products were very small sized, low cost LCDs, they typically involved only a single source driver and a single gate driver, whereas the larger sized LCD panels that I worked on while at Hitachi and Philips had multiple source and gate drivers.

19. I am the named inventor or co-inventor on three U.S. patents in the PDP field.

Materials Considered

20. In forming my opinions, I reviewed the following documents referenced by their exhibit number in the Petition for *Inter Partes* Review of the '550 Patent:

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 7,420,550 to Shen et al. ("'550 Patent")
1002	Japanese Patent Application Publication No. H08-305322 and Certified English Translation Thereof ("Sharp Reference")
1003	U.S. Patent No. 6,081,250 to Shimada et al. ("Shimada")
1004	U.S. Patent No. 6,407,795 to Kamizono et al. ("Kamizono")
1005	Prosecution History of U.S. Appl. No. 10/929,473
1006	U.S. Patent No. 5,805,128 to Kim et al. ("Kim")
1009	U.S. Patent Application Publication No. US 2003/0048249 A1 to Sekido et al. ("Sekido")

21. I also base this declaration on my knowledge from my 30 years of experience working on liquid crystal display (LCD) and related technologies.

22. I reserve the right to amend or supplement this declaration based upon any reports by any expert(s) for the Patent Owner, or any new documents and/or other information that becomes available.

Compensation

23. I am being compensated at my consulting rate of $250 per hour for my time spent in connection with this case. I am being separately reimbursed for any out-of-pocket

expenses. No part of my compensation is dependent upon the outcome of this proceeding or the nature of the opinions that I express.

Legal Standards

24. To render my invalidity analysis, I have been informed about the legal standards for patent invalidity in *inter partes* review proceedings before the Patent Trial and Appeal Board.

25. Specifically, I understand that the petitioner must prove patent invalidity by a "preponderance of the evidence," that there is no "presumption of validity" in *inter partes* review proceedings, and that claims are to be given their "broadest reasonable" construction in light of the specification as would be read by a person of ordinary skill in the art.

26. I also understand that a patent claim may be invalidated as anticipated if a single prior art reference discloses, either expressly or inherently, each and every element of the patent claim.

27. I also understand that a patent claim may be invalidated by one or more references, either alone or in combination, as being "obvious" to a person of ordinary skill in the art at the time the invention was made.

28. I understand that one way of demonstrating obviousness in the situation where a prior art reference discloses a single element but the claim requires multiple elements is to demonstrate that there are no new and unexpected results from increasing the number of such elements.

29. I further understand that an additional way of demonstrating obviousness is to demonstrate that one or more items of prior art either alone or in combination, contain all of the elements of a claim.

30. It is my understanding that in considering the issue of obviousness, I should consider what a person of ordinary skill in the pertinent art would have known at the time of the invention, as well as what such a person would have reasonably expected to have been able to do in view of that knowledge.

31. I understand that in analyzing the issue of obviousness, I should consider and determine: (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; and (3) the level of ordinary skill in the pertinent art.

32. I further understand that any of the following may provide a "reason" for combining elements known in the prior art: (a) a need or problem known in the field at the time of invention and addressed by the patent; (b) an obvious use of familiar elements beyond their primary purposes; (c) a design need or market pressure to solve a problem; (d) a simple substitution of one known element for another that would provide predictable results; (e) the use of known techniques to improve similar methods or products in the same way; or (f) some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

33. I also understand that claims may be invalid if they are directed to obvious design choices. Specifically, I understand that a patent claim that simply arranges old elements with each performing the same function it had been known to perform is not patentable. The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.

34. I also understand that certain "secondary considerations" of non-obviousness may be considered, to the extent that they exist. It is my understanding that such secondary considerations include, among others: (a) commercial success; (b) long felt but unsolved needs; and (c) the failure of others. I understand that there must be some connection to the secondary considerations and the claimed invention. I reserve my right to address any evidence or opinions the patent owner may submit on this issue.

THE '550 PATENT

35. I understand that the application leading to the '550 Patent was U.S. Patent Application No. 10/929,473, which was filed on August 31, 2004. For the purposes of my analysis, I assume that the time of the purported invention was August 31, 2004.

36. The '550 Patent relates to an active matrix liquid crystal display (LCD) device and driving circuit for the LCD device. In particular, the '550 Patent describes a specific way of connecting the gate and data lines to the thin film transistors (TFTs) driving pixels in an LCD panel.

LCD Panels and Driving Devices Were Known in the Prior Art

37. As acknowledged in the '550 Patent, active matrix LCD panels and the use of data and gate lines, or source and gate drivers for TFTs in LCD panels were all known in prior art. (Ex. 1001, '550 Patent, Col. 1:23-61, Figs. 1A-1B).

38. As shown below by multiple shaded blocks in annotated Figure 1A of the '550 Patent, the "Prior Art" driving circuit for LCD panels included multiple source drivers 11 and multiple gate drivers 12. (*Id.* at Fig. 1A). The source drivers 11 (purple boxes) provide image signals (i.e., video signals) to an LCD panel 10 through a plurality of data lines 111 (purple lines), while the gate drivers 12 (orange boxes) provide scanning signals (i.e., control signals) to the LCD panel 10 through a plurality of gate lines 121 (orange lines).

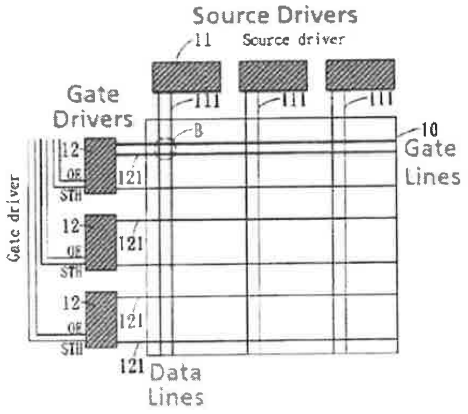


Fig. 1A (Prior Art)

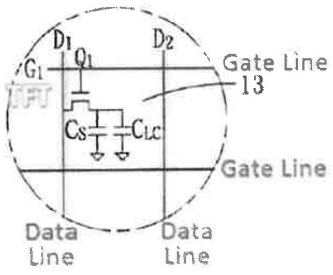


Fig. 1B (Prior Art)

39. As shown above in Figure 1A, prior art LCD panels included data lines 111 and gate lines 121 arranged in a matrix array.

40. According to the '550 Patent, the data lines 111 and gate lines 121 in the "Prior Art" shown in Figures 1A and 1B are "insulated with each other." (Ex. 1001, '550 Patent, Col. 1:45-47).

41. As shown above in Figure 1B, a pixel 13 in this prior art LCD panel is formed within each area enclosed by intersecting data lines (e.g., purple line D_1) and gate lines (e.g., orange line G_1).

42. As the '550 Patent acknowledges, each pixel 13 in prior art LCD panel included a thin film transistor Q_1 (TFT, highlighted in yellow), which is switched on and off by a control signal from the gate driver 12 through a gate line G_1.

43. The source of the TFT Q_1 receives the image signal sent from the source driver 11 through the data line D_1. An output voltage from the TFT Q_1 drives liquid crystal molecules corresponding to the pixel 13 to form an image. (*Id.* at Col. 1:45-57, Fig. 1B).

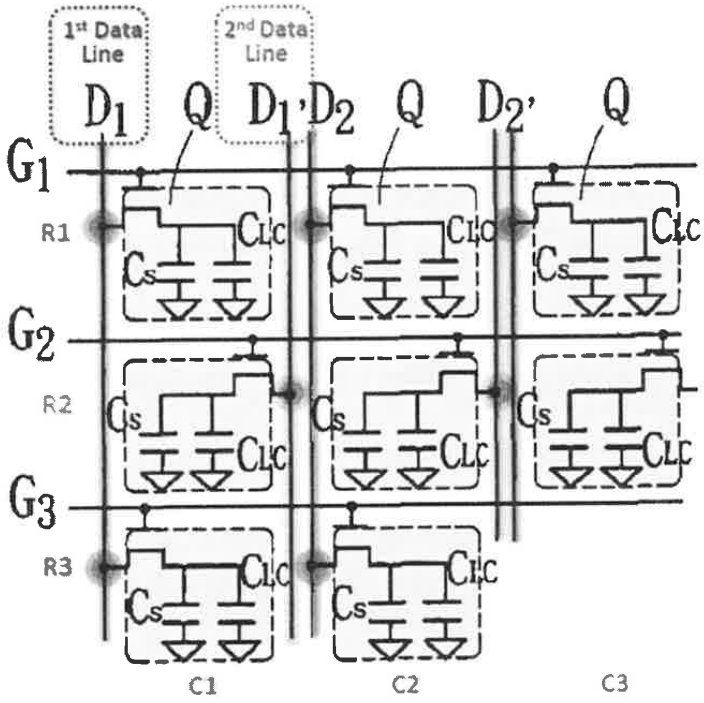
44. The time that an LCD needs to react to the driving voltage output by each TFT is called "response time," and the video quality of an LCD panel is dependent on this response time. In this regard, the video quality may be poor if the LCD response time is too long. (*Id.* at Cols. 1:62-2:41).

The Alleged Invention of the '550 Patent

45. According to the '550 Patent, its "chief object" is to provide an LCD driving circuit having a matrix structure in which the gate and data lines are connected to the TFTs in a specific way that allegedly increases "the response speed" of the LCD. (*Id.* at Col.

3:18-20, 35-40). This configuration is shown in, for example, Figure 4B, which is reproduced below.

'550 Patent Fig. 4B



46. As shown above in annotated Figure 4B, the driving device includes a matrix array formed from rows (R1-R3) and columns (C1-C3) of TFTs (Q). Each TFT in the matrix is associated with a pixel (represented by the dashed rectangles). The driving device further includes a certain number ("N") of gate lines G_i (i=1, 2, ... N), and a certain number ("M") of groups (e.g., pairs) of data lines D_j and $D_{j'}$ (j, j'=(1,1'), (2, 2'), ... (M, M')). For

example, as shown in Figure 4B above, the driving device has three gate lines, G_1, G_2, and G_3, and two groups of data lines ((D_1, $D_{1'}$) and (D_2, $D_{2'}$)).

47. As shown in Figures 4A, 5A, and 6A, the '550 Patent describes a source driver with a limit of 60 Hz but provides no further explanation or specification. Absent in the '550 Patent is the number of drive channels or outputs per source driver and matrix size. One would calculate the number of required driver ICs by dividing the horizontal pixel count by the number of drive channels per data driver. The driving device shown in Figure 4A uses 60 Hz source drivers; it doubles the normal calculated number of source drivers and mounts them on a single glass panel edge. The driving device shown in Figure 5A also uses 60 Hz source drivers; it again doubles the normal calculated number of data drivers, but mounts them on both the top and bottom edges of the panel with an interdigitated column connection. The driving device shown in Figure 6A uses 120 Hz or faster source drivers, mounted on one panel edge, and then adds dual switches to each output channel for driving the paired data electrodes.

48. The '550 Patent does not discuss the benefits or reasons for including a single source driver and a single gate driver on the one hand, and having a set of multiple source and gate drivers on the other hand.

49. Multiple source and gate drivers were commonly used in the prior art, particularly LCD panels as they increased in screen size. In fact, when I was in the LCD industry before the filing date of the '550 Patent, it was a common practice to change the

panel design to increase the size of the panel and/or the number of pixels by simply adding more driver ICs. For example, while the ***small***, low cost LCD panel (which had an equivalent pixel dimension of 7×4) that I worked on at Alien Technology had only a single source driver and a single gate driver, all the ***large sized*** LCD panels (which had pixel dimension of at least 800×600) that I worked on at Philips had multiple driver ICs.

50. Consistent with my experience, U.S. Patent Application Publication No. US 2003/0048249 A1 to Sekido et al. (Ex. 1009, "Sekido"), which was published on March 13, 2003, states that "in order to drive many gate bus lines and the source bus lines on the display circuit board, ***a plurality of the gate drivers and source drivers must*** be connected to the area around the liquid crystal display panel." (Par. [0006]) (emphasis added). Sekido further teaches that increasing the size of the LCD screen will increase the number of driver ICs in the panel. (Par. [0008]). Other prior art references discussed below also teach the use of multiple source and gate drivers for a large sized or high resolution LCD panel.

51. As shown above in Figure 4B, the gate line G_i (e.g., G_1, G_2, and G_3) in each row is connected to the gates of each TFT in that row. However, for each column, the first and second data lines D_j and $D_{j'}$ that form a group of data lines are not connected to all TFTs in that column. Instead, the first data line D_j in each column is connected only to the sources of the TFTs in the ***odd rows*** (see the red boxes in R1, R3, etc.) of that column,

while the second data line $D_{j'}$ in the same column is connected only to the sources of the TFTs in the ***even rows*** (see the green box in R2) that column. (*Id.* at Col. 8:10-31).

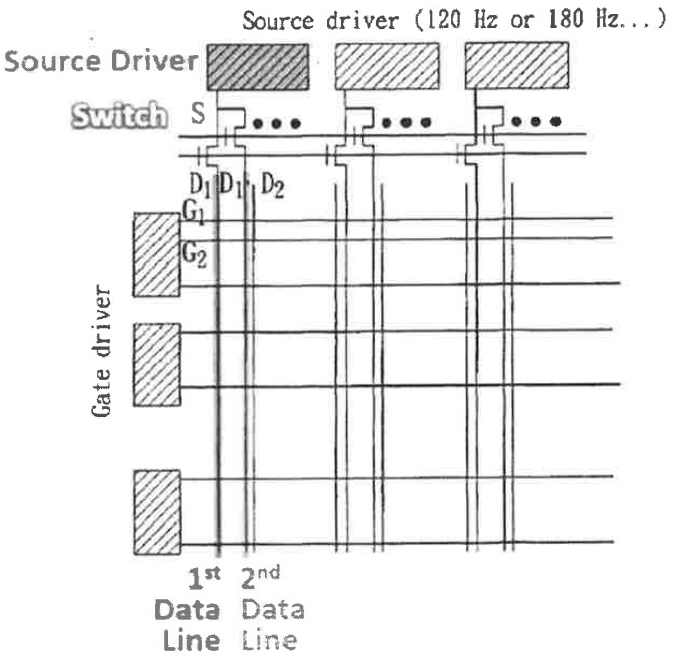
52. For example, referring to the first group of data lines D_1 and $D_{1'}$ (see the red and green lines) in first column (C1) of Figure 4B above, the first data line D_1 (see the red line) is connected to the sources (red dots) of the TFTs in the first and third rows (red boxes in R1 and R3 of the first column C1), while the second data line $D_{1'}$ (green line) is connected to the source (green dot) of the TFT in the second row (green box in R2 of the first column C1). Similarly, for the second pair of data lines (i.e., D_2 and $D_{2'}$) in the second column, the first data line (i.e., D_2) is connected to the sources of the TFTs in the first and third rows (i.e., R1 and R3 of the second column C2), while the second data line $D_{2'}$ is connected to the source of the TFT in the second row (i.e., R2 of the second column C2).

53. According to the '550 Patent, this alternating connection with the Odd Row/Even Row ("Odd Row/Even Row" configuration) reduces the response time of the LCD panel. (*Id.* at Col. 3:35-40). However, the '550 Patent does not explain how this reduction occurs.

54. The gate lines are connected to the gate driver are "insulated with each other;" and the data lines are connected to the source driver and are "insulated with each other." (Ex. 1001, '550 Patent, Col. 8:20-22, Col. 8:29-31). The '550 Patent goes on to explain that a space is provided between the neighboring data lines (e.g., $D_{1'}$ and D_2) to prevent them from short circuiting. (Ex. 1001, '550 Patent, Col. 8:31-36, Fig. 4C).

55. As shown below in annotated Figure 6A, the first and second data lines D_j and $D_{j'}$ (e.g., red and green lines D1 and D1') in each group (i.e., pair) of data lines are connected to the same source driver (purple box), and data is transferred to these data lines by an electronic switch S (highlighted in yellow). (*Id.* at Col. 5:4-8, Col. 8:50-52).

'550 Patent Fig. 6A



56. In addition, all of the source drivers are installed on the same side (e.g., upper side) of the LCD panel. (*See also id.* at Fig. 4A, Col. 8:37-38). The '550 Patent acknowledges that these components were arranged in the exact same way in the "Prior Art" in Figure 1A. (*Id.* at Col. 1:36-45, Fig. 1A).

57. The '550 Patent also states that the gate driver can be "a chip on glass or an integrated gate driver circuit on glass." (*Id.* at Col. 8:53-54). However, the '550 Patent does not define either of these terms, nor does it explain the difference between "a chip on glass" and "an integrated gate driver circuit on glass."

PROSECUTION HISTORY OF THE '550 PATENT

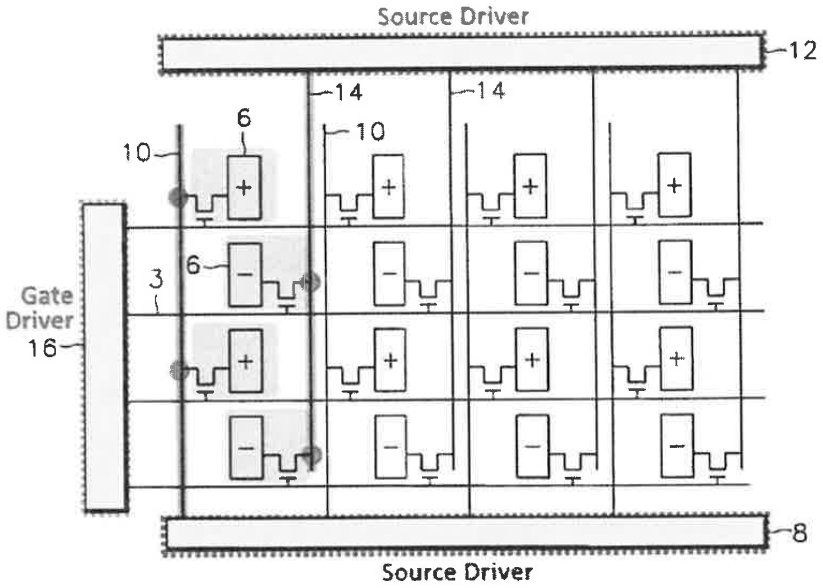
58. I understand that as originally filed, the application for the '550 Patent included claims directed to six different embodiments described in the '550 Patent. I also understand that, in response to a "Restriction Requirement" (Ex. 1005, p. 122), only the claims directed to the "First Embodiment" (i.e., "Species I; Figures 4A-4C") (*Id.* at p. 127) were elected and the claims directed to the other embodiments were canceled.

59. I understand that during prosecution, the application claim corresponding to Claim 1 of the '550 Patent was rejected as anticipated by U.S. Patent No. 5,805,128 to Kim et al. (Ex. 1006, "Kim"). (*See* Ex. 1005, p. 141). This application claim was identical to Claim 1, except that it did not include the last element of Claim 1, namely "the first data lines and the second data lines of each group of data lines are connected with the same source driver." (*See id.* at pp. 31, 152).

60. As shown below, annotated Figure 5 of Kim shows an LCD driving device of matrix structure type including the Odd Row/Even Row configuration, gate lines 3 connected to a gate driver 16, first data lines 10 connected to a data driver 8 on the bottom, and second data lines 14 connected to a data driver 12 on the top. (Ex. 1006, Kim, Col.

3:26-37, Col. 4:28-51, FIG. 5). I note that Figure 5 of Kim shows the Odd Row/Even Row configuration that is virtually identical to the one shown in Figures 5A and 5B of the '550 Patent.

Kim Fig. 5



61. In the prosecution history, I did not find any argument by the applicants disputing the Examiner's position that Kim disclosed ***all elements*** of the rejected claim, including the Odd Row/Even Row configuration and gate driver**s**. Rather, the applicants distinguished the rejected claim over Kim by including an additional claim limitation, namely that "the first data lines and the second data lines of each group of data lines are connected with the same source driver." (Ex. 1005, pp. 152, 156). The claim was subsequently allowed by the Examiner.

62. Even though Figure 5 of Kim does not disclose "the same source driver" limitation, the technique of connecting first and second data lines of each group of data lines with the same source driver in an LCD device was well known in the prior art, including the Sharp Reference and Shimada as discussed below. I understand that none of the Sharp Reference, Shimada, and Kamizono referred to in this declaration was considered by the Examiner during prosecution of the '550 Patent.

CLAIM CONSTRUCTION

63. I understand that in *inter partes* review proceedings, patent claims are to be given their "broadest reasonable" construction in light of the specification as would be read by a person of ordinary skill in the art.

64. Most of the terms of Claims 1-5 of the '550 Patent are clear to me, except for the following terms.

"The first and the second date lines of the first group of date lines"

65. Independent Claims 1 and 2 each recite that "the first and the second **date lines** of the first group of **date lines** are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column . . . ." (Ex. 1001, '550 Patent, Col. 19:52-56, Col. 20:13-17) (emphasis added). Nowhere else in the '550 Patent is there any mention or discussion of "date lines." I believe that the term "date lines" in this claim recitation is meant to be "data lines."

"Gate lines . . . insulated with each other" and "data lines . . . insulated with each other"

66. Independent Claims 1 and 2 each recite "a group of N gate lines . . . **insulated with each other**" and "M groups of data lines . . . **insulated with each other**." (Ex. 1001, '550 Patent, Col. 19:44-45, 51-52, Col. 20:5-6, 12-13) (emphasis added). The '550 Patent does not explain what "insulated with each other" means. Rather, the specification uses the same phrase "insulated with each other" when describing the data lines 111 and gate lines 121 shown in the "Prior Art" in Figures 1A and 1B of the '550 Patent (*id.* at Col. 1:45-47), as well as the data lines (D_1, $D_{1'}$, D_2, $D_{2'}$) and the gate lines (G_1, G_2, G_3) shown in Figures 4A-4C of the First Embodiment. (*Id.* at Col. 8:20-22, 29-31).

67. I believe that "insulated with each other" means "spaced apart from and parallel to each other." This is consistent with Figures 1A-1B of the "Prior Art" in the '550 Patent, which show that the data lines 111 are spaced apart from and parallel to each other (thereby "insulated with each other") and the gate lines 121 are likewise spaced apart from and parallel to each other (thereby "insulated with each other"). This is also consistent with all of the figures that describe the First Embodiment of the '550 Patent (e.g., Figs 4A-4C, 5A-5B, 6A-6B), which also show that the data lines (e.g., D_1, $D_{1'}$, D_2, $D_{2'}$) are spaced apart from and parallel to each other (thereby "insulated with each other"), and the gate lines (e.g., G_1, G_2, G_3) are spaced apart from and parallel to each other (thereby "insulated with each other").

"the gate drivers" and the "source drivers"

68. Independent Claims 1 and 2 refer to "gate lines connected to the ***gate drivers***" and "data lines connected to the ***source drivers***." However, the term "source driver" is not mentioned in the specification of the '550 Patent. Rather, the specification refers to "data drivers."

69. Using the broadest reasonable construction, I believe that a person of ordinary skill in the art would construe these terms as written in the plural form, that is, "the gate drivers" refer to more than one gate driver and "the source drivers" refer to more than one source driver.

70. However, the specification, drawings, and prosecution history of the '550 Patent use the terms "source drivers" and "gate drivers" to cover a variety of driving circuits and configurations known at the time of the invention. These are discussed below:

1. "Gate Drivers" and "Source Drivers" May Refer to Multiple Driving Circuits

71. In the certain figures in the '550 Patent, the "gate drivers" and "source drivers" are used to refer to multiple driving circuits, as shown in the "Prior Art" (e.g., Fig. 1A of the '550 Patent). As shown in Figure 1A, the "gate driver" and "source driver" each comprise multiple driver circuits (e.g., integrate circuit (IC) chips in the purple and orange boxes).

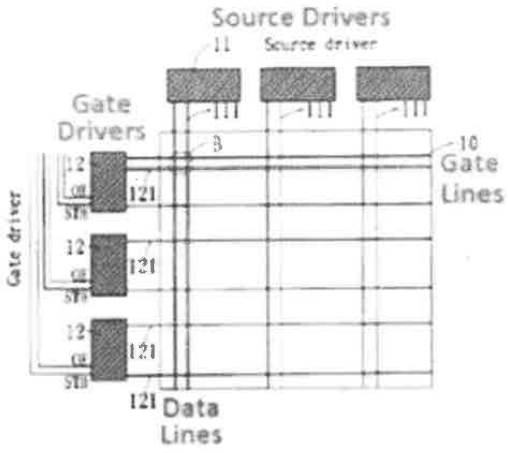


Fig. 1A (Prior Art)

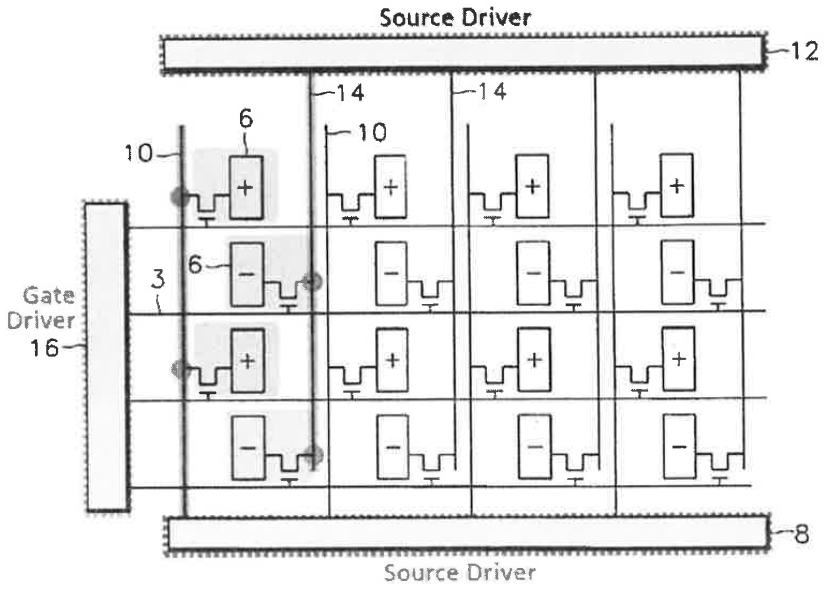
72. At the time that the '550 Patent was filed, it was widely known that such drivers could be implemented using multiple IC chips. Specifically, as LCD displays increase in size with the increased number of pixels, the number of gate lines and data lines likewise increases. However, it becomes difficult, from a packaging and cost perspective, to fabricate a ***single*** chip capable of driving ***hundreds or even thousands*** of data and source lines. Therefore, a person of ordinary skill in the art would use multiple driver IC chips in larger sized LCD panels to keep costs, time and labor down and to simplify packaging.

2. "Gate Drivers" and "Source Drivers" May Refer to A Single Circuit With Multiple Outputs

73. In addition, a person of ordinary skill in the art would understand that "gate drivers" and "source drivers" includes a single circuit (whether an IC or made up of discrete components) having multiple outputs. In that case, a person of ordinary skill in the art would understand that each data or gate line is connected to a separate "driver." This is because

each output provides a unique signal to a data or gate line. This is illustrated, for example, in the Kim reference (Ex. 1006), cited during the prosecution of the '550 Patent (discussed above). As shown below in Figure 5, the gate driver 16 of Kim is depicted as a single circuit block having multiple output lines. The Examiner found that Kim discloses the claimed "gate drivers." (Ex. 1005, p. 141). The applicants did not dispute this. The Examiner and applicants' understanding is consistent with that of a person of ordinary skill in the art at the time of the invention.

Kim Fig. 5



LEVEL OF SKILL IN THE ART

74. A person of ordinary skill in the art would have had an undergraduate degree in electrical engineering, or equivalent work experience. That person would also have had 2

to 5 years of experience designing flat panel display drive electronics, designing active matrices for LCDs, or designing IC drivers.

STATE OF THE ART

75. By the filing date of the '550 Patent in 2004, the LCD display industry had numerous multi-national companies manufacturing LCD displays in volume for various consumer applications like notebook computers, desktop monitors, televisions, pocket entertainment devices, and mobile phones. Competition for market share was fierce, and older LCD issues like limited viewing angle, display brightness, and motion blur were incrementally improved with each product introduction. As the LCD industry grew, so did the support infrastructure for liquid crystal material, substrate glass, polarizer material, backlight modules, light control films, chemicals for color filters, and silicon drive ICs. The LCD manufacturer had multiple supply sources for each of these components.

76. The LCD driver ICs for source and gate drivers were designed by companies in close communication with the panel manufacturers. These ICs use conventional single crystal silicon processing and are manufactured in multiple foundries. The time from driver specification to volume manufacture was on the order of one year. Therefore, panel manufacturers used the ICs that were available at the time of their product introductions.

77. The LCD driver ICs had increasing number of output channels, faster clocking speeds, different logic interfaces, and more features for the display manufacturers. The ICs were sold for COG assembly or Tape Automated Bonding (TAB). The COG method uses an

Anisotropic Conductive Film (ACF) for interconnection between the driver pads and the panel electrodes. The TAB method, along with numerous variations, attaches the driver die to a flexible film with copper traces. The driver outputs are connected to the panel electrodes with ACF, and the logic inputs and power to the driver are connected with ACF or conventional connectors. The display module assembly used COG and TAB extensively since the 1990's. It was also well-known at the time of the filing date of the '550 Patent that an LCD panel must include a glass substrate or other substantially transparent substrate to transmit the light from the backlight to the LCD viewer's eyes. LCD panels modulate the light generated by the backlight assembly and passed through the glass substrate (or other transparent substrate) according to the TFT drive signals. The light exits the LCD surface nearest the viewer and allows the viewer to see the visual image generated based on the electrical input signal.

78. The number and location of source and gate drivers depends on the LCD panel size, pixel size, and other market driven factors. The available drivers could be mounted on a single panel edge or both panel edges. This is true for both the gate axis and the data or source axis. This design change was made as early as the 1970s. When the drivers are attached on opposite panel edges, the interconnection density of connections per linear distance is halved, the driver's power dissipation is spread out, the data clocking rate is halved, peak currents to drivers are distributed more evenly, and the image is more uniform if electrode resistance is an issue across the panel.

79. As of the filing date of the '550 patent, workers in the field of LCD devices were aware of several developments, including:

a. active matrix LCD panels;

b. the Odd Row/Even Row configuration;

c. the use of single or multiple gate drivers and single or multiple source drivers, with the decision to use multiple drivers driven, at least in part, by the size of the LCD panel;

d. the use of chip on glass technology; and

e. the use of integrated driver circuit on glass

SHARP REFERENCE

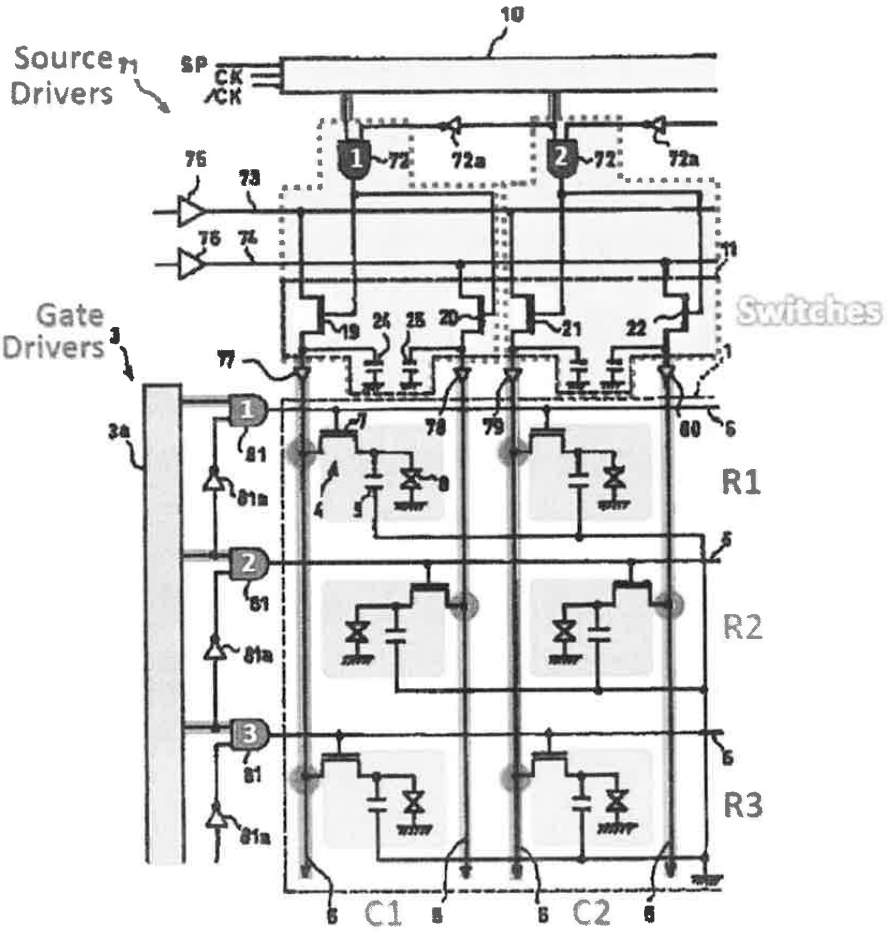
80. The Sharp Reference discloses an LCD device comprising a matrix array of thin film transistors (TFTs) 7, which drive the corresponding array of pixel units 4, as shown below in annotated Figure 10. (Ex. 1002, Sharp Reference, Pars. [0049], [0130], [0140]-[0145], FIG. 10).

81. The Sharp Reference states that its object is to improve image quality by reducing data signal noise and crosstalk (e.g., image blurring) and preventing a "ghost phenomenon" arising from the slow response time. (*Id.*, Par. [0030]).

82. The Sharp Reference also teaches that source driver circuits can be implemented in a certain way (using "driver sample hold method") to solve the problem of

insufficient image data write time arising from increasing the number of pixels in the horizontal scan direction in an LCD panel. (*Id.*, Pars. [0013]-[0019]).

Sharp Reference Fig. 10



83. As shown above in annotated Figure 10, each gate bus line 6 is connected to a gate driver 3. Specifically, each gate bus line 6 is associated with a unique AND circuit 81 (e.g., shaded in orange and labeled as "1"), and gate shift register 3a. In this way, each

gate bus line 6 is individually driven by the output of the unique AND circuit 81. (*Id.*, Pars. [0142]-[0145], FIG. 10).

84. I believe that under the broadest reasonable construction discussed above, a person of ordinary skill in the art would have understood that Figure 10 of the Sharp Reference explicitly shows multiple gate drivers. Specifically, I believe that each gate driver includes gate shift register 3a and an AND circuit 81 connected to an individual gate line 6 because they operate together to generate a non-overlapping gate pulse for each gate line 6. The first gate driver is the AND circuit "1" in communication with shift register 3a; the second gate driver is the AND circuit "2" in communication with shift register 3a; and the third gate driver is the AND circuit "3" in communication with shift register 3a. (*Id.*).

85. Annotated Figure 10 also shows groups of source bus lines 5 connected to the source drivers 71.

86. I believe that under the broadest reasonable construction discussed above, a person of ordinary skill in the art would have understood that Figure 10 of the Sharp Reference explicitly shows multiple source drivers. Specifically, I believe that each source driver includes source shift register 10, AND circuit 72, data signal lines 73, 74, sampling switches 19, 20 (or 21, 22), and sampling capacitors 24, 25 (or 26, 27). The first source driver includes AND circuit 72 (labeled "1") in communication with shift register 10, data signal lines 73, 74, sampling switches 19, 20, and sampling capacitors 24, 25. The second source driver includes AND circuit 72 (labelled "2") in communication with shift register 10,

sampling switches 21 and 22, and sampling capacitors (not numbered). (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], [0145], FIG. 10).

87. As shown above in annotated Figure 10, each set of first source bus line 5 (red) and second source bus line 5 (green) in each column (e.g., C1, C2) is associated with a unique AND circuit 72 (e.g., shaded in purple and labeled as "1" and "2"). This unique AND circuit 72 operates with the associated circuit elements, i.e., source shift register 10, and a unique set of sampling switches (e.g., 19, 20) and sampling capacitors (e.g., 24, 25) to drive the first and second source bus lines (red and green lines) in each group of source bus lines 5. (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], [0145], FIG. 10).

88. For example, for the first source driver in the first column C1, the AND circuit 72 obtains the output of the source shift register 10 and inputs its logical product to the gate terminals of the sampling switches 19 and 20. Meanwhile, data signals from the data signal lines 73 and 74 are respectively input to the source terminals of the sampling switches 19 and 20, and their outputs are respectively held in the sampling capacitors 24 and 25. These held output signals are then input to the first and second source bus lines 5 on both sides of pixel units 4 in the first column C1. For the second source driver in the second column C2, the AND circuit 72 obtains the output of the source shift register 10 and inputs its logical product to the gate terminals of the sampling switches 21 and 22. Meanwhile, data signals from the data signal lines 73 and 74 are respectively input to the source terminals of the sampling switches 21 and 22, and their outputs are respectively held in the sampling

capacitors (not numbered). These held output signals are then input to the first and second source bus lines 5 on both sides of pixel units 4 in the second column C2. (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], [0145], FIG. 10). In this way, each set of first and second source bus lines 5 associated with each column of pixel units 4 are individually driven by a separate source driver. Accordingly, I believe that the Sharp Reference explicitly teaches multiple source drivers.

89. The Sharp Reference also teaches that the gate bus lines 6 are spaced apart from and parallel to each other (i.e., insulated with each other), and that the source bus lines 5 are likewise spaced apart from and parallel to each other (i.e., insulated with each other). (*Id.*, FIG. 10).

90. As shown above in annotated Figure 10, each gate bus line 6 is connected with the gates of all of the TFTs 7 in the row associated with that gate bus line. For example, the first gate line 6 is connected with the gates of all of the TFTs 7 of the first row (R1), the second gate line 6 is connected with the gates of all of the TFTs 7 of the second row (R2), etc. (*Id.*, Par. [0143], FIG. 10).

91. Annotated Figure 10 above also shows the claimed Odd Row/Even Row configuration. In this regard, the first source bus line 5 (red line) and the second source bus line 5 (green line) in each group of data bus lines are respectively connected with the sources of all of the TFTs 7 of the **odd rows** (red boxes in R1 and R3) and **even rows**

(green boxes in R2) of the column (C1, C2) associated with that group of source bus lines, as required by all Claims of the '550 Patent.

92. For example, the first source bus line 5 (red line) of the first group is connected with the sources (red dots) of the TFTs 7 of the first row and third row (see the red boxes in R1 and R3) in the first column C1, while the second source bus line 5 (green line) of the first group is connected with the sources (green dot) of the TFT 7 of the second row (green box in R2) in the first column C1. (*Id.*, Pars. [0131]-[0140], [0145], FIG. 10). The same Odd Row/Even Row configuration is provided in each column (e.g., C2).

93. The benefits of the Odd Row/Even Row configuration were already well known in the prior art, including the Sharp Reference. The Sharp Reference teaches that the Odd Row/Even Row configuration in an LCD Panel prevents adjacent pixel TFTs 7 in the column direction from being turned on simultaneously. This reduces the effect of data signal noise and therefore improves the video quality of the LCD panel. (*Id.*, Pars. [0144]-[0145], [0030]).

94. In this regard, I believe that the benefits of using the Odd Row/Even Row configuration became particularly significant as the size of the LCD panel and/or the number of pixels increased. When LCD screens became large enough to compete against the conventional cathode ray tube (CRT) screens, there was market and design need to improve the video quality of LCD panels. But this required increased number of pixels in an LCD panel and at the same time, a faster way to drive these pixels accurately. The Odd

Row/Even Row configuration was one of the various techniques developed in the prior art to meet this need.

95. As shown in Figure 10, the source drivers 71 for all source bus lines 5 are installed on the same side (e.g., upper side) of the display panel.

96. Figure 10 also shows that the first and the second source bus lines 5 (the red and green lines) in each group of source bus lines are connected with the same source driver. (*Id.*, Pars. [0131]-[0140], FIG. 10).

97. The transfer of data signals from the data signal lines 73, 74 to the first and the second source bus lines 5 (the red and green lines) is switched by sampling switches 19, 20 (or 21, 22) (highlighted in yellow). (*Id.*, Pars. [0134]-[0135], [0137]-[0139], FIG. 10).

THE SHARP REFERENCE ANTICIPATES CLAIMS 1-3

98. As discussed below, I believe that the Sharp Reference explicitly discloses each and every element of Claims 1-3 of the '550 Patent.

99. As shown below in annotated Figure 10, the Sharp Reference teaches an LCD device comprising a matrix array of thin film transistors (TFTs) 7, which drive the corresponding array of pixel units 4. (*Id.*, Pars. [0049], [0130], [0140]-[0145], FIG. 10).

THE SHARP REFERENCE DISCLOSES MULTIPLE GATE DRIVERS

100. As explained above in paragraph 84, I believe that Figure 10 of the Sharp Reference explicitly discloses multiple gate drivers.

101. As shown in Figure 10, gate lines 6 are connected to the corresponding gate drivers 3, as required by Claims 1 and 2.

102. Each gate driver comprises gate shift register 3a, and AND circuit 81. (*Id.*, Pars. [0142]-[0145], FIG. 10).

THE SHARP REFERENCE DISCLOSES MULTIPLE SOURCE DRIVERS

103. As explained above in paragraphs 86-88, Figure 10 also explicitly discloses multiple source drivers.

104. As shown in Figure 10, groups of data lines 5 are connected to the corresponding source drivers 71.

105. Each source driver comprises source shift register 10, AND circuit 72, data signal lines 73, 74, sampling switches 19, 20 (or 21, 22), and sampling capacitors 24, 25 (or 26, 27). (Ex. 1002, Sharp Reference, Pars. [0131]-[0139], FIG. 10).

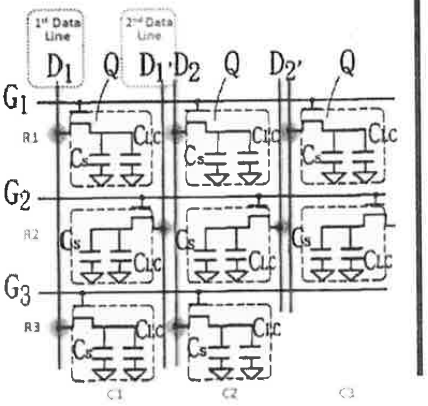
THE SHARP REFERENCE DISCLOSES THAT FIRST AND SECOND DATA LINES IN EACH GROUP OF DATA LINES ARE CONNECTED WITH THE SAME SOURCE DRIVER

106. As required by Claims 1-2, annotated Figure 10 of the Sharp Reference shows that the first and second data lines (e.g., red and green lines 5) in each group of data lines are connected with the ***same*** source driver (e.g., source driver in purple comprising source shift register 10, AND circuit 72, data signal lines 73, 74, sampling switches 19, 20 (or 21, 22), and sampling capacitors 24, 25 (or 26, 27)). (*Id.*, Pars. [0131]-[0140], FIG. 10). As discussed above, during prosecution, Claim 1 of the '550 Patent was allowed over Kim based on this feature.

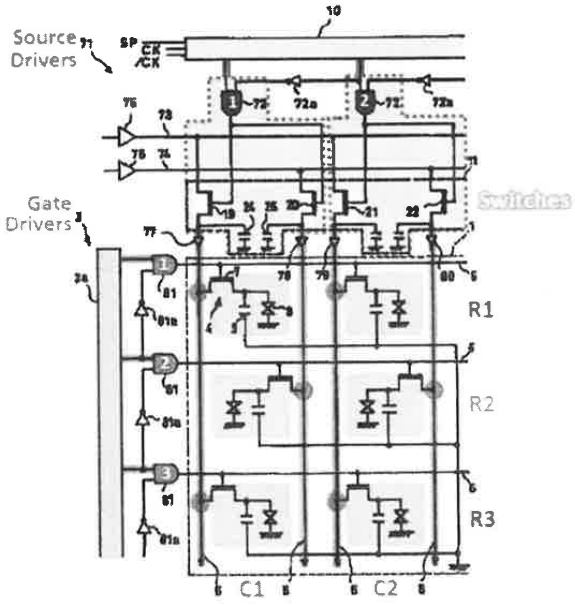
THE SHARP REFERENCE DISCLOSES THAT DATA LINES/GATE LINES ARE INSULATED WITH EACH OTHER

107. As explained above, Figure 10 of the Sharp Reference also shows that the gate lines 6 are "insulated with each other" under the broadest reasonable construction of this term since they are spaced apart from and parallel to each other; and the data lines 5 are likewise insulated with each other as they are spaced apart and parallel to each other. (Ex. 1002, Sharp Reference, FIG. 10). Indeed, the spacing (insulation) between the data and gate lines in the Sharp Reference and the '550 Patent is virtually identical, as shown below in the side-by-side comparison of Figure 4B of the '550 Patent and Figure 10 of the Sharp Reference.

'550 Patent Fig. 4B



Sharp Reference Fig. 10



THE SHARP REFERENCE TEACHES THE ODD ROW/EVEN ROW CONFIGURATION

108. The claimed Odd Row/Even Row configuration of the '550 Patent (shown on the left) is present in the LCD device of the Sharp Reference (shown on the right). (*Id.*, Pars. [0144]-[0145], FIG. 10). Specifically, the first data line 5 (see the red line) is connected to the sources (red dots) of the TFTs (red boxes) in the odd rows (R1 and R3). The second data line 5 (green line) is connected to the sources (green dot) of the TFTs (green boxes) in the even rows (R2). Figure 4B of the later '550 Patent (shown on the left) has the exact same Odd Row/Even Row configuration.

THE SHARP REFERENCE DISCLOSES THAT EACH SOURCE DRIVER IS INSTALLED ON THE SAME SIDE OF THE DISPLAY PANEL

109. Figure 10 of the Sharp Reference also shows that each source driver (e.g., source drivers in purple) is installed on the same side (e.g., upper side) of the display panel (Ex. 1002, Sharp Reference, Pars. [0130]-[0140], FIG. 10), as required by Claim 2.

THE SHARP REFERENCE DISCLOSES SWITCHES FOR DATA TRANSFER

110. Figure 10 of the Sharp Reference shows that data transfer is switched by each sampling switch 19, 20, 21, 22 (*id.*, Pars. [0134]-[0135], [0137]-[0139], FIG. 10), as required by Claim 2.

THE SHARP REFERENCE DISCLOSES A SPACE BETWEEN NEIGHBORING DATA LINES TO PREVENT SHORT CIRCUITING

111. Claim 3, which depends from Claim 2, recites that "there is a space [i.e., a gap] between the neighboring data lines to prevent them from short circuit." Figure 10 of

the Sharp Reference clearly shows a space between the neighboring data lines 5 that prevents short circuiting.

112. Just like in Figure 4B of the '550 Patent, Figure 10 shows that the first data line 5 (red) is on the left side of the pixel TFTs in the first column (C1), and the second data line 5 (green) is on the right side of the pixel TFTs in the first column (C1). This space prevents short circuiting between the first and second data lines.

113. When two neighboring data lines are shown to be spaced apart from each other in the schematic circuit diagrams for an LCD driving device, such as Figure 10 of the Sharp Reference or Figure 4B of the '550 Patent, I expect that there is a sufficient space between these data lines to prevent short circuiting. Otherwise, the LCD driving device would not be operating as described in the reference.

SHARP REFERENCE DISCLOSES EACH AND EVERY ELEMENT OF CLAIMS 1-3

114. The following claim charts summarize where I believe each element of Claims 1-3 is taught by the Sharp Reference:

The Claims Of The '550 Patent	Sharp Reference
1. A liquid crystal display driving device of matrix structure type including:	Sharp Reference discloses a liquid crystal display driving device of matrix structure type (Ex. 1002, Sharp Reference, Pars. [0001]-[0003], [0130], FIG. 10).
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels	Sharp Reference discloses a group of thin film transistors 7 with matrix array consisting of n (e.g., 3) rows and m (e.g., 2) columns of thin film transistors 7, wherein each thin film transistor can drive one pixel unit 4 so that n×m

The Claims Of The '550 Patent	Sharp Reference
can be driven;	(e.g., 3×2) of pixel units can be driven (Ex. 1002, Sharp Reference, Pars. [0049], [0130], [0140]- [0145], FIG. 10).
a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	Sharp Reference discloses a group of n (e.g., 3) gate bus lines 6 connected to the gate drivers 3. The first gate driver is the AND circuit "1" in communication with shift register 3a; the second gate driver is the AND circuit "2" in communication with shift register 3a; and the third gate driver is the AND circuit "3" in communication with shift register 3a. The gate lines are insulated with each other by being spaced apart from and parallel to each other. The first gate bus line 6 is connected with the gates of all the thin film transistors 7 of the first row. The second gate bus line 6 is connected with the gates of all the thin film transistors 7 of the second row . . . and the n^{th} (e.g., 3^{rd}) gate bus line 6 is connected with the gates of all the thin film transistors 7 of the n^{th} (e.g., 3^{rd}) row (Ex. 1002, Sharp Reference, Pars. [0142]-[0145], FIG. 10).
M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines	Sharp Reference discloses m (e.g., 2) groups of source bus lines 5 connected to the source drivers 71. The first source driver includes AND circuit 72 (labeled "1") in communication with shift register 10, data signal lines 73, 74, sampling switches 19, 20, and sampling capacitors 24, 25. The second source driver includes AND circuit 72 (labelled "2") in communication with shift register 10, sampling switches 21 and 22, and sampling capacitors (not numbered). The groups of data lines are insulated with each other by being spaced apart from and parallel to each other. The first and the second source bus lines 5 of the first group of source bus lines are respectively connected

The Claims Of The '550 Patent	Sharp Reference
are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column, and	with the sources of all the thin film transistors 7 of the odd and the even rows of the first column. . . . The first and the second source bus lines 5 of the m^{th} (e.g., 2^{nd}) group of source bus lines are respectively connected with the sources of the all the thin film transistors 7 of the odd and the even rows of the m^{th} (e.g., 2^{nd}) column (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], [0145], FIG. 10).
the first data lines and the second data lines of each group of data lines are connected with the same source driver.	Sharp Reference discloses that the first source bus lines 5 and the second source bus lines 5 of each group of source bus lines are connected with the same source driver 10, 72, 73, 74, 19, 20, 24, 25 (or 10, 72, 73, 74, 21, 22, 26, 27) (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], FIG. 10).
2. The liquid crystal display device of matrix structure type including:	See Claim 1 above.
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels can be driven;	See Claim 1 above.
a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	See Claim 1 above.
M groups of data lines connected to the source drivers and insulated with	See Claim 1 above.

The Claims Of The '550 Patent	Sharp Reference
each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column,	
wherein the first data lines and the second data lines of each group of data lines are connected with the same source driver,	See Claim 1 above.
each source driver is installed on the same side of the display panel and	Sharp Reference discloses that the first source driver(AND circuit 72 (labeled "1") in communication with shift register 10, data signal lines 73, 74, sampling switches 19, 20, and sampling capacitors 24, 25) and the second source driver (AND circuit 72 (labelled "2") in communication with shift register 10, sampling switches 21 and 22, and sampling capacitors (not numbered)) are installed on the same side (e.g., upper side) of the display unit 1 (Ex. 1002, Sharp Reference, Pars. [0130]-[0140], FIG. 10).
the data transfer is switched by an electronic switch.	Sharp Reference discloses that the data transfer is switched by each sampling switch 19, 20, 21, 22 (Ex.1002, Sharp Reference, Pars. [0134]-[0135], [0137]-[0139], FIG. 10).
3. The liquid crystal display driving	Sharp Reference discloses that there is a space

The Claims Of The '550 Patent	Sharp Reference
device of matrix structure type as claimed in claim 2, wherein there is a space between the neighboring data lines to prevent them from short circuit.	between the neighboring data lines 5. These spaces prevent the data lines from short circuiting. (Ex. 1002, Sharp Reference, FIG. 10).

115. Accordingly, it is my opinion that Claims 1-3 of the '550 Patent are anticipated by the Sharp Reference.

THE SHARP REFERENCE RENDERS CLAIMS 1-3 AND 5 OBVIOUS TO A PERSON OF ORIDNARY SKILL IN THE ART

116. As discussed above, it is my opinion that the Sharp Reference explicitly discloses each and every element of Claims 1-3 of the '550 Patent, including the claimed source and gate drivers, and thus anticipates Claims 1-3.

117. I believe that no reasonable person of ordinary skill in the art would have interpreted the Sharp Reference as disclosing only a single source driver and a single gate driver in Figure 10.

118. Even under such a tenuous and narrow interpretation of the Sharp Reference, I believe that Claims 1-3 would be obvious to a person of ordinary skill in the art.

THERE IS NO UNEXPECTED RESULT FROM USING MULTIPLE SOURCE AND GATE DRIVERS IN AN LCD PANEL INSTEAD OF A SINGLE SOURCE DRIVER AND A SINGLE GATE DRIVER

119. I understand that one way of demonstrating obviousness in the situation where a prior art reference discloses a single element but the claim requires multiple

elements is to demonstrate that there are no new and unexpected results from increasing the number of such elements.

120. The duplication of the source and gate drivers shown in Figure 10 of the Sharp Reference simply allows more pixels to be added when increasing the size of the LCD panel. The addition of source and gate drivers would not change the way the LCD Panel of the Sharp Reference operates in the Odd Row/Even Row configuration. Accordingly, no unexpected results would be produced from duplicating the source and gate driver circuits (i.e., adding more drivers) shown in Figure 10 of the Sharp Reference.

121. The prior art was abundant with examples of larger sized LCD panels using multiple source and gate drivers. In fact, when I was working in the LCD industry prior to the filing date of the '550 Patent, it was a routine industry practice to change the panel design to increase the size of the panel and/or the number of pixels by simply adding more driver ICs. For example, while the ***small***, low cost LCD panel (which had an equivalent pixel dimension of 7×4) that I worked on at Alien Technology had only a single source driver and a single gate driver, the ***large sized*** LCD panels (which had pixel dimension of at least 800×600) that I worked on at Philips used multiple driver ICs. Using additional source and gate drivers in connection with increasing the size of the panel or the number of pixels in an LCD panel was a well-known and readily available design option.

122. Consistent with my experience and as discussed above, the prior art reference (Ex. 1009) states that "in order to drive many gate bus lines and the source bus

lines on the display circuit board, ***a plurality of the gate drivers and source drivers must*** be connected to the area around the liquid crystal display panel." (*Id.*, Par. [0006]) (emphasis added). Sekido further teaches that increasing the size of the LCD screen will increase the number of the driver ICs. (*Id.*, Par. [0008]).

123. As explained in the Sharp Reference, its use of the Odd Row/Even Row configuration improves the image quality of an LCD panel with the increased number of pixels by reducing the effect of data signal noise. (Ex. 1002, Sharp Reference, Pars. [0144]-[0145], [0030]).

124. Hence, I believe that duplication of source and gate drivers for a larger sized LCD device would have involved only routine skill in the art and does not produce any unexpected result.

125. The '550 Patent fails to demonstrate or even suggest any new and unexpected results stemming from having more than one source driver circuit and more than one gate driver circuit in the claimed LCD driving device. The '550 Patent includes no explanation of the difference between having a single source driver and a single gate driver and having multiple source and gate drivers in the LCD device.

126. In fact, the '550 Patent interchangeably uses the singular ("source driver"/"gate driver") and plural ("source drivers"/"gate drivers") to describe these components. (*See* Ex. 1001, '550 Patent, Col. 8:21 ("[T]here are N gate lines connected to

gate driver . . . ." (emphasis added)); *see also id.*, Figure 1A and Col. 1:36-45 (using the singular terms "data driver 11" and "gate driver 12")).

127. In addition, during prosecution of the '550 Patent, the applicants did not dispute the Examiner's finding that Figure 5 of Kim (Ex. 1006), which shows a ***single*** block for gate driver 16, meets the gate driver**s** limitation of Claims 1 and 2. (Ex. 1005, p. 156).

128. Even if, contrary to my opinion, Patent Owner contends that the Sharp Reference does not disclose the claimed "source drivers" and "gate driver," I believe that it would nevertheless have been obvious to a person of ordinary skill in the art to modify the LCD driving device of the Sharp Reference to include additional source and gate driver circuits in addition to what are shown in Figure 10.

129. It is my opinion that at a minimum, Claims 1-3 of the '550 Patent are obvious over the Sharp Reference.

THE SHARP REFERENCE DISCLOSES INTEGRATED GATE DRIVER CIRCUIT

130. Claim 5 requires that the "gate driver is an integrated gate driver circuit installed on glass." However, this would have also been obvious in view of the Sharp Reference.

131. The Sharp Reference teaches that the gate driver, the source driver, and the display unit consisting of a plurality of pixel units in an LCD device can be formed monolithically on the same substrate in an LCD panel to "to improve the drive force of the pixel transistor that accompanies larger screen size, and to reduce the drive IC mounting

costs and the like." (Ex. 1002, Sharp Reference, Claim 6, Pars. [0160], [0172]-[0173], [0008], [0020], [0036], [0045]). Since the gate drivers are formed monolithically on the same substrate as the pixel TFTs, the result is an integrated gate driver circuit installed on the same substrate as the pixel TFTs.

132. Moreover, It was well-known at the time of the filing date of the '550 Patent that an LCD panel must include a glass substrate or other substantially transparent substrate to transmit the light from the backlight to the LCD viewer's eyes. LCD panels modulate the light generated by the backlight assembly and passed through the glass substrate (or other transparent substrate) according to the TFT drive signals. The light exits the LCD surface nearest the viewer and allows the viewer to see the visual image generated based on the electrical input signal.

133. The use of a glass substrate was the preferred choice, especially in an LCD panel having a large number of pixels. Compared to other transparent materials, glass is cheaper, provides a smoother surface, and is also more resistant to a high temperature required for processing TFTs in an LCD panel. In addition, a glass substrate protects liquid crystal materials and TFTs in the LCD panel from moisture. In my experience, LCD panels with a large number of pixels using TFTs all included glass substrates.

134. Thus, I believe that it would have been obvious to a person of ordinary skill in the art that the integrated gate driver circuit taught by the Sharp Reference is installed on a glass substrate in an LCD panel since the use of glass substrate is one of small number of

widely known design options for an LCD panel having the light transmitted from the backlight. Since this technology was widely understood and available at the time the '550 Patent was filed, I believe that a person of ordinary skill in the art would have been successful in forming an integrated gate driver circuit on a glass substrate.

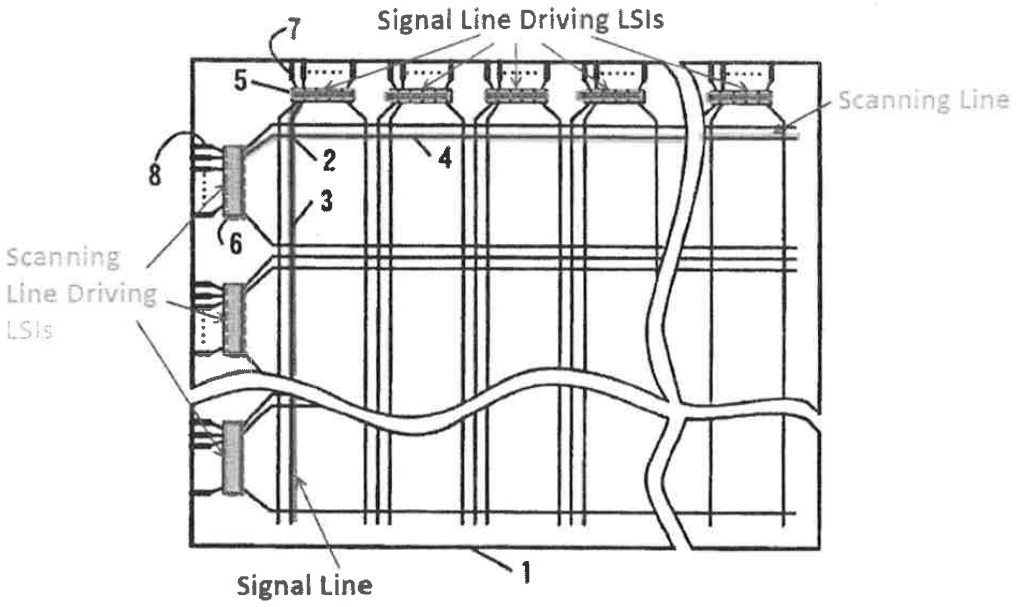
135. Accordingly, it is my opinion that Claim 5 of the '550 Patent is also obvious over the Sharp Reference.

KAMIZONO

136. Kamizono describes an active matrix LCD for a video monitor such as a television receiver or a computer display, and teaches fabricating circuits that are suitable for a large sized LCD panel. (Ex. 1004, Kamizono, Abstract, Col. 1:5-7, Col. 3:1-36).

137. As shown below in annotated Figure 15, Kamizono teaches an LCD panel 1 having data lines ("signal lines 3") connected to multiple source driver ICs ("signal line driving LSIs 5") and gate lines ("scanning lines 4") connected to multiple gate driver ICs ("scanning line driving LSIs 6"). A pixel is located at the intersection 2 between a data line 3 and a gate line 4. The pixels are arranged in the image display region of the LCD panel, while the driving LSIs are arranged in the non-image display region of the panel. (*Id.*, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15). The source driver ICs 5 send data signals to operate TFTs and pixels via data lines 3, while the gate driver ICs 6 send voltage pulse to the gates of TFTs via gate lines 4.

Kamizono Fig. 15



138. Kamizono further teaches that while a "small sized" LCD panel has "a few (2 or 3) of the [driving] LSIs," a "large-screen" LCD panel uses more driving LSIs, such as 4 or 5 scanning line driving LSIs and 10 or more signal line driving LSIs. (*Id.*, Col. 9:19-20, Col. 11:53-64, FIGS. 5, 9, and 15).

139. Kamizono also teaches that for an LCD device having an "increased screen size," these multiple source or gate drivers ("liquid crystal driving LSIs") are commonly mounted as a semiconductor chip by a chip-on-glass (COG) method or a tape automated bonding (TAB) method. According to Kamizono, the COG method is preferred over the TAB

method because of the operational reliability and reduction of the overall product size provided by the COG method, which is consistent with my experience. (*Id.*, Col. 1:12-58).

140. I understand chip-on-glass (COG) to be a method of attaching single-crystal silicon die or Large Scale Integrated (LSI) circuits directly on the glass substrate of the LCD panel. The benefits of using COG are increased reliability, smaller LCD module size, and less weight. The silicon die are designed and fabricated by conventional silicon wafer processes. The die are electrically connected to the panel either through wire bonding or using Anisotropic Conductive Film (ACF). ACF is a type of plastic that contains metalized spheres. The density of the spheres in the film prevents adjacent sphere to sphere connection but connects the die output pads to the panel electrode pads through the thin plastic film.

141. Kamizono further teaches that an LCD panel 1 can be a poly-Silicon TFT panel and the source and gate drivers can be mounted on the panel in the non-image display area of the panel ("a spare area other than a display area of the liquid crystal panel 1"). (*Id.*, Col. 13:50-55). Since the gate drivers are formed on the same substrate as the pixel TFTs, the result is integrated gate driver circuit installed on the same substrate as the pixel TFTs.

CLAIMS 1-5 ARE OBVIOUS OVER THE SHARP REFERENCE IN VIEW OF KAMIZONO

142. I reiterate my opinion discussed above that the Sharp Reference expressly discloses each and every element of Claims 1-3, including the claimed source and gate drivers, and thus anticipates Claims 1-3.

143. Again, to the extent that the Patent Owner argues that the Sharp Reference discloses only a single source driver and a single gate driver in Figure 10, no reasonable person of ordinary skill in the art would agree.

MODIFICATION OF THE LCD DRIVING DEVICE OF THE SHARP REFERENCE TO INCLUDE MULTIPLE SOURCE AND GATE DRIVERS OF KAMIZONO WOULD HAVE BEEN WITHIN THE SKILL OF A PERSON OF ORDINARY SKILL IN THE ART AND WOULD HAVE PRODUCED NO UNEXPECTED RESULT

144. Kamizono teaches the use of multiple source driver ICs 5 and multiple gate driver ICs 6 to send signals through data lines and gate lines in an LCD device. Indeed, Figure 15 of Kamizono is virtually identical to Figure 4A of the '550 Patent.

145. For the reasons discussed below, it is my opinion that even under such a misreading of the Sharp Reference, it would still have been obvious to a person of ordinary skill in the art to combine the teachings of the Sharp Reference and Kamizono to arrive at the LCD driving device of Claims 1-5 of the '550 Patent.

146. The Sharp Reference and Kamizono are in the same field of LCD display technology. They both disclose active matrix LCD devices and are both directed to improving the performance of a large sized LCD panel. The Sharp Reference teaches that source drivers can be implemented in a certain way (e.g., using "driver sample hold

method") to solve the problem of insufficient image data write time arising from increasing the number of pixels in in an LCD panel. (Ex. 1002, Sharp Reference, Pars. [0013]-[0019]). Kamizono teaches that a "large-screen" LCD panel uses more source and gate driver LSIs than a "small sized" LCD panels would use. (Ex. 1004, Kamizono, Col. 9:19-20, Col. 11:53-64, FIGS. 5 and 9). Because both references addressed the same design needs for larger sized LCD panels, I believe that a person of ordinary skill in the art making the source and gate driving circuit for a large-screen LCD panel would have been motivated to combine the teachings of the Sharp Reference and Kamizono.

147. The technique of using multiple gate and source drivers has been used to improve Kamizono's larger sized LCD panels. The source drivers and the Odd Row/Even Row configuration taught in the Sharp Reference also improve the larger sized LCD panels. Hence, a person of ordinary skill in the art would recognize that Kamizono's technique would improve similar devices, such as larger sized LCD panels of the Sharp reference, in the same way. In my opinion, using multiple source and gate driver ICs as taught in Kamizono in the LCD panel of the Sharp Reference is well within the level of ordinary skill in the art, particularly since Figure 10 of the Sharp Reference is configured to have separate circuitry drive data through each gate line and each pair of data lines and Kamizono likewise shows separate circuit (i.e., source drivers 5 and data drivers 6).

148. Based on my experience and knowledge, I believe that modifying the LCD driving device of the Sharp Reference to include the multiple source and gate driver ICs of

Kamizono would not produce unexpected result, but would merely lead to a predictable result, since such a modification simply allows more pixels to be added to increase the size of the LCD panel without changing the way LCD Panel operates.

149. Kamizono teaches the use of multiple source and gate drivers (as does the Sharp Reference), and the Sharp Reference discloses all of the other limitations of Claims 1-3, as shown in the claim charts provided above. Moreover, for the reasons discussed above, there was a clear motivation to combine these references. Thus, to the extent that the Patent Owner argues that the Sharp Reference does not teach multiple source and gate drivers, which is contrary to my opinion discussed above, I believe that, at a minimum, Claims 1-3 of the '550 Patent would be obvious over the Sharp Reference in view of Kamizono.

KAMIZONO DISCLOSES A CHIP ON GLASS

150. Dependent Claim 4 requires that the gate driver is a chip installed on glass.

151. Kamizono teaches that the use of a chip-on-glass is the preferred way of implementing the gate drivers for a large sized LCD panel. (Ex. 1004, Kamizono, Col. 1:12-58).

152. Based on my experience and knowledge, I believe that using the chip on glass of Kamizono for the gate driver in the LCD device of the Sharp Reference would not produce any unexpected result and would not affect, for example, the Odd Row/Even Row configuration in the LCD device of the Sharp Reference.

153. Based on my experience and knowledge, I believe that a person of ordinary skill in the art would recognize that Kamizono's technique of using a chip on glass for the gate driver to improve a large screen LCD panel (e.g., increasing the operational reliability and reducing the overall product size--see Ex. 1004, Kamizono, Col. 1:12-58) can be also used to improve the large screen LCD panel of the Sharp Reference in the same way.

154. A person of ordinary skill in the art making a large-screen LCD panel would have been motivated to combine the teachings of the Sharp Reference and Kamizono to arrive at Claim 4.

THE SHARP REFERENCE DISCLOSES INTEGRATED GATE DRIVER CIRCUIT

155. Claim 5 requires that the gate driver is an integrated gate driver circuit installed on glass. As discussed above, this would have been obvious in view of the Sharp Reference.

156. The Sharp Reference teaches that the gate driver, the source driver, and the display unit consisting of a plurality of pixel units in an LCD device can be formed monolithically on the same substrate in an LCD panel to "to improve the drive force of the pixel transistor that accompanies larger screen size, and to reduce the drive IC mounting costs and the like." (Ex. 1002, Sharp Reference, Claim 6, Pars. [0160], [0172]-[0173], [0008], [0020], [0036], [0045]). Since the gate drivers are formed monolithically on the same substrate as the pixel TFTs, the result is integrated gate driver circuit installed on the same substrate as the pixel TFTs.

157. Moreover, as discussed above, it was well-known at the time of the filing date of the '550 Patent that an LCD panel must include a glass substrate or other substantially transparent substrate to transmit the light from the backlight to the LCD viewer's eyes. LCD panels modulate the light generated by the backlight assembly that passes through the glass substrate (or other transparent substrate) according to the TFT drive signals. The light exits the LCD surface nearest the viewer and allows the viewer to see the visual image generated based on the electrical input signal.

158. Again, the use of a glass substrate was the preferred choice, especially in an LCD panel having a large number of pixels. Compared to other transparent materials, glass is cheaper, provides a smoother surface, and is also more resistant to a high temperature required for processing TFTs in an LCD panel. In addition, a glass substrate protects liquid crystal materials and TFTs in the LCD panel from moisture. In my experience, LCD panels with a large number of pixels using TFTs all included glass substrates.

159. Thus, I believe that it would have been obvious to a person of ordinary skill in the art that the integrated gate driver circuit taught by the Sharp Reference is installed on a glass substrate in an LCD panel since the use of glass substrate is one of small number of widely known design options to make an LCD panel and to have the light transmitted from the backlight.

THE COMBINATION OF THE SHARP REFERENCE AND KAMIZONO TEACHES ALL ELEMENTS OF CLAIMS 1-5

160. The following claim charts summarize where I believe each element of Claims 1-5 is taught by the combination of the Sharp Reference and Kamizono:

The Claims Of The '550 Patent	Sharp Reference in View of Kamizono
1. A liquid crystal display driving device of matrix structure type including:	Sharp Reference discloses a liquid crystal display driving device of matrix structure type (Ex. 1002, Sharp Reference, Pars. [0001]-[0003], [0130], FIG. 10).
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels can be driven;	Sharp Reference discloses a group of thin film transistors 7 with matrix array consisting of n (e.g., 3) rows and m (e.g., 2) columns of thin film transistors 7, wherein each thin film transistor can drive one pixel unit 4 so that n×m (e.g., 3×2) of pixel units can be driven (Ex. 1002, Sharp Reference, Pars. [0049], [0130], [0140]- [0145], FIG. 10).
a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	Sharp Reference discloses a group of n (e.g., 3) gate bus lines 6 connected to the gate drivers 3. The gate lines are insulated with each other by being spaced apart from and parallel to each other. The first gate bus line 6 is connected with the gates of all the thin film transistors 7 of the first row. The second gate bus line 6 is connected with the gates of all the thin film transistors 7 of the second row . . . and the n^{th} (e.g., 3^{rd}) gate bus line 6 is connected with the gates of all the thin film transistors 7 of the n^{th} (e.g., 3^{rd}) row (Ex. 1002, Sharp Reference, Pars. [0142]-[0145], FIG. 10). Kamizono discloses scanning lines 4 connected to multiple scanning line driving LSIs 6 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).

The Claims Of The '550 Patent	Sharp Reference in View of Kamizono
M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column, and	Sharp Reference discloses m (e.g., 2) groups of source bus lines 5 connected to the source drivers 71. The groups of data lines are insulated with each other by being spaced apart from and parallel to each other. The first and the second source bus lines 5 of the first group of source bus lines are respectively connected with the sources of all the thin film transistors 7 of the odd and the even rows of the first column. . . . The first and the second source bus lines 5 of the m^{th} (e.g., 2^{nd}) group of source bus lines are respectively connected with the sources of the all the thin film transistors 7 of the odd and the even rows of the m^{th} (e.g., 2^{nd}) column (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], [0145], FIG. 10). Kamizono discloses signal lines 3 connected to multiple signal line driving LSIs 5 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).
the first data lines and the second data lines of each group of data lines are connected with the same source driver.	Sharp Reference discloses that the first source bus lines 5 and the second source bus lines 5 of each group of source bus lines are connected with the same source driver 10, 72, 73, 74, 19, 20, 24, 25 (or 10, 72, 73, 74, 21, 22, 26, 27) (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], FIG. 10).
2. The liquid crystal display device of matrix structure type including:	See Claim 1 above
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels can be driven;	See Claim 1 above
a group of N gate lines connected to	See Claim 1 above

The Claims Of The '550 Patent	Sharp Reference in View of Kamizono
the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	
M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column,	See Claim 1 above.
wherein the first data lines and the second data lines of each group of data lines are connected with the same source driver,	See Claim 1 above
each source driver is installed on the same side of the display panel and	Sharp Reference discloses that the first source driver(AND circuit 72 (labeled "1") in communication with shift register 10, data signal lines 73, 74, sampling switches 19, 20, and sampling capacitors 24, 25) and the second

The Claims Of The '550 Patent	Sharp Reference in View of Kamizono
	source driver (AND circuit 72 (labelled "2") in communication with shift register 10, sampling switches 21 and 22, and sampling capacitors (not numbered)) are installed on the same side (e.g., upper side) of the display unit 1 (Ex. 1002, Sharp Reference, Pars. [0130]-[0140], FIG. 10).
the data transfer is switched by an electronic switch.	Sharp Reference discloses that the data transfer is switched by each sampling switch 19, 20, 21, 22 (Ex.1002, Sharp Reference, Pars. [0134]-[0135], [0137]-[0139], FIG. 10).
3. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein there is a space between the neighboring data lines to prevent them from short circuit.	Sharp Reference discloses that there is a space between the neighboring data lines 5. These spaces prevent the data lines from short circuiting. (Ex. 1002, Sharp Reference, FIG. 10).
4. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein the gate driver is a chip installed on glass.	Kamizono discloses that a liquid crystal driving LSI is commonly mounted as a semiconductor chip by a chip-on-glass (COG) method. (Ex. 1004, Kamizono, Col. 1:12-58).
5. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein the gate driver is an integrated gate driver circuit installed on glass.	Kamizono discloses LCD driving circuits that form an integrated structure with a poly-Silicon TFT panel. (Ex. 1004, Kamizono, Col. 13:50-55).

161. Accordingly, it is my opinion that Claims 4-5 of the '550 Patent are also obvious over the Sharp Reference in view of Kamizono.

CLAIMS 1-5 ARE OBVIOUS OVER SHIMADA IN VIEW OF KAMIZONO

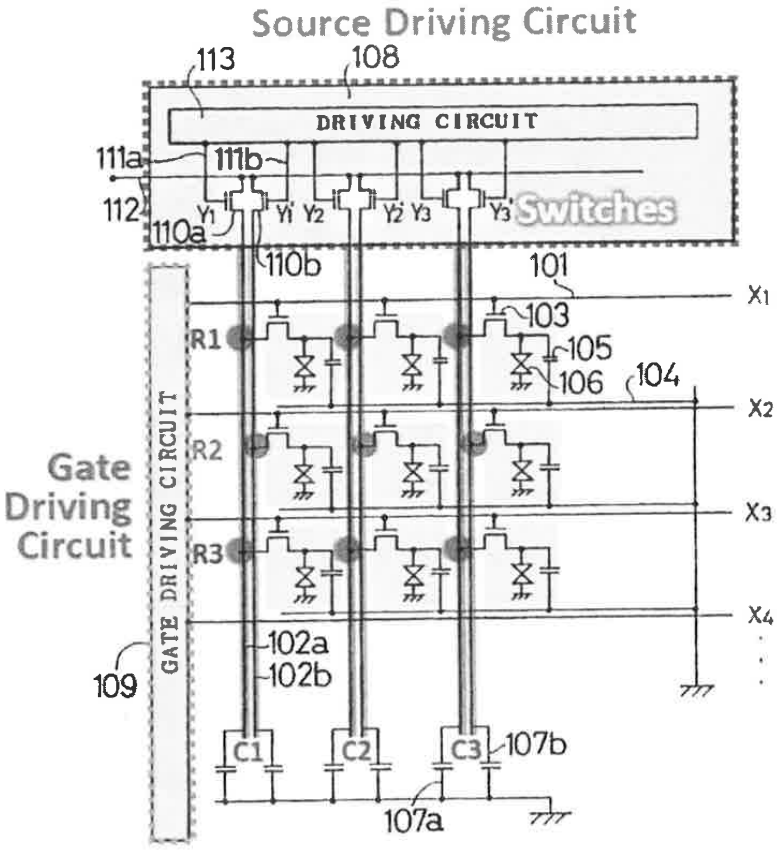
162. As explained below, it is my opinion that Claims 1-5 of the '550 Patent are also obvious over Shimada in view of Kamizono.

SHIMADA

163. As shown below in annotated Figure 4, Shimada teaches an LCD device comprising a matrix array of thin film transistors (TFTs) 103, which drive the corresponding array of pixels 106. (Ex. 1003, Shimada, Col. 4:31-63, Fig. 4).

164. Like the Sharp Reference and Kamizono, Shimada addresses the technical problems arising from increasing the size of the LCD panel and the number of pixels, such as line delay. (*Id.* at Cols. 2:35-3:63). Shimada states that its object is to "reduce the effect of signal delay on display quality" of the LCD device, thereby improving image quality. (*Id.* at Col. 2:66-67).

Shimada Fig. 4



165. As shown in Figure 4, a group of gate bus lines 101 (X_1, X_2, X_3, . . .) is connected to the gate driving circuit 109, and each gate bus line is connected with the gates of all of the TFTs 103 in the row associated with that gate bus line. For example, the first gate line X_1 is connected with the gates of all of the TFTs 103 of the first row (R1), the

second gate line X_2 is connected with the gates of all of the TFTs 103 of the second row (R2), etc. (*Id.* at Col. 4:31-40, Fig. 4).

166. Shimada also teaches that the gate bus lines 101 (X_1, X_2, X_3, . . .) are spaced apart from and parallel to each other (i.e., insulated with each other). (*Id.*, Fig. 4).

167. Figure 4 also shows groups of data bus lines 102a, 102b (the red and green lines) connected to the ***same*** source driving circuit 108. I understand that this was the basis for allowance of Claim 1 by the Patent Office. Figure 4 also shows that the data bus lines (e.g., 102a, 102b) are spaced apart from and parallel to each other (i.e., insulated with each other). (*Id.*, Col. 4:31-40, Fig. 4).

168. As shown above in Figure 4 of Shimada, the first data bus line 102a (red line) and the second data bus line 102b (green line) in each group of data bus lines are respectively connected with the sources of all of the TFTs 103 of the **odd rows** (red boxes in R1 and R3) and **even rows** (green boxes in R2) of the column (C1, C2, C3) associated with that group of data bus lines, as required Claims 1-5 of the '550 Patent.

169. For example, the first data bus line 102a (red line) of the first group is connected with the sources (red dots) of the TFTs 103 of the first row and third row (see the red boxes in R1 and R3) in the first column (C1), while the second data bus line 102b (green line) of the first group is connected with the sources (green dot) of the TFT 103 of the second row (green box in R2) in the first column (C1). (*Id.* at Col. 4:41-63, Fig. 4). The same Odd Row/Even Row configuration is provided in each column (e.g., C2 and C3).

170. Shimada teaches that this Odd Row/Even Row configuration reduces the effect of signal delay caused by the increased number of pixels, thereby improving the video quality of the display of a larger-sized LCD panel. (*Id.* at Cols. 2:34-3:2, Col. 5:49-66).

171. As shown in Figure 4, the source driving circuit 108 for all data bus lines is installed on the same side (e.g., upper side) of the display panel.

172. Figure 4 also shows that the transfer of video signals from the video signal line 112 to the first and the second data bus lines 102a, 102b is switched by the switches 110a, 110b. (*Id.* at Col. 4:41-51, Fig. 4).

IT WOULD HAVE BEEN OBVIOUS TO COMBINE SHIMADA'S LCD DEVICE WITH KAMIZONO'S TEACHING OF MULTIPLE SOURCE AND GATE DRIVERS

173. The LCD device of Shimada discloses all of the key elements of Claims 1-3 of the '550 Patent, including the Odd Row/Even Row configuration.

174. Kamizono discloses source drivers 5 and gate drivers 6. (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).

175. As discussed below, I believe that it would have been obvious to a person of ordinary skill in the art at the time the '550 Patent was filed to combine the teachings of Shimada and Kamizono to arrive at the LCD driving device of Claims 1-3.

176. Shimada and Kamizono are in the same field of LCD display technology. They both disclose active matrix LCD devices and are both directed to improving the performance of a large screen LCD panel. Shimada states that increasing the number of pixels causes undesirable line delay and teaches the Odd Row/Even Row configuration in a

larger sized LCD device to reduce the effect of signal delay on display quality of the LCD device. (Ex. 1003, Shimada, Cols. 2:35-3:63). Kamizono teaches that a "large-screen" LCD panel uses more source and gate driver LSIs than a "small sized" LCD panels would use. (Ex. 1004, Kamizono, Col. 9:19-20, Col. 11:53-64, FIGS. 5 and 9). Because both references addressed the same design need for larger sized LCD panels, I believe that a person of ordinary skill in the art making the source and gate driving circuit for a large-screen LCD panel would have been motivated to combine the teachings of Shimada and Kamizono to arrive at Claims 1-3.

177. Based on my experience and knowledge, I believe that modifying the LCD driving device of Shimada to include the multiple source and gate driver ICs of Kamizono would not produce unexpected results, since such a modification simply allows more pixels to be added to increase the size of the LCD panel. This modification would not change the way Shimada's LCD panel operates in the Odd Row/Even Row configuration.

178. In addition, I believe that a person of ordinary skill in the art would recognize that Kamizono's technique of including multiple source and gate drivers to improve a large screen LCD panel can also be used to improve the large screen LCD panel of Shimada in the same way. This would be well within the level of ordinary skill in the art.

179. Indeed, the prior art was replete with examples of larger sized LCD panels using multiple source and gate drivers. In fact, when I was working in the LCD industry prior to the filing date of the '550 Patent, it was a routine industry practice to change the panel

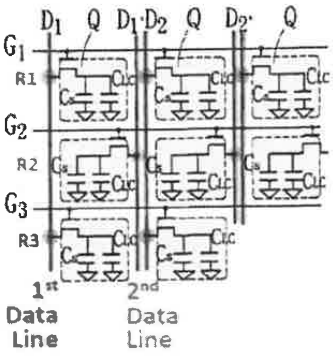
design to increase the size of the panel and/or the number of pixels by simply adding more driver ICs. For example, while the ***small***, low cost LCD panel (which had an equivalent pixel dimension of 7×4) that I worked on at Alien Technology had only a single source driver and a single gate driver, the ***large sized*** LCD panels (which had pixel dimension of at least 800×600) that I worked on at Philips used multiple driver ICs. Using additional source and gate drivers in connection with increasing the size of the panel or the number of pixels in an LCD panel was a well-known and readily available design option.

180. Consistent with my experience, the prior Sekido reference (Ex. 1009) states that "in order to drive many gate bus lines and the source bus lines on the display circuit board, ***a plurality of the gate drivers and source drivers must*** be connected to the area around the liquid crystal display panel." (Ex. 1009, Sekido, Par. [0006]) (emphasis added). This prior art further teaches that increasing the size of the LCD screen will increase the number of the driver ICs. (*Id.*, Par. [0008]).

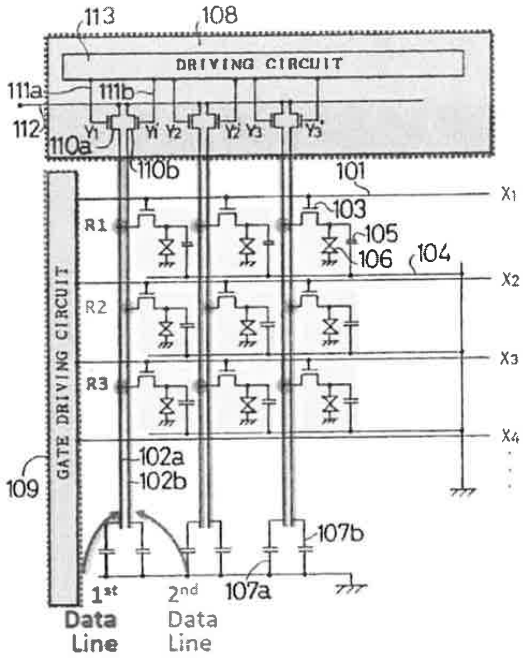
181. Accordingly, I believe that it would have been obvious to a person of ordinary skill in the art to modify the LCD driving device of Shimada to include the multiple source and gate drivers shown in Kamizono and connect them to the data lines (e.g., 102a, 102b) and the gate lines (X_1, X_2, X_3, X_4) of Shimada, respectively.

182. Moreover, as discussed below, Shimada teaches all of the other limitations of Claims 1 and 2 of the '550 Patent.

'550 Patent Fig. 4B



Shimada Fig. 4



SHIMADA DISCLOSES THE ODD ROW/EVEN ROW CONFIGURATION

183. As shown above in annotated Figure 4, Shimada discloses the claimed Odd Row/Even Row configuration of the '550 Patent (shown on the left). (Ex. 1003, Shimada, Col. 4:41-63, Fig. 4).

184. Specifically, the first data line 102a (see the red line) is connected to the sources (red dots) of the TFTs (red boxes) in the odd rows (R1 and R3). The second data line 102b (green line) is connected to the sources (green dot) of the TFTs (green boxes) in the even rows (R2). Figure 4B of the later '550 Patent has the same Odd Row/Even Row configuration.

185. Like the '550 Patent, Shimada teaches that this Odd Row/Even Row configuration reduces the effect of signal delay on the quality of the display, thereby improving image quality. (*Id.* at Cols. 2:66-3:2).

SHIMADA DISCLOSES THAT FIRST AND SECOND DATA LINES IN EACH GROUP OF DATA LINES ARE CONNECTED WITH THE SAME SOURCE DRIVER

186. As shown above in Figure 4 of Shimada, the first and second data lines (e.g., 102a (red line) and 102b (green line)) in each group of data lines in are connected with the ***same*** source driver 108 (*Id.* at Col. 4:41-51, Fig. 4), as required by Claims 1 and 2. I understand that this was the basis for allowance of Claim 1 during prosecution.

SHIMADA DISCLOSES THAT EACH SOURCE DRIVER IS INSTALLED ON THE SAME SIDE OF THE DISPLAY PANEL

187. As shown above in Figure 4 of Shimada, each source driver 108 is installed on the same side of the display panel (*id.* at Col. 4:41-46, Fig. 4), as required by independent Claim 2.

SHIMADA DISCLOSES AN ELECTRONIC SWITCH FOR DATA TRANSFER

188. As shown above in Figure 4 of Shimada, data transfer is switched by an electronic switch 110a, 110b (*id.*), as required by independent Claim 2.

SHIMADA DISCLOSES THAT GATE LINES/DATA LINES ARE INSULATED WITH EACH OTHER

189. In addition, Shimada teaches that the gate lines 101 (X_1, X_2, X_3, . . .) are "insulated with each other" under the broadest reasonable construction since they are shown to be spaced apart from and parallel to each other. Likewise, Shimada teaches that

the data bus lines (e.g., 102a, 102b) are insulated with each other as they are spaced apart from and parallel to each other. (*Id.* at FIG. 4).

190. Because Shimada and Kamizono combine to disclose all of the elements of Claims 1 and 2, and further because there was a clear motivation for a person of ordinary skill in the art to combine these references, I believe that Claims 1 and 2 are obvious over Shimada in view of Kamizono.

SHIMADA DISCLOSES A SPACE BETWEEN THE NEIGHBORING DATA LINE TO PREVENT SHORT CIRCUITING

191. Claim 3, which depends from Claim 2, recites that "there is a space [i.e., a gap] between the neighboring data lines to prevent them from short circuit." Figure 4 of Shimada clearly shows that there is a space between the neighboring data lines (e.g., between 102a and 102b) that prevents short circuiting.

192. When two neighboring data lines are shown to be spaced apart from each other in the schematic circuit diagram for an LCD driving device, such as Figure 4 of Shimada, I expect that there is a sufficient space between these data lines to prevent short circuiting. Otherwise, the LCD driving device would not be operating as described in the reference.

KAMIZONO DISCLOSES A CHIP ON GLASS

193. Dependent Claim 4 requires that the gate driver is a chip installed on glass.

194. Kamizono teaches that the use of a chip-on-glass is the preferred way of implementing the gate drivers for a large sized LCD panel. (Ex. 1004, Kamizono, Col. 1:12-58).

195. Shimada and Kamizono are in the same field of LCD display technology. They both disclose active matrix LCD devices and are both directed to improving the performance of a large screen LCD panel. Shimada states that increasing the number of pixels causes undesirable line delay and teaches the Odd Row/Even Row configuration in a ***larger sized*** LCD device to reduce the effect of signal delay on display quality of the LCD device. (Ex. 1003, Shimada, Cols. 2:35-3:63). Kamizono teaches that a "large-screen" LCD panel uses more source and gate driver LSIs than a "small sized" LCD panels would use. (Ex. 1004, Kamizono, Col. 9:19-20, Col. 11:53-64, FIGS. 5 and 9). Because both references addressed the same design need for larger sized LCD panels, I believe that a person of ordinary skill in the art making the gate drivers for a large-screen LCD panel would have been motivated to combine the teachings of Shimada and Kamizono to arrive at Claim 4.

196. Based on my experience and knowledge, I believe that using the chip on glass of Kamizono for the gate driver in the LCD device of Shimada would not produce any unexpected result and would not affect, for example, the Odd Row/Even Row configuration in Shimada's LCD device.

197. Based on my experience and knowledge, I believe that a person of ordinary skill in the art would recognize that Kamizono's technique of using a chip on glass for the gate driver to improve a large screen LCD panel (e.g., increasing the operational reliability and reducing the overall product size) can be also used to improve the large screen LCD panel of Shimada in the same way.

198. Accordingly, a person of ordinary skill in the art making a large-screen LCD panel would have been motivated to combine the teachings of Shimada and Kamizono to arrive at Claim 4.

199. Accordingly, it is my opinion that Claim 4 is also obvious over Shimada in view of Kamizono.

KAMIZONO DISCLOSES INTEGRATED GATE DRIVER CIRCUIT

200. Claim 5 requires that the gate driver is an integrated gate driver circuit installed on glass.

201. Kaminozo teaches that an LCD panel can be a poly-Silicon TFT panel and the source and gate drivers can be mounted on the panel in a spare area other than the display area of the panel (i.e., forming an integrated structure with the LCD panel). (Ex. 1004, Kamizono, Col. 13:50-55). Since the gate drivers are formed on the same substrate as the pixel TFTs, the result is integrated gate driver circuit installed on the same substrate as the pixel TFTs.

202. Moreover, as discussed above, it was well-known at the time of the filing date of the '550 Patent that an LCD panel must include a glass substrate or other substantially transparent substrate to transmit the light from the backlight to the LCD viewer's eyes. LCD panels modulate the light generated by the backlight assembly and passed through the glass substrate (or other transparent substrate) according to the TFT drive signals. The light exits the LCD surface nearest the viewer and allows the viewer to see the visual image generated based on the electrical input signal.

203. The use of a glass substrate was the preferred choice, especially in an LCD panel having a large number of pixels. Compared to other transparent materials, glass is cheaper, provides a smoother surface, and is also more resistant to a high temperature required for processing TFTs in an LCD panel. In addition, a glass substrate protects liquid crystal materials and TFTs in the LCD panel from moisture. In my experience, LCD panels with a large number of pixels using TFTs all included glass substrates.

204. Thus, I believe that it would have been obvious to a person of ordinary skill in the art that the integrated gate driver circuit taught by Kamizono is installed on a glass substrate in an LCD panel since the use of glass substrate is one of small number of widely known design options to make an LCD panel and to have the light transmitted from the backlight.

205. As discussed above, because Shimada and Kamizono addressed the same design need for larger sized LCD panels, I believe that a person of ordinary skill in the art

making the gate drivers for a large-screen LCD panel would have been motivated to combine the teachings of Shimada and Kamizono to arrive at Claim 5.

206. Based on my experience and knowledge, I believe that using the integrated gate driver circuit on glass of Kamizono for the gate driver in the LCD device of Shimada would not produce any unexpected result and would not affect, for example, the Odd Row/Even Row configuration in Shimada's LCD device.

207. Accordingly, it is my opinion that Claim 5 of the '550 Patent is also obvious over Shimada in view of Kamizono.

THE COMBINATION OF SHIMADA AND KAMIZONO TEACHES ALL ELEMENTS OF CLAIMS 1-5

208. The following claim charts summarize where I believe each element of Claims 1-5 is taught by the combination of Shimada and Kamizono:

The Claims Of The '550 Patent	Shimada in View of Kamizono
1. A liquid crystal display driving device of matrix structure type including:	Shimada discloses a liquid crystal display driving device of matrix structure type (Ex. 1003, Shimada, Col. 1:8-10, Col. 4:31-67, Figs. 4, 7).
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels can be driven;	Shimada discloses a group of thin film transistors 103 with matrix array consisting of N (e.g., 3) rows and M (e.g., 3) columns of thin film transistors 103, wherein each thin film transistor can drive one pixel 106 so that N×M of pixels can be driven (Ex. 1003, Shimada, Col. 4:31-63, Fig. 4).
a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the	Shimada discloses a group of N gate lines 101 (e.g., X_1, X_2, X_3, . . .) connected to the gate driver (e.g., gate driving circuit 109) and insulated with each other by being spaced apart

The Claims Of The '550 Patent	Shimada in View of Kamizono
thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	from and parallel to each other. The first gate line X_1 is connected with the gates of all the thin film transistors 103 of the first row. The second gate line X_2 is connected with the gates of all the thin film transistors 103 of the second row . . . and the N^{th} gate line X_N is connected with the gates of all the thin film transistors 103 of the N^{th} row. (Ex. 1003, Shimada, Col. 4:31-40, Figs. 4, 7). Kamizono discloses scanning lines 4 connected to multiple scanning line driving LSIs 6 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).
M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column, and	Shimada discloses M (e.g., 3) groups of data lines 102a, 102b connected to the source driver (e.g., the source driving circuit 108) and insulated with each other by being spaced apart from and parallel to each other. The first and the second data lines 102a, 102b of the first group of data lines are respectively connected with the sources of all the thin film transistors 103 of the odd and the even rows of the first column. The first and the second data lines 102a, 102b of the second group of data lines are respectively connected with the sources of all the thin film transistors 103 of the odd and the even rows of the second column . . . and the first and the second data lines 102a, 102b of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors 103 of the odd and the even rows of the M^{th} column (Ex. 1003, Shimada, Col. 4:41-63, Fig. 4). Kamizono discloses signal lines 3 connected to multiple signal line driving LSIs 5 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).

The Claims Of The '550 Patent	Shimada in View of Kamizono
the first data lines and the second data lines of each group of data lines are connected with the same source driver.	Shimada discloses that the first data lines 102a and the second data lines 102b of each group of data lines are connected with the same source driver 108 (Ex. 1003, Shimada, Col. 4:41-63, Fig. 4; *compare with* Ex. 1001, '550 Patent, Fig. 6A).
2. The liquid crystal display device of matrix structure type including:	Shimada discloses a liquid crystal display driving device of matrix structure type (Ex. 1003, Shimada, Col. 1:8-10, Cols. 4:31-5:15, Figs. 4, 7).
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels can be driven;	Shimada discloses a group of thin film transistors 103 with matrix array consisting of N (e.g., 3) rows and M (e.g., 3) columns of thin film transistors 103, wherein each thin film transistor can drive one pixel 106 so that N×M of pixels can be driven (Ex. 1003, Shimada, Col. 4:31-63, Fig. 4).
a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	Shimada discloses a group of N gate lines 101 (e.g., X_1, X_2, X_3, . . .) connected to the gate driver (e.g., gate driving circuit 109) and insulated with each other by being spaced apart from and parallel to each other. The first gate line X_1 is connected with the gates of all the thin film transistors 103 of the first row. The second gate line X_2 is connected with the gates of all the thin film transistors 103 of the second row . . . and the N^{th} gate line X_N is connected with the gates of all the thin film transistors 103 of the N^{th} row (Ex. 1003, Shimada, Col. 4:31-40, Figs. 4, 7). Kamizono discloses scanning lines 4 connected to multiple scanning line driving LSIs 6 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).
M groups of data lines connected to the source drivers and insulated with	Shimada discloses M (e.g., 3) groups of data lines 102a, 102b connected to the source driver

The Claims Of The '550 Patent	Shimada in View of Kamizono
each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column,	(e.g., the source driving circuit 108) and insulated with each other by being spaced apart from and parallel to each other. The first and the second data lines 102a, 102b of the first group of data lines are respectively connected with the sources of all the thin film transistors 103 of the odd and the even rows of the first column. The first and the second data lines 102a, 102b of the second group of data lines are respectively connected with the sources of all the thin film transistors 103 of the odd and the even rows of the second column . . . and the first and the second data lines 102a, 102b of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors 103 of the odd and the even rows of the M^{th} column (Ex. 1003, Shimada, Col. 4:41-63, Fig. 4). Kamizono discloses signal lines 3 connected to multiple signal line driving LSIs 5 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).
Wherein the first data lines and the second data lines of each group of data lines are connected with the same source driver,	Shimada discloses that the first data lines 102a and the second data lines 102b of each group of data lines are connected with the same source driver 108 (Ex. 1003, Shimada, Col. 4:41-63, Fig. 4; *compare with* Ex. 1001, '550 Patent, Fig. 6A).
each source driver is installed on the same side of the display panel and	Shimada discloses that each source driver 108 is installed on the same side (e.g., upper side) of the display panel (Ex. 1003, Shimada, Col. 4:41-46, Fig. 4).
The data transfer is switched by an electronic switch.	Shimada discloses that the data transfer is switched by an electronic switch 110a, 110b (Ex. 1003, Shimada, Col. 4:41-46, Fig. 4).

The Claims Of The '550 Patent	Shimada in View of Kamizono
3. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein there is a space between the neighboring data lines to prevent them from short circuit.	Shimada discloses that there is a space between the neighboring data lines 102a, 102b (Ex. 1003, Shimada, Figs. 4, 7).
4. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein the gate driver is a chip installed on glass.	Kamizono discloses that a liquid crystal driving LSI is commonly mounted as a semiconductor chip by a chip-on-glass (COG) method. (Ex. 1004, Kamizono, Col. 1:12-58).
5. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein the gate driver is an integrated gate driver circuit installed on glass.	Kamizono discloses LCD driving circuits that form an integrated structure with a poly-Silicon TFT panel. (Ex. 1004, Kamizono, Col. 13:50-55).

209. Accordingly, it is my opinion that Claims 1-5 of the '550 Patent are also obvious over Shimada in view of Kamizono.

210. At this time I am not aware of any arguments and evidence of "secondary considerations" that would render the claims of the '550 Patent non-obvious with respect to my opinions set forth herein on the issue of obviousness. Should Patent Owner present such evidence, I reserve the right to respond to such evidence and arguments.

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: March 20, 2015

By: Michael J. Marentic

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(54) **DRIVE CIRCUIT DEVICE FOR DISPLAY DEVICE, AND DISPLAY DEVICE USING THE SAME**

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(51) **Int. Cl.**[7] **G09G 3/36**

(52) **U.S. Cl.** **345/98**

(57) **ABSTRACT**

A drive circuit device for a display device which drives a plurality of source bus lines provided on a display panel, the drive circuit device comprises: a driver unit(**20**) that receives a clock signal, a data signal and a control signal, and sequentially fetches the data signal, and generates drive signals for the source bus lines in accordance to the fetched data signal; and a gate unit(**22**) that, after elapse of specified time from the reception of the driver unit, and at a timing when a rear-stage drive circuit device starts receiving, starts outputting of a propagation signal including at least one of the clock signal, data signal and control signal to the rear-stage drive circuit device. Consequently, the power consumption required for supplying these signals and the generated amount of electromagnetic waves resulting from the signal supply can be suppressed.

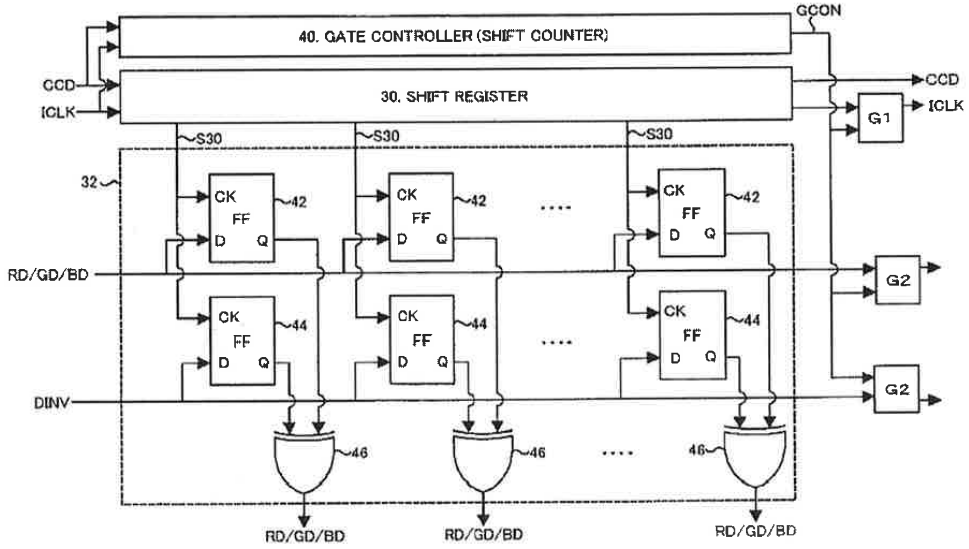


FIG. 1

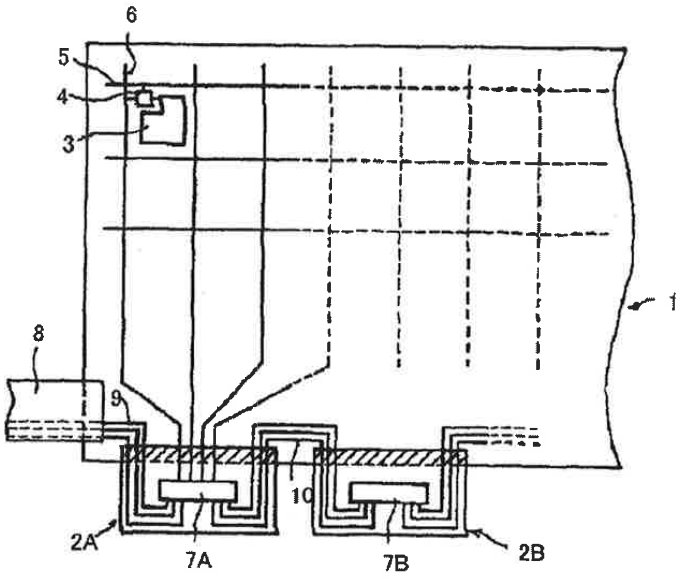
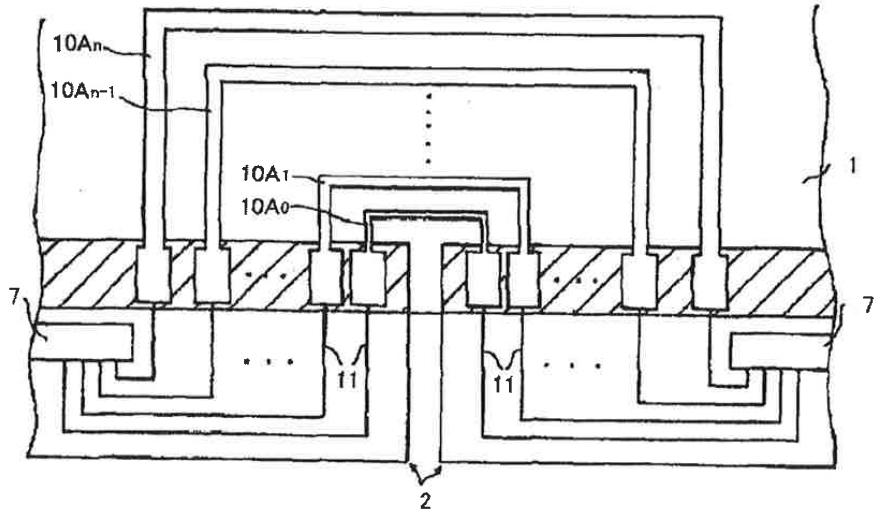


FIG. 2



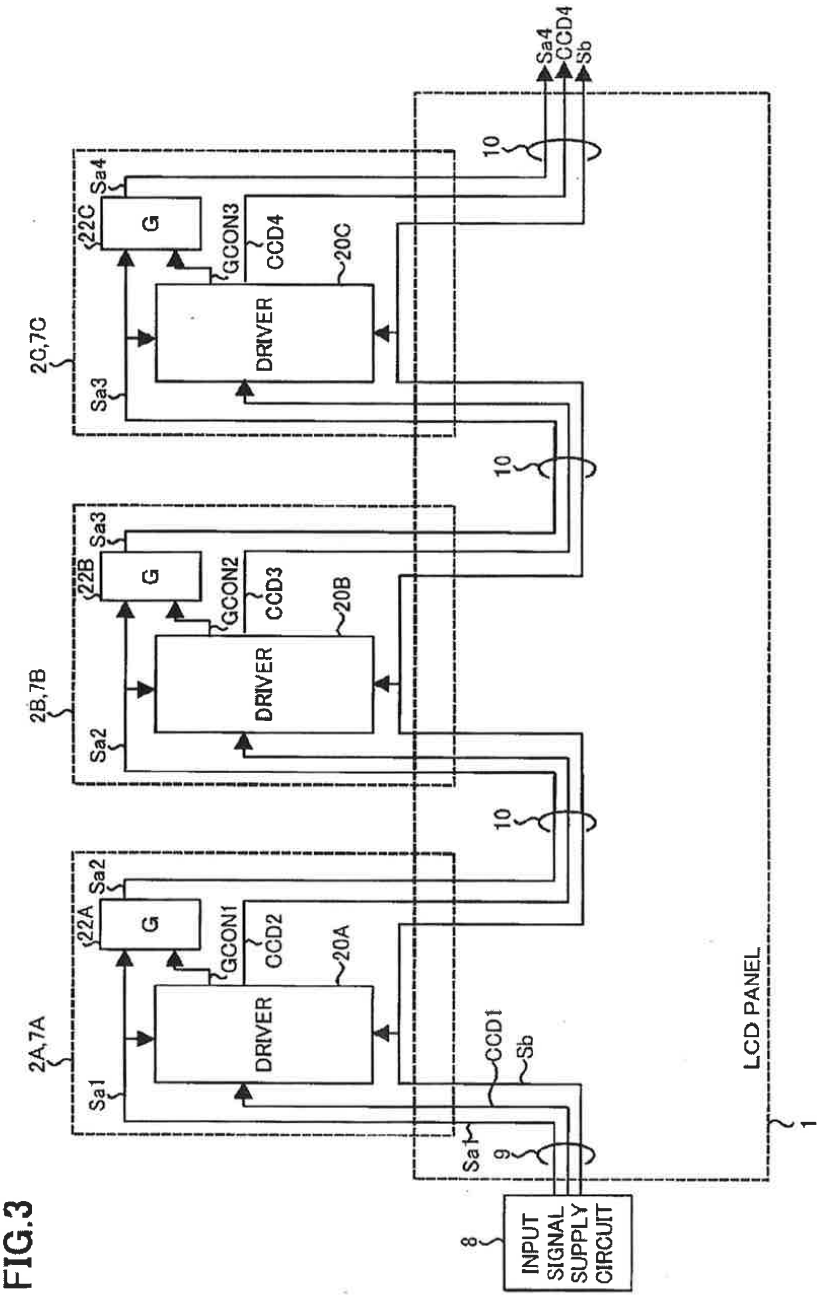


FIG.3

FIG. 4

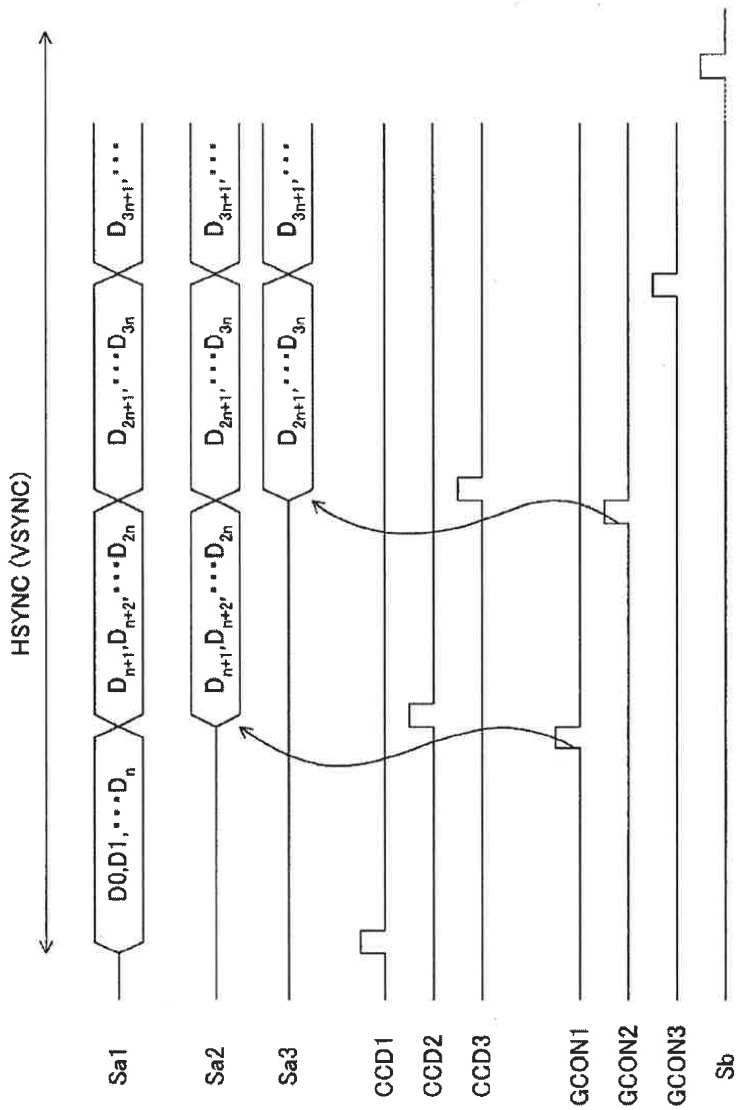
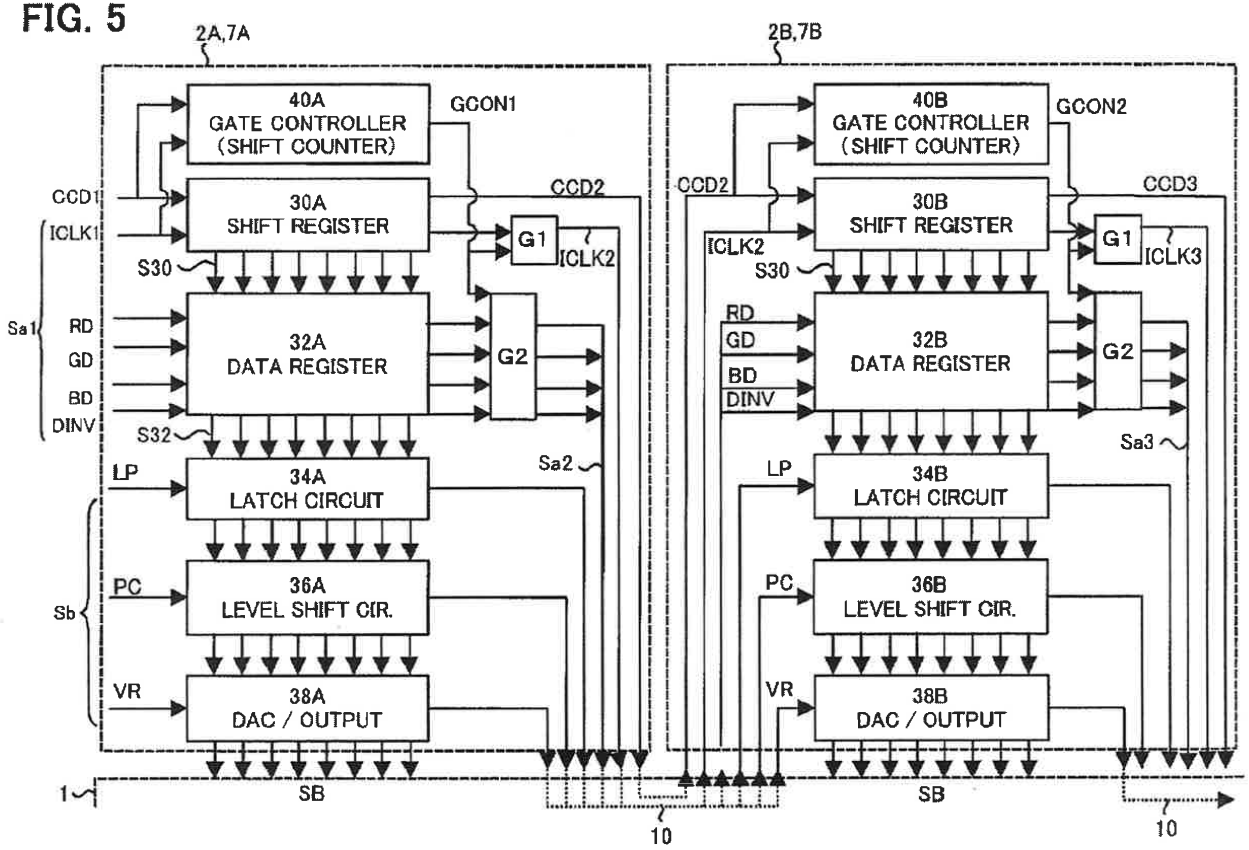


FIG. 5



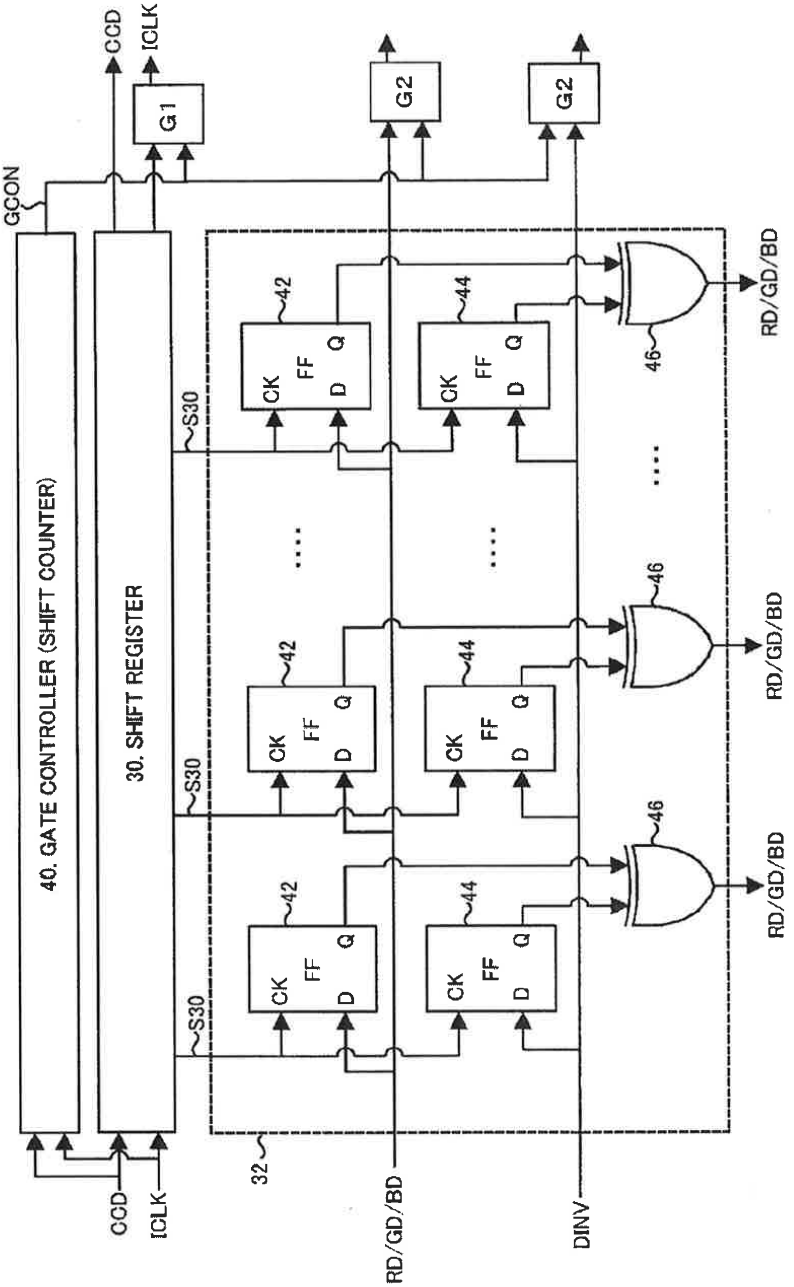
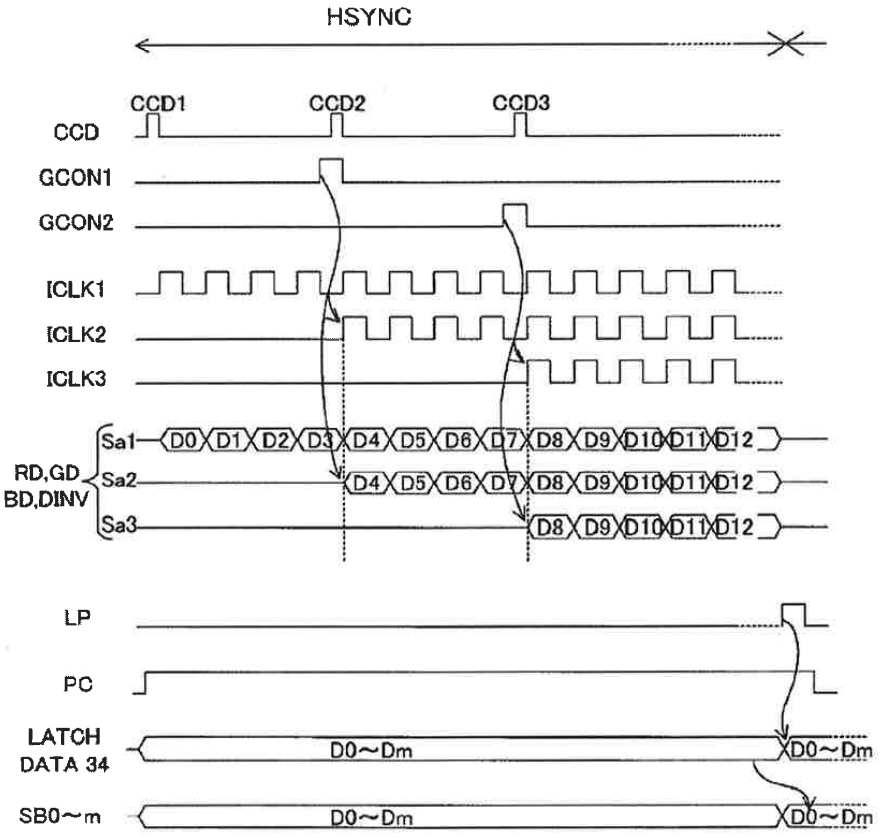


FIG. 6

FIG. 7



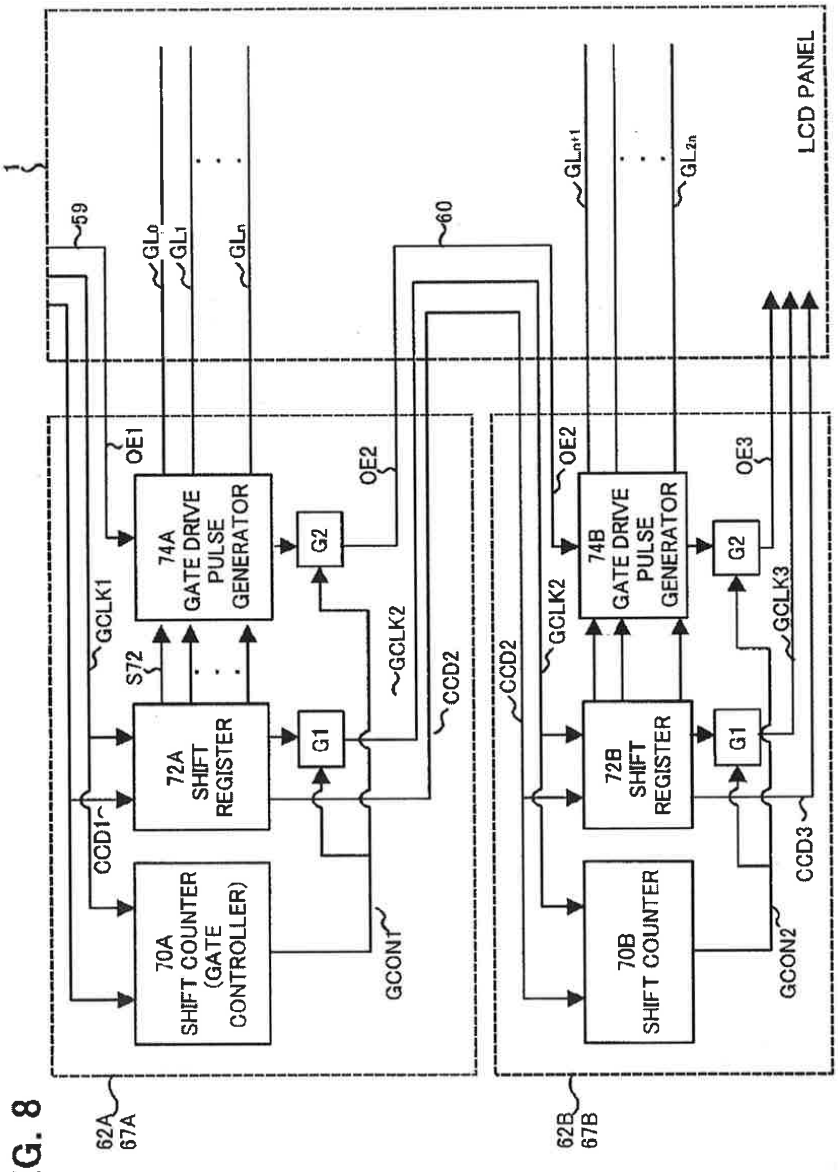
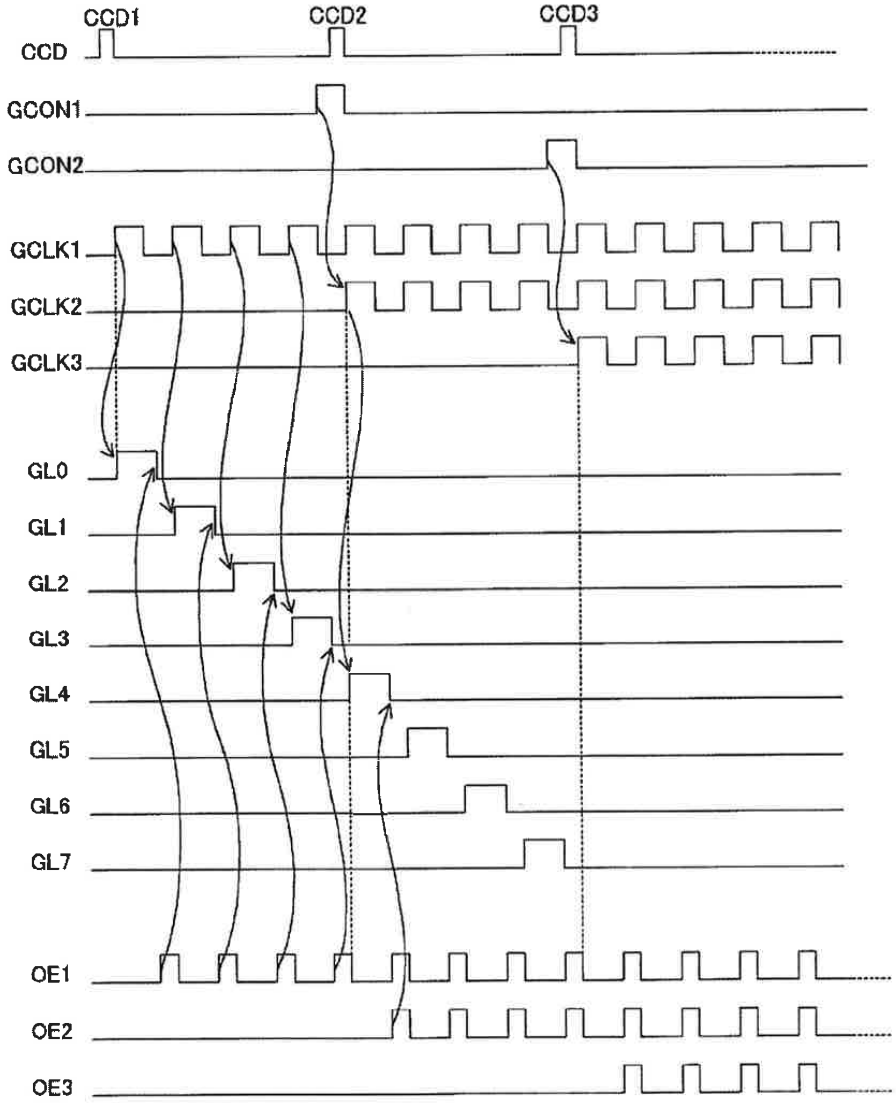


FIG. 8

FIG. 9



DRIVE CIRCUIT DEVICE FOR DISPLAY DEVICE, AND DISPLAY DEVICE USING THE SAME

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates generally to a drive circuit device for a display device such as a liquid crystal display device, and more particularly, to a drive circuit device that can reduce power consumption and suppress occurrence of electromagnetic waves.

[0003] 2. Description of the Related Art

[0004] The liquid crystal display device is now widely being used for the monitor screen of a computer, etc., because of its space-saving feature. In recent years, a larger type is further being called for, and development of structure to meet the requirement is increasingly being made.

[0005] Of the liquid crystal display devices, a liquid crystal display device of an active-matrix type has pixels in a matrix arrangement, using active elements, like TFTs (tin film transistors). This liquid crystal display device has pixel electrodes and a common electrode on a liquid crystal display panel or substrate, and a liquid crystal layer between them. Further, the liquid crystal display panel has source bus lines and gate bus lines, which cross each other, and TFTs provided at the crossing positions. And, by driving the gate bus lines to cause the TFTs of the pixels located in the row direction to a conductive state, and applying voltage corresponding to the half tone of the pixel to each source bus line, the voltage corresponding to the half tone of the pixel is applied between the pixel electrode and the common electrode. As the result of the application of voltage, the liquid crystal layer between the pixel electrode and the common electrode has a transmission factor corresponding to the applied voltage, thereby allowing a reproduction of an expected half tone to be possible.

[0006] In order to perform such display operations, a gate driver which sequentially drives the gate bus lines, and a source driver which drives the source bus lines simultaneously with the voltage corresponding to the displayed data, are connected to the liquid crystal display panel. The gate driver and the source driver will be embodied by an integrated circuit device, and each of the drivers drives a plurality of gate bus lines or a plurality of source bus lines, respectively. Therefore, in order to drive many gate bus lines and the source bus lines on the display circuit board, a plurality of the gate drivers and source drivers must be connected to the area around the liquid crystal display panel.

[0007] With the requirement for space saving, the downsizing of the liquid crystal display device seems to be the current trend, but, on the other hand, to meet the request for larger size of the monitor screen, a space for packing the gate driver and the source driver is becoming limited. With this limitation, signal lines for the data signal, clock signal or control signal to be supplied to the plurality of the source drivers and the gate drivers are formed on an LCD panel, on which TFT source bus lines and gate bus lines for the liquid crystal display panel are installed.

[0008] Unlike a printed circuit board, the signal lines to be formed on the liquid crystal display panel has relatively higher resistance and capacitance compared with a printed circuit board, and cannot be covered with a ground wiring layer. For this reason, when pulse signal with high frequency is applied to these signal lines, a lot of power is consumed to drive these signal lines, and a strong electromagnetic wave will be sent out along with the driving. Especially, along the upsizing of the screen, the number of the driver Ics will be increased, and further, the signal lines for propagating the data signal, clock signal, or control signal becomes longer, so that the power consumption and occurrence of electromagnetic wave is considerably increased.

SUMMARY OF THE INVENTION

[0009] It is therefore the object of the present invention to provide a drive circuit device for a display device that can suppress power consumption and occurrence of electromagnetic waves, and a display device using the same.

[0010] In order to attain the above objects, an aspect of the present invention provides a drive circuit device for a display device which drives a plurality of source bus lines provided on a display panel, the drive circuit device comprising: a driver unit that receives a clock signal, a data signal and a control signal, and sequentially fetches the data signal, and generates drive signals for the source bus lines in accordance to the fetched data signal; and a gate unit that, after elapse of specified time from the reception of the driver unit, and at a timing when a rear-stage drive circuit device starts receiving, starts outputting of a propagation signal including at least one of the clock signal, data signal and control signal to the rear-stage drive circuit device.

[0011] In order to achieve the above objects, another aspect of the present invention provides a drive circuit device for a display device which sequentially drives a plurality of gate bus lines provided on a display panel, the drive circuit device comprising: a driver unit that receives a clock signal and a control signal, and sequentially generates a drive signal for the gate bus lines, in synchronism with the clock signal; and a gate unit that, after elapse of specified time from the reception of the driver unit, and at a timing when a rear-stage drive circuit device starts receiving, starts outputting of a propagation signal including at least one of the clock signal and control signal to the rear-stage drive circuit device.

[0012] According to the present invention, a drive circuit device on a front stage receives the clock signal, data signal and control signal for generating the drive signal, and output at least one signal of these signals at a timing when a drive circuit device on a rear stage starts receiving these signals. Therefore, when a plurality of drive circuit devices are provided in serial on a display panel, and a clock signal, data signal, control signal, etc. are to be sequentially received by the plurality of the drive circuit devices, these signals will not be supplied to any drive circuit device on a rear stage of the drive circuit device which is currently receiving signals. Consequently, the power consumption required for supplying these signals and the generated amount of electromagnetic waves resulting from the signal supply can be suppressed, compared with the case of supplying these signals to all drive circuit devices.

[0013] In a more preferred embodiment, in the display device, a plurality of the drive circuit devices are connected in serial, and the drive circuit devices are connected to a display panel. Even if the display panel becomes larger, and

the number of drive circuit devices increases, the power consumption and generated amount of electromagnetic waves can be suppressed, because propagating signals, like a clock signal, will only be supplied to the drive circuit devices, from the initial stage through the necessary stage according to the drive circuit devices as described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] **FIG. 1** shows a configuration of a liquid crystal display device in the embodiment of the present invention;

[0015] **FIG. 2** shows an enlarged view of the joint section between a drive circuit device circuit board **2** and a display panel **1**;

[0016] **FIG. 3** shows a configuration of a drive circuit device and a display panel in the embodiment of the present invention;

[0017] **FIG. 4** is an operation-timing chart of the drive circuit device shown in **FIG. 3**;

[0018] **FIG. 5** shows a configuration of a source side drive circuit device;

[0019] **FIG. 6** shows a configuration of a data register in the source side drive circuit device;

[0020] **FIG. 7** is an operation-timing chart of the source side drive circuit device;

[0021] **FIG. 8** shows a configuration of a gate side drive circuit device; and

[0022] **FIG. 9** is an operation flowchart of the gate side drive circuit device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0023] Embodiments of the present invention will now be described with reference to the drawings. It is however to be understood that the protective scope of the present invention is not limited to the embodiments shown below, but that it covers up to the invention defined by claims and its equivalents.

[0024] **FIG. 1** shows a configuration of a liquid crystal display device in the embodiment. A display panel **1** has a TFT substrate forming TFTs, a common electrode substrate forming a common electrode, and a liquid crystal layer to be provided between them. Out of these components, a configuration of the TFT substrate is shown in **FIG. 1**. That is to say, on the display panel **1**, pixel electrodes **3** are arranged in a matrix pattern, and corresponding to this matrix arrangement, a plurality of gate bus lines **5** and a plurality of source bus lines **6**, crossing the gate bus lines, are provided, and further, TFTs **4** are provided at the intersections respectively. And, when the gate bus line **5** is driven, the TFT**4** connected to the gate bus line and located in the row direction will be brought into conduction, and the voltage applied to each of the source bus lines **6** will be supplied to the pixel electrode **3**. As the result of this operation, the voltage corresponding to the display data will be applied to the liquid crystal layer between the common electrode, though not noted in the drawing, and the respective pixel electrodes **3**, and the liquid crystal layer can demonstrate an expected transmission factor.

[0025] To the peripheral area of the display panel **1**, circuit boards **2**A and **2**B, mounting a drive circuit device **7**A or **7**B, respectively, to drive the source bus lines **6**, are connected. Moreover, a printed circuit board **8** mounting an input signal supply circuit to supply a clock signal, data signal, control signal or other signals to the drive circuit devices **7**A and **7**B is connected to the peripheral area of the display panel **1**. And, the clock signal, data signal, control signal or other signals outputted from the printed circuit board **8** are supplied to the drive circuit device circuit board **2**A on the initial stage, through an input wiring **9** on the display panel **1**, and further are supplied to a drive circuit device **7**A on the initial stage, through wiring of the drive circuit device circuit board **2**A.

[0026] Moreover, the drive circuit device **7**A on the initial stage supplies the clock signal, data signal and control signal to the drive circuit device circuit board **2**B on the next stage, through a connection wiring **10** on the display panel **1**, and a drive circuit device **7**B on the circuit board **2**B receives these signals. And, the second drive circuit device **7**B supplies the clock signal, data signal and control signal to drive circuit devices on the following stages, though not shown in the drawing.

[0027] As described above, the propagation signals, like the clock signal, data signal, control signal, or other signals outputted from the printed circuit board **8** of the input signal supply circuit are supplied to the plurality of the drive circuit devices **7**A and **7**B connected in tandem, through the connection wiring **10** on the display panel **1**.

[0028] Each of the drive circuit devices **7**A and **7**B generates drive signals for the source bus lines, corresponding to the data signal and control signal inputted synchronizing with the clock signal. And, in the timing after all the drive circuit devices **7**A and **7**B sequentially input the corresponding data signal, the drive circuit devices **7**A and **7**B drive the corresponding source bus lines **6** simultaneously. Synchronizing with this drive, a drive circuit device on the gate side, which is not shown in the drawing, drives one of the gate bus lines **5**, and the voltage applied to the respective source bus lines **6** is applied to the pixel electrodes **3** through the TFT **4**.

[0029] **FIG. 2** shows an enlarged view of the joint section between the drive circuit device circuit board **2** and the display panel substrate **1**. On the surface of the display panel **1**, a connection wiring **10**A is provided, and wirings **11** on the circuit board **2** mounting a drive circuit IC**7** and the connection wiring **10**A are connected at the joint section shown in the diagonally shaded area. The connection wirings **10**A are formed so that the wiring width becomes wider and wider toward the outer side, so that delay of the signal transmittal of each wiring can be equal.

[0030] On the other hand, the plurality of gate bus lines **5** are sequentially driven by a drive circuit device on the gate side, which is not shown in the drawing, synchronizing with the timing of a horizontal synchronization signal. The drive circuit device on the gate side is also mounted on a circuit board same as shown in **FIGS. 1 and 2**, and the circuit board is connected to the peripheral area around the display panel **1**. Moreover, a gate clock signal and control signal that should be supplied to the drive circuit device on the gate side are propagated and supplied to a plurality of gate side drive circuit device circuit boards, through connection wirings provided on the display panel **1**.

[0031] FIG. 3 shows a configuration of a drive circuit device and a display panel in an embodiment of the present invention. The configuration shown in FIG. 3 can be applied to both of a source side drive circuit device and a gate side drive circuit device. As described above, to a display panel 1, like a liquid crystal panel, a drive circuit device circuit board 2 mounting a drive circuit device 7 is connected. In FIG. 3, the drive circuit device 7 and the circuit board 2 mounting the same are shown without distinguishing between them. And, three drive circuit devices 7A, 7B and 7C are connected through the connection wiring 10 on the display panel 1.

[0032] In FIG. 3, a clock signal, data signal and control signal to be supplied to the individual drive circuit device 7 are shown all together as a propagation signal Sa. This propagation signal Sa is a signal that changes during the same horizontal synchronization period (or vertical synchronization period), and is sequentially inputted to a drive circuit device 7A on an initial stage, a drive circuit device 7B on a next stage, and a drive circuit device 7C on a third stage. Also, a timing signal Sb is supplied to the plurality of the drive circuit devices 7 in parallel, and controls the specified operation timing for the plurality of the drive circuit devices 7. The timing signal Sb controls not only the operation timing, but also may control the operation itself. Further, a cascade signal CCD is a signal to control the timing when the individual drive circuit devices 7A, 7B and 7C start inputting of the propagation signal Sa, and the drive circuit device on the front stage supplies the cascade signal CCD to the drive circuit device on the rear stage to control the timing for the drive circuit device on the rear stage to start inputting.

[0033] The propagation signal Sa is inputted by the drive circuit device 7A on the initial stage, and then, inputted by the drive circuit device 7B on the next stage, and further inputted by the drive circuit device 7C on the third stage. The input start timing of the propagation signal Sa at the respective drive circuit devices 7A, 7B and 7C is controlled by the cascade signal CCD. Therefore, the propagation signal Sa is not required to be supplied to the drive circuit devices 7B and 7C on the following stages, while the drive circuit device 7A on the initial stage is inputting the signal Sa. Moreover, it is not necessary to supply the propagation signal Sa to the drive circuit devices 7C on the third stage and the following stages, while the drive circuit device 7B on the second stage is inputting the signal Sa.

[0034] Accordingly, the individual drive circuit devices 7A, 7B and 7C have driver circuits 20A, 20B and 20C to input the propagation signal Sa and drive the source bus lines or the gate bus lines, and gate circuits 22A, 22B and 22C to control the propagation of the propagation signal Sa to the rear stage. And, the gate circuits begin the propagation of the propagation signal Sa to the circuit on the rear stage, responding to gate control signals GCON 1, 2 and 3. And, the gate control signals have almost the same timing as the timing of the cascade signals CCD 2, 3 and 4 to be supplied to the drive circuit devices on the next stage, respectively, or slightly earlier timing than that. Therefore, the cascade signals CCD 2, 3 and 4 can be used instead of the gate control signals GCON 1, 2 and 3. In other words, the propagation start of the gate circuits 22A, 22B and 22C can be controlled by the cascade signals CCD 2, 3 and 4.

[0035] Therefore, to the drive circuit device 7A on the initial stage, a propagation signal Sa1 is supplied and inputted, however, the propagation of the propagation signal Sa1 to the rear stage is initially stopped by the gate circuit 22A. And at the timing when the drive circuit device 7B on the next stage starts inputting of the propagation signal, the gate circuit 22A is opened, and a propagation signal Sa2 is propagated to the drive circuit device 7B on the next stage. A propagation signal Sa3 to the drive circuit device 7C on the third stage is the same as the propagation signal Sa2.

[0036] FIG. 4 shows an operation-timing chart of the drive circuit device shown in FIG. 3. In FIG. 4, the propagation signal Sa, the cascade signal CCD, the gate control signal GCON, and the timing signal Sb are shown. The propagation signal Sa is sequentially inputted to the plurality of the drive circuit devices 7, during horizontal synchronization period (or vertical synchronization period), to be used for generating a drive signal. As an example of the propagation signal Sa, FIG. 4 shows that the data signals D0 through Dn, Dn+1 through D2n, and D2n+1 through D3n are individually inputted to the drive circuit devices 7A, 7B and 7C. The data signal can be a clock signal or a specified control signal.

[0037] A propagation signal Sa1 outputted from an input signal supply circuit, which is not shown in the drawing, is fetched into the driver circuit 20A, responding to a first cascade signal CCD1 to be supplied to the drive circuit device 7A on the initial stage. The propagation signal Sa1 means, as described later, a dot clock signal, data signal and its control signal, in the case of the source side drive circuit device, or a gate clock signal and its control signal in the case of the gate side drive circuit device.

[0038] While the drive circuit device 7A on the initial stage is inputting this propagation signal Sa1, the gate circuit 22A remains in the closed state, so, propagation to the drive circuit devices 7B and 7C on the rear stages will not be performed. Therefore, the propagation signal Sa1 which sequentially changes will only be propagated up to the drive circuit device 7A on the initial stage, so, the input signal supply circuit 8 will not drive the connection wiring 10 to the drive circuit devices on the rear stages.

[0039] Next, when the input of the propagation signal Sa1 by the drive circuit device 7A on the initial stage finishes, the supply of propagation signal Sa2 to the drive circuit device 7B on the next stage starts. That is to say, the gate circuit 22A opens, responding to the gate control signal GCON1 generated by the driver circuit 20A on the initial stage, and the propagation of the propagation signal Sa2 to the next stage starts. Further, responding to the cascade signal CCD2 generated by the driver circuit 20A on the initial stage, a driver circuit 20B in the drive circuit device 7B on the next stage starts inputting of the propagation signal Sa2. Therefore, the gate control signal GCON1 controls the start-up of the propagation of the propagation signal Sa to the rear stage, and the cascade signal CCD1 controls the start-up of the input of the propagation signal by the drive circuit device on the rear stage. Therefore, the gate control signal GCON1 has almost the same timing as the timing of the cascade signal CCD1, so, the gate control signal can be replaced with the cascade signal.

[0040] In FIG. 4, a timing signal Sb occurs once during the horizontal synchronization period (or vertical synchronization period), and controls the predetermined operation timing of the driver circuit.

[0041] **FIG. 5** shows a configuration of a source side drive circuit device. Further, **FIG. 6** shows a configuration of a data register in the source side drive circuit device. And, **FIG. 7** shows an operation-timing chart of the source side drive circuit device.

[0042] In **FIG. 5**, a drive circuit device circuit board **2A** and a drive circuit device **7A** on the initial stage, and a drive circuit device circuit board **2B** and a drive circuit device **7B** on the next stage are shown. Like **FIG. 3**, the drive circuit device and its mounting circuit board are shown without distinguishing between them. And, these drive circuit board circuit boards **2A** and **2B** are connected to a liquid crystal display panel **1**.

[0043] In the case of the source side drive circuit device, as a propagation signal Sa that changes during a horizontal synchronization period, and to be inputted sequentially by individual drive circuit devices, there are a clock signal ICLK, display data signals RD, GD, BD, and their invert control signal DINV. Also, as a signal Sb to be inputted simultaneously to all drive circuit devices, there are a latch pulse LP, a phase control signal PC to control a drive polarity, and a standard voltage VR. And, to the source side drive circuit device, a cascade signal CCD to control the input start of a data signal is inputted.

[0044] The drive circuit device **7A** on the initial stage has a shift register **30A**, which starts inputting of a clock ICLK1 responding to a cascade signal CCD1, and shifts output signals **S30** synchronizing with the clock ICLK1; a data register **32A**, which inputs and holds display data signals RD, GD, BD and a data invert control signal DINV, responding to the output signal **S30** of the shift register **30A**; and a latch circuit **34A**, which responding to a latch pulse LP, latches the data signals that are inverted or are not inverted from the display data signals RD, GD and BD inputted and held by the data register **32A**, corresponding to the data invert control signal DINV.

[0045] Moreover, a drive control circuit device **7A** has a level shift circuit **36A**, that reverses the phases of the data signal latched by the latch circuit **34A** for even numbered source bus lines and odd numbered source bus lines, corresponding to the phase control signal PC, and a D/A converter and output circuit **38A**, that converts digital outputs of the level shift circuit **36A** into analog outputs, and outputs the analog drive signals to the source bus lines SB.

[0046] Also, the drive control circuit device **7A** has a first gate circuit G1 to propagate the clock signal ICLK1, that is the propagation signal Sa1, to the following stage, and a second gate circuit G2 to propagate the display data RD, GD, BD, and the data invert signal DINV to the following stage. A gate control signal GCON1 to control the gate circuits is generated by a gate control circuit **40A**. The gate control circuit **40A** inputs and shifts the clock ICLK1, responding to the cascade signal CCD1, and generates the gate control signal GCON1, in the timing when a drive circuit device on the next stage starts inputting the propagation signal Sa2. The first and the second gate circuits G1 and G2 open, responding to the gate control signal GCON1, and start propagating of the propagation signal Sa2 and the clock ICLK2 to the drive circuit device on the next stage.

[0047] Like the drive circuit device **7A**, a drive circuit device **7B** on the next stage has a shift register **30B**, a data register **32B**, a latch circuit **34B**, a level circuit **36B**, a D/A converter/output circuit **38B**, a gate control circuit **40B**, and further a first and a second gate circuits G1 and G2. And, the drive circuit device **7A** on the initial stage and the drive circuit device **7B** on the next stage are connected through connection wirings **10** on a display panel **1**.

[0048] As shown in **FIG. 6**, the data register **32** has first flip-flops **42** to sequentially latch display data signals RD, GD and BD, synchronizing with shift outputs **S30** to be sequentially outputted from the shift register **30**, synchronizing with the clock ICLK, second flip-flops **44** to sequentially latch a data invert control signal DINV, and EOR gates **46** to output an XOR (an exclusive OR) of the data invert control signal and the display data. Each of the display data signals RD, GD and BD is a digital signal of 8 bits; therefore, the first flip-flops **42** latch digital signals of 24 bits. Also, the data invert control signal DINV is a control signal of 1 bit to be supplied, corresponding to the 24 bits display data signals.

[0049] With the display data signals RD, GD and BD being digital signals of 24 bits, 24 signal lines must be driven to H, L levels, synchronizing with the clock ICLK. So, information on whether the supplied display data signals RD, GD and BD of 24 bits should be inverted or not, comparing the display data signal of the previous pixel and the display data signal of the next pixel, will be generated as the data invert control signal DINV. By the utilization of the data invert control signal DINV, the number of bits of the display data signals which change from H level to L level, or from L level to H level can be reduced to less than a half of 24 bits.

[0050] For instance, in case of displaying data in white for the previous pixel, corresponding to the highest tone level, the display data signal of 24 bits is all H level, and if the pixel next to that is for display in black, corresponding to the lowest tone level, the display data signal of 24 bits is all L level. Consequently, the display data signals of 24 bits must change from the H level to the L level simultaneously. Therefore, by driving only the data invert control signal DINV to the H level to show inversion of display data signals, leaving all the display data signal on H level without changing, the power to drive the display data signal lines can be suppressed.

[0051] By the EOR gate **46**, the latched display data signals are inverted by the data invert control signal DINV of H level that indicates invert, and the latched display data signals are not inverted by the data invert control signal DINV of L level that indicates non-invert.

[0052] Then, the following shows description of operation of the source side drive circuit device, with reference to the operation-timing chart shown in **FIG. 7**. The drive circuit device **7A** on the initial stage inputs the clock ICLK1, responding to the cascade signal CCD1, and the shift register **30A** sequentially generates the data latch signals **S30**, synchronizing with the clock. Further, the display data signals RD, GD and BD, and their invert control signal DINV (the propagation signal Sa1 as noted in **FIG. 7**) change, synchronizing with the clock ICLK1, and the data register **32A** inputs and holds these display data signals and the invert control signal, responding to the data latch signals **S30**.

[0053] During that processing, the gate control circuit **40A** counts the clock ICLK responding to the cascade signal

CCD1, and generates a gate control signal GCON1, aligning with the timing when the drive circuit device **7B** on the next stage starts inputting the display data signals and their invert control signal.

[0054] Responding to this gate control signal GCON1, the first and the second gate circuits G1 and G2 start sequential transferring of the clock signal ICLK2, the display data signals RD, GD, BD, and the data invert control signal DINV to the rear stage. The gate circuits G1 and G2, which comprise, for instance, a non-invert buffer circuit, a transfer circuit, etc., start propagating of signals to the rear stage, responding to the gate control signal GCON1. Therefore, as shown in **FIG. 7**, a second propagation signal Sa2 starts changing, responding to the gate control signal GCON1. Further, a second clock signal ICLK2 also starts changing, responding to the gate control signal GCON1.

[0055] Responding to a cascade signal CCD2 outputted from a shift register **30A** on the initial stage, a shift register **30B** in a drive circuit device 7B on a second stage starts inputting of the clock ICLK2, and sequentially outputs data latch signals **S30**, synchronizing with the clock. Responding to the output, a data register **32B** inputs and holds the display data signals RD, GD, BD, and the data invert control signal DINV, that are the second propagation signal Sa2.

[0056] When the drive circuit device 7B on the second stage almost finishes the input of the display data signals and the data invert control signal, a gate control circuit **40B** outputs a second gate control signal GCON2, aligning with the timing when a drive circuit device on the third stage, which is not shown in the drawing, starts input. With this output, transfer of a clock signal ICLK3, display data signals RD, GD, BD, and the data invert control signal DINV to a drive circuit device on the third stage starts.

[0057] When the input of the display data signals and the data invert control signal finished at all drive circuit devices, a latch pulse signal LP is generated, and latch circuits **34** in all drive circuit devices latch display data **D0** through Dm held in the data registers **32**. Simultaneously with the latch, the display data **D0** through Dm held by the latch circuits **34** are transferred to level shift circuits **36**.

[0058] The level shift circuit **36** changes the polarity of the display data to the odd side source bus lines into negative or positive, and the polarity of the display data to the even side source bus lines into negative or positive, corresponding to a phase control signal PC, and outputs to a digital/analog convert circuit and output circuit **38**. Then, the source bus lines **SB0** through SBm will be driven simultaneously.

[0059] As described above, while a source drive circuit device on the initial stage is inputting the display data signal, data invert signal and the clock signal, transfer of these signals to a source drive device on the next stage is stopped, for the purpose of suppressing power consumption and occurrence of electromagnetic wave caused by changes in these signals. And, in the timing when a source drive circuit device on the second stage starts inputting of the display data signal, data invert signal and the clock signal, the gate circuit opens, so that propagation of these propagation signals to source drive circuit devices on the second can be started. However, at this time, propagation of these propagation signals to source drive circuit devices on the third stages or following stages is left in the stopped state.

[0060] As described above, the propagation signals are propagated only to the least possible number of drive circuit devices, and the propagation of the propagation signals to drive circuit devices on the following stages is stopped, so that power consumption and occurrence of electromagnetic wave can be suppressed.

[0061] **FIG. 8** shows a configuration of a gate side drive circuit device. And **FIG. 9** shows its operation flowchart. The gate side drive circuit devices **67A** and **67B** are individually mounted on drive circuit device circuit boards **62A** and **62B**, and connected to a liquid crystal display panel **1**. Also, the devices **67A** and **67B**, and the circuit boards **62A** and **62B** are shown in **FIG. 8**, without distinguishing each other. And, the gate side drive circuit device **67A** on the initial stage and the gate side drive circuit device **67B** on the next stage are connected through connection wirings **60** on the display circuit panel **1**.

[0062] The gate side drive circuit devices **67A** and **67B** sequentially drive gate bus lines **GL0** through GLn and GLn+1 through GL2N provided on the display panel **1**, synchronizing with a gate clock GCLK. For this purpose, the gate side drive circuit device has shift registers **72A** and **72B** to input a gate clock GCLK, and sequentially generate a drive timing signal **S72** synchronizing with the input; and gate drive pulse generator circuits **74A** and **74B** to sequentially generate gate drive pulse signals, synchronizing with the drive timing signal **S72**. Output enable signals **0E1** and **0E2** to be supplied to the gate drive pulse generator circuits **74A** and **74B** are signals to control the drive pulse timing for the purpose of preventing the gate bus lines from becoming the double selection state caused by the overlapping drive pulses to the adjacent gate bus lines.

[0063] Moreover, the gate drive circuit devices **67A** and **67B** have gate circuits G1 and G2 to control the propagation of the gate clock GCLK and the output enable signal OE to the rear stage. Shift counters **70A** and **70B** generate the gate control signals GCON1 and 2 aligning with the timing when a drive circuit device on the rear stage starts input, and these gate circuits G1 and G2 start the transfer of the gate clock and output enable signal to the rear stage, responding to the gate control signals. The operations of the gate circuit and the shift counter (gate control circuit) are the same as those on the source side drive circuit device.

[0064] Next, the following describes operations with reference to **FIG. 9**. From an input circuit device, which is not shown in **FIG. 8**, through input wirings **59** on the display panel **1**, the gate clock signal **GCLK1**, the output enable signal **OE1**, and the cascade signal **CCD1** are supplied to the drive circuit device **67A** on the initial stage. The shift register **72A** starts the input of the gate clock **GCLK1**, responding to the cascade signal CCD1, and sequentially generates gate drive timing signals **S72**, and further, the gate drive pulse generator circuit **74A** sequentially generates gate drive pulses **GL0** and so on. The gate drive pulses **GL0** and so on generated by the gate drive pulse generator circuit **74A** rise in the timing of the drive timing signal **S72**, and fall in the timing of the output enable signal **OE1**.

[0065] When the gate side drive circuit device **67A** on the initial stage finishes driving of the corresponding gate bus lines, the gate control signal GCON1 is generated in the timing when the gate side drive circuit device **67B** on the next stage starts inputting of the gate clock signal GCLK2

and the output enable signal OE2, so that the gate circuits G1 and G2 start the transfer of the gate clock signal and the output enable signal to the rear stage. Therefore, responding to the gate control signal GCON1, the propagation of a second gate clock signal GCLK2 and a second output enable signal OE2 starts.

[0066] The gate side drive circuit device **67**B on the next stage starts inputting of the second gate clock signal GCLK2 and the second output enable signal OE2, and sequentially drives the corresponding gate bus lines GL. And, the gate side drive circuit device **67**B on the next stage also opens the gate circuits G1 and G2, aligning with the timing when the gate side drive circuit device on the rear stage (not noted in the drawing) starts inputting of the gate clock signal and the output enable signal, and starts the propagation of a third gate clock signal GCLK3 and a third output enable signal OE3.

[0067] Therefore, the propagation signals, like the gate clock signal GCLK and the output enable signal OE are only propagated up to the drive circuit device that inputs these signals and drives the gate bus lines, and the propagation to drive circuit devices on the following stages will not be performed. Therefore, power consumption associated with driving these signals and occurrence of electromagnetic wave can be suppressed.

[0068] As described above, in the embodiments of the present invention, the supply of the clock signal, data signals, control signals, etc. to a plurality of drive circuit devices is limited only to the stage that inputs these signals and performs the predetermined operation, and the supply of these signals is stopped to drive circuit devices on the following stages. Therefore, even if drive load becomes larger, caused by the signal wiring to supply these signals becoming longer, or the signal wiring formed on the display panel increases the resistance or capacitance, the signal wiring to be driven can be suppressed, so that power consumption and occurrence of electromagnetic wave can be suppressed.

[0069] In the embodiment as described above, in the source side drive circuit device, the timing of starting the propagation of all of the clock signal, data signals and data invert signal to the rear stage has been controlled by the gate circuit, but the timing of starting the propagation of at least one of the clock signal, data signals and data invert signal to the rear stage may be controlled. Also, in the gate side drive circuit device, the timing of starting the propagation of at least one of the gate clock signal and output enable signal to the rear stage may be controlled.

[0070] As set forth hereinabove, according to the present invention, by means of allowing the propagation signals propagating to a plurality of drive circuit devices, not to be propagated to drive circuit devices in the rear stages following the drive circuit device that inputs the propagation signal, power consumption accompanied with driving of the propagation signal and occurrence of electromagnetic wave can be suppressed. Therefore, the drive circuit device of the present invention is useful as a drive circuit device for the display device such as the liquid crystal display device.

What is claimed is:

1. A drive circuit device for a display device which drives a plurality of bus lines disposed on a display panel, the drive circuit device comprising:

a driver unit that receives a propagation signal including at least one of a clock signal and a control signal, and generates a drive signal for the bus lines; and

a gate unit that, at the timing when a rear-stage drive circuit device starts receiving the propagation signal, after elapse of predetermined time from the reception of the driver unit, starts outputting of the propagation signal to the rear-stage drive circuit device.

2. A drive circuit device for a display device which drives a plurality of source bus lines disposed on a display panel, the drive circuit device comprising:

a driver unit that receives a clock signal, a data signal and a control signal, and sequentially fetches the data signal to generate a drive signal for the source bus lines in accordance to the fetched data signal; and

a gate unit that, at the timing when a rear-stage drive circuit device starts receiving a propagation signal including at least one of the clock signal, data signal and control signal, after elapse of predetermined time from the reception of the driver unit, starts outputting of the propagation signal to the rear-stage drive circuit device.

3. The drive circuit device according to claim 2, wherein

the control signal includes an invert control signal indicative of "invert", or "non-invert" of the data signal.

4. The drive circuit device according to claim 2, wherein

the driver device receives an input cascade signal to control the start of fetch of the data signal, and outputs an output cascade signal to control the fetch of the data signal at the rear stage, after the completion of fetching of the data signal.

5. The drive circuit device according to claim 4, further comprising:

a gate control circuit that inputs the input cascade signal and clock signal, and generates a gate control signal to control the gate unit to start outputting of the propagation signal.

6. The drive circuit device according to claim 4, wherein

the gate unit starts outputting of the propagation signal, in response to the output cascade signal.

7. The drive circuit device according to claim 4, further comprising:

a data register to fetch and hold the data signal at the timing of the clock signal, in response to the input cascade signal.

8. A drive circuit device for a display device which sequentially drives a plurality of gate bus lines disposed on a display panel, the drive circuit device comprising:

a driver unit that receives a clock signal and a control signal, and sequentially generates drive signals for the gate bus lines, in synchronism with the clock signal; and

a gate unit that, at the timing when a rear-stage drive circuit device starts receiving a propagation signal including at least one of the clock signal and control

signal, after the elapse of predetermined time from the reception of the driver unit, starts outputting of the propagation signal to the rear-stage drive circuit device.

9. The drive circuit device according to claim 8, wherein

the control signal includes an output enable signal to control the outputting period of the drive signal generated by the driver unit.

10. The drive circuit device according to claim 8, wherein

the drive circuit device receives an input cascade signal to control the start of fetching of the clock signal, and outputs an output cascade signal to control the fetching of the clock signal at the rear stage, after the completion of generation of the drive signals for the gate bus lines.

11. The drive circuit device according to claim 10, further comprising:

a gate control circuit which inputs the input cascade signal and the clock signal, and generates a gate control signal to control the gate unit to start outputting of the propagation signal.

12. The drive circuit device according to claim 10, wherein

the gate unit starts outputting of the propagation signal, in response to the output cascade signal.

13. The drive circuit device according to claim 10, further comprising:

a gate drive signal generator circuit to generate the drive signals at the timing of the clock signal, in response to the input cascade signal.

14. A display device having a plurality of drive circuit devices according to any one of claims 1, 2, or 8 that are connected in tandem, the display device comprising:

a display panel to which the plurality of drive circuit devices are connected, the display panel being provided with a plurality of source bus lines and a plurality of gate bus lines that intersect the source bus lines.

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