

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG DISPLAY CO.,
LTD, and SONY CORPORATION,
Petitioner,

v.

SURPASS TECH INNOVATION LLC,
Patent Owner.

Case IPR2015-00887
Patent 7,420,550 B2

Before SALLY C. MEDLEY, BRYAN F. MOORE, and BETH Z. SHAW,
Administrative Patent Judges.

SHAW, *Administrative Patent Judge.*

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Samsung Electronics Company, LTD., Samsung Display Company, LTD., and Sony Corporation (collectively “Petitioner”) filed a Petition to institute an *inter partes* review of claims 1–5 of Patent 7,420,550 B2 (“the ’550 patent”) pursuant to 35 U.S.C. §§ 311–19. Paper 1 (“Pet.”). Surpass Tech Innovation LLC (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 7 (“Prelim. Resp.”). We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

For the reasons set forth below, we institute an *inter partes* review of claims 1–5 of the ’550 patent.

A. Related Matters

Petitioner indicates that the ’550 patent is asserted in *Surpass Tech Innovation LLC v. Samsung Display Co., Ltd.* (Civil Action No. 1:14-cv-00337-LPS) and *Surpass Tech Innovation LLC v. Sharp Corporation* (Civil Action No. 1:14-cv-00338-LPS). Pet. 1. We denied *inter partes* review of the ’550 patent on March 10, 2015 in IPR2015-00022, Paper 9.

B. The ’550 Patent (*Ex. 1001*)

The ’550 patent is titled “Liquid Crystal Display Driving Device of Matrix Structure Type and Its Driving Method.” Ex. 1001, Title. The ’550 patent specifically discloses a matrix structure arrangement for a liquid crystal display (LCD) panel in which pixels are arranged in rows and columns.

An example of this structure is shown in Figures 4A and 4B of the '550 patent. Figure 4A is reproduced below:

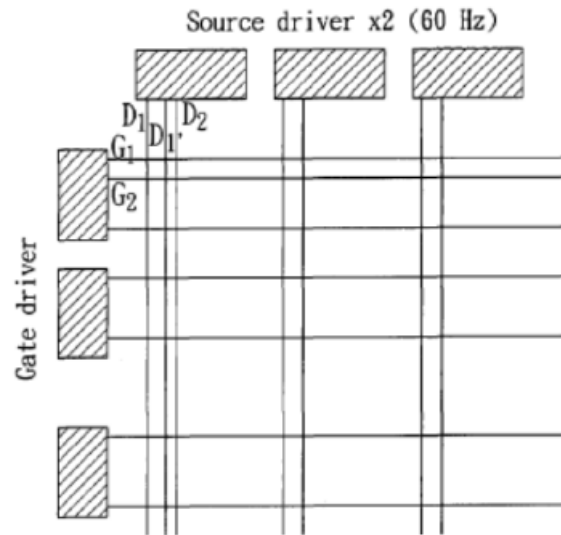


Fig. 4A

Figure 4A, reproduced above, depicts a schematic view showing the arrangement of the gate lines and the data lines of the display panel. Ex. 1001, 4:49–51. Figure 4B is reproduced below:

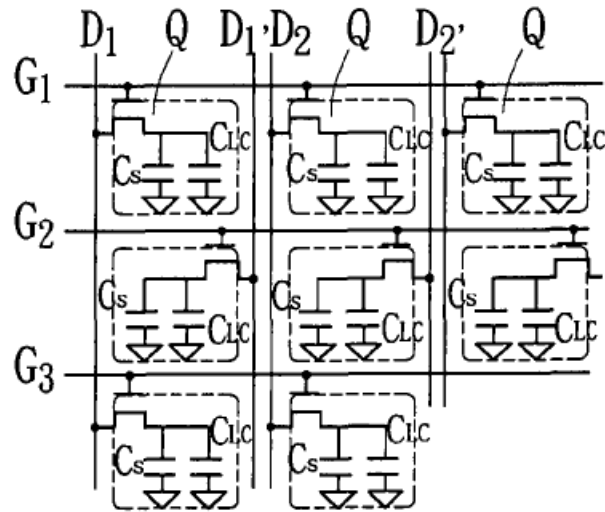


Fig. 4B

Figure 4B, reproduced above, depicts an enlarged schematic sectional view taken from Figure 4A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected to the gate lines and the data lines, of each thin film transistor. *Id.* at 4:52–56.

As shown in Figure 4A and Figure 4B, data lines D_1 , D_1' , D_2 , D_2' are connected to source drivers, and the data lines are grouped in pairs, such as D_1 and D_1' . The first and the second data lines D_1 , D_1' of the first group of data lines respectively are connected with the sources of all the thin film transistors Q of the odd and the even rows of the first column. *Id.* at 8:23–26.

The driving device includes a group of thin film transistors Q with matrix array, which consists of N rows and M columns of thin film transistors, wherein each thin film transistor Q can drive one pixel, so $N \times M$ pixels (shown by rectangle with dotted line) can be driven. *Id.* at 8:12–17.

The first gate line G_1 is connected with the gates of all the thin film

transistors Q of the first row, the second gate line G_2 is connected with the gates of all the thin film transistors Q of the second row, and so are the others. *Id.* at 8:17–20.

C. Illustrative Claim

Independent claim 1 of the '550 patent is illustrative and recites:

1. A liquid crystal display driving device of matrix structure type including:

a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that $N \times M$ of pixels can be driven;

a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and

M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second data lines of the first group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column, and the first data lines and the second data lines of each group of data lines are connected with the same source driver.

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