**TSU-JAE KING LIU**
Conexant Systems Distinguished Professor
Member, Kavli Energy Nanosciences Institute at Berkeley
Department of Electrical Engineering and Computer Sciences
253 Cory Hall #1770, University of California at Berkeley
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**EDUCATION** STANFORD UNIVERSITY, Palo Alto, California, USA

1994 Ph.D. in Electrical Engineering
Thesis: Applications of polycrystalline silicon-germanium thin films in metal-oxide semiconductor technologies
Thesis Advisor: Professor Krishna C. Saraswat

1986 M.S. in Electrical Engineering

1984 B.S. in Electrical Engineering

**EXPERIENCE**

UNIVERSITY OF CALIFORNIA, Berkeley, California, USA
7/14 to present *Chair*, Department of Electrical Engineering and Computer Sciences
7/12 to present *Chair*, Electrical Engineering Division
7/12 to 6/14 *Associate Chair*, Department of Electrical Engineering and Computer Sciences
Responsible for EECS Department programs, operations, strategic growth and relationships. Oversee academic personnel actions within the Electrical Engineering Division.

7/08 to 6/12 UNIVERSITY OF CALIFORNIA, Berkeley, California, USA
*Associate Dean for Research*, College of Engineering
Oversaw operations of the Engineering Research Support Organization which provides research administration support to faculty, research centers, and affiliated organized research units in the UC Berkeley College of Engineering. Facilitated new multi-disciplinary research initiatives, collaborations with international universities, and College development. Provided support to faculty for large center proposals and limited submission opportunities.

UNIVERSITY OF CALIFORNIA, Berkeley, California, USA
7/09 to present *Conexant Systems Distinguished Professor*
7/03 to present *Professor*, Electrical Engineering and Computer Sciences
Research and instruction in the areas of nanometer-scale CMOS devices and technology, semiconductor memory devices, micro/nano-electro-mechanical devices and technology, and large-area electronics. Research theme/thrust leader for the NSF Nanoscale Science and Engineering Center Of Integrated Nanomechanical Systems (COINS), the NSF Science and Technology Center for Energy Efficient Electronics Science (E3S), the SRC/MARCO-DARPA Focus Center on Materials, Structures, and Devices (MSD).

UNIVERSITY OF CALIFORNIA, Berkeley, California, USA
1/12 to 12/12 *Faculty Director*, UC Berkeley Marvell Nanofabrication Laboratory ("Nanolab")
8/06 to 6/08 *Faculty Director*, UC Berkeley Microfabrication Laboratory ("Microlab")
& 8/00 to 7/04 Responsible for overseeing lab operations and policies, setting new directions, and securing industrial support (in the form of grants and equipment, service, and cash donations) for this shared cleanroom research facility which supports a broad range of academic and industrial research. Liaison between Micro/Nanolab and faculty as well as industry.

11/04 to 6/06 SYNOPSYS, INC., Mountain View, California, USA
*Senior Director of Engineering*, Advanced Technology Group
Development of new silicon technologies and associated intellectual property.

7/03 to 6/04 UNIVERSITY OF CALIFORNIA, Berkeley, California, USA
*Vice Chair for Graduate Matters*, Electrical Engineering and Computer Sciences
Oversight and policy-setting for graduate admissions and the graduate study program.

| | |
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| 5/00 to 10/04 | PROGRESSANT TECHNOLOGIES, INC., Fremont, California, USA<br>*Co-founder and President*<br>Development and licensing of negative differential resistance transistor technology for low-cost, low-power integrated-circuit products. Negotiated sale of Progressant to Synopsys, Inc. |
| 7/99 to 6/03 | UNIVERSITY OF CALIFORNIA, Berkeley, California, USA<br>*Associate Professor*, Electrical Engineering and Computer Sciences<br>Research and instruction in the areas of sub-100nm CMOS devices and technology, novel semiconductor memory devices, micro-electro-mechanical systems technology, and maskless ion beam lithography. |
| 8/96 to 6/99 | UNIVERSITY OF CALIFORNIA, Berkeley, California, USA<br>*Assistant Professor*, Electrical Engineering and Computer Sciences<br>Research and instruction in the areas of integrated-circuit devices and technology, thin-film transistor technology, and micro-electromechanical systems technology. |
| 2/95 to 7/96 | STANFORD UNIVERSITY, Palo Alto, California, USA<br>*Consulting Assistant Professor*, Electrical Engineering<br>Initiated and guided graduate-level research projects to explore applications of silicon-germanium ($Si_{1-x}Ge_x$) in large-area electronics technologies. |
| 4/92 to 7/96 | XEROX PALO ALTO RESEARCH CENTER, Palo Alto, California, USA<br>*Member of Research Staff*<br>Conducted research and development of polycrystalline Si (poly-Si) thin-film transistor (TFT) technologies for high-resolution, high-performance flat-panel display applications. Collaborated with researchers at various universities, national laboratories, and companies to develop materials, processing techniques, and tools for flat-panel display manufacture. Investigated novel applications of silicon-germanium ($Si_{1-x}Ge_x$) for TFT technologies. Participated in ARPA- and EPRI-sponsored workshops to support and provide guidance to university research programs pertaining to TFT technologies. |
| 9/89 to 4/92 &<br>4/86 to 6/89 | STANFORD UNIVERSITY, Palo Alto, California, USA<br>*Research Assistant*<br>Helped develop instructional semiconductor-particle-transport simulation program. Investigated gate-dielectric materials for germanium MOS transistors. Studied formation of epitaxial silicon-germanium ($Si_{1-x}Ge_x$) films on Si and the effects of Ge at the $SiO_2$/Si interface, for $Si_{1-x}Ge_x$/Si heterojunction field-effect transistor applications. Modeled pyrometric temperature measurement. Developed a chemical vapor deposition technology for $Si_{1-x}Ge_x$ films. Characterized physical and electrical properties of polycrystalline $Si_{1-x}Ge_x$ films. Investigated applications of $Si_{1-x}Ge_x$ in MOS technologies. |
| 6/89 to 9/89 | TEXAS INSTRUMENTS, INCORPORATED, Dallas, Texas, USA<br>*Member of Technical Staff*<br>Participated in development of real-time temperature sensor for single-wafer rapid-thermal processing equipment. |
| 9/85 to 4/86 &<br>9/84 to 6/85 | STANFORD UNIVERSITY, Palo Alto, California, USA<br>*Teaching Assistant and Student Undergraduate Advisor*<br>Served as teaching assistant for courses in introductory electronics, linear systems, digital filters, signal processing, analog circuit laboratory, and semiconductor device physics. Duties included lecturing, supervision of laboratory sessions, individual tutoring, grading of problem sets and examinations, and providing curriculum counseling to undergraduate students. |
| Summer 1985 | HEWLETT-PACKARD COMPANY, Palo Alto, California, USA<br>*Production Engineer*<br>Wrote phase-linearity production test for the HP 8770A Arbitrary Waveform Synthesizer. |
| Summer 1984 | INTERNATIONAL BUSINESS MACHINES CORPORATION, San Jose, California, USA<br>*Pre-Professional Engineer*<br>Performed circuit simulations for microprocessor chip. Wrote computer programs for circuit analysis and product testing. |
| Summer 1983 &<br>Summer 1982 | TEXAS INSTRUMENTS, INCORPORATED, Houston, Texas, USA<br>*Engineering Aide*<br>Performed circuit simulations for DRAM products. Wrote computer programs for data analysis |

**PROFESSIONAL ACTIVITIES**

- Technical Program Committee Member, *2nd Int'l. Active Matrix Liquid Crystal Display Symposium* (1995)
- Organizing Committee Member, *International Semiconductor Device Research Symposium* (1995, 1997, 1999)
- Technical Program Committee Member, *Annual Device Research Conference* (1996, 1997, 1998)
- Co-chair, *Active Matrix Liquid Crystal Displays Conference, IS&T/SPIE Symposium on Electronic Imaging Science and Technology* (1997)
- Program Committee Member, *Int'l Conference on Solid State Devices and Materials* (1997, 2002-2004)
- Committee Member, *IEEE Int'l Electron Devices Meeting, Subcommittee on Detectors, Sensors and Displays* (1998, 1999)
- Short Course Organizer, *IEEE International Electron Devices Meeting* (2003)
- Committee Member, *IEEE International Electron Devices Meeting, Subcommittee on CMOS Devices* (2007)
- Committee Member, *IEEE International Electron Devices Meeting, Subcommittee on Solid-State Devices* (2008)
- International Advisory Committee Member, *International SiGe Technology and Device Meeting* (2002-present)
    - General Chair, *International SiGe Technology and Device Meeting* 2012
- Lead Organizer, *Symposium on CMOS Front-End Materials and Process Technology, 2003 MRS Spring Meeting*
- Chair, Emerging Applications Committee, *Symposium on SiGe: Materials, Processing, and Devices, 2004 Fall ECS Meeting*
- Organizer, *Symposium on Materials and Processes for Non-Volatile Memories, 2004 MRS Fall Meeting*
- Committee Member, *2004 International Conference on Solid-State and Integrated-Circuit Technology*
- Committee Member, *VLSI-Technology, Systems, and Applications Symposium* (2005, 2006, 2007)
- Technical Program Committee Member, *IEEE Symposium on VLSI Technology* (2005-2012)
  Short course co-organizer, 2009
  Rump session co-organizer, 2010
  Publication/publicity co-chair, 2012
- Program Committee Member, *IEEE Silicon Nanoelectronics Workshop* (2005-2012)
    - Program Chair, *2010 IEEE Silicon Nanoelectronics Workshop*
    - General Chair, *2012 IEEE Silicon Nanoelectronics Workshop*
- Technical Program Committee Member, *2006 IEEE Nanotechnology Materials and Devices Conference*
- Technical Program Committee Member, *IEEE International SOI Conference* (2011-2012)
- Organizing Committee Member, *2014 ECEDHA Conference* (2013-14)

- Member, *IEEE EDS VLSI Technology and Circuits Technical Committee* (2000-2001)
- Member, *Emerging Research Devices Working Group, SIA Int'l Technology Roadmap for Semiconductors* (2002- present)
- Member, *Process Integration, Devices, and Structures Working Group, SIA Int'l Technology Roadmap for Semiconductors* (2004-present)

- Editor, *IEEE Electron Device Letters* (1999-2004)
- Reviewer, *IEEE Electron Device Letters*, *IEEE Transactions on Electron Devices*, *IEEE Transactions on Nanotechnology*, *Solid State Electronics*, *Microelectronic Engineering*, *Nanotechnology Reviews*

**INDUSTRIAL ACTIVITIES**

Past and present technical consultant or advisory board member to various organizations including:

- Acorn Technologies, Inc. (Pacific Palisades, California)
- Advanced Process Development Group, Lawrence Livermore National Laboratory (Livermore, California) which spun out FlexICs (Milpitas, California)
- Advanced Technology Development Facility, SEMATECH (Austin, TX)
- Applied Materials (Santa Clara, CA)
- Crossbar Technologies Corp. (Santa Clara, CA)
- Rolltronics, Inc. (Menlo Park, California), 2000-2003
- Ronal Systems Corporation (Mountain View, California), 2003-2004
- SARIF (Vancouver, Washington)
- Silicon Clocks, Inc. (Fremont, California)
- Symmorphix, Inc. (Sunnyvale, California)
- Transvision Microsystems (Milpitas, California)

**SERVICE AS EXPERT WITNESS**

- *In the Matter of Certain Color Television Receivers and Color Display Monitors, and Components Thereof*, Investigation No. 337-TA-534 (International Trade Commission), 2005
- *L.G. Display Co., Ltd., v. AU Optronics Corporation et al*., Civil Action No. 06-0627-JJF (District of Delaware), 2009
- *Semiconductor Energy Laboratory Co., Ltd. v. Samsung Electronics Co., Ltd.; S-LCD Corporation; Samsung Electronics America, Inc.; Samsung Telecommunications America, LLC, and Samsung Mobile Display Co., Ltd*., Civil Action No. 3:09-CV-00001-BBC (Western District of Wisconsin), 2010
- *Anvik Corp. v. Nikon Precision, Inc., et al*., Civ. No. 7:05-7891 (S.D.N.Y.) ), 2012
- *In the Matter of Certain Integrated Circuit Devices and Products Containing the Same*, Investigation No. 337-TA-873 (International Trade Commission), 2014

**AFFILIATIONS**

- Advisor, Berkeley Nanotechnology Club
- Member and past Faculty Advisor for CA-A Chapter, Tau Beta Pi
- Fellow of the Institute of Electrical and Electronics Engineers
- Member, American Association for the Advancement of Science
- Past Member: Society for Information Display, Materials Research Society, Electrochemical Society

**AWARDS AND HONORS**

- Ross M. Tucker AIME Electronics Materials Award, 1992
- NSF CAREER Award, 1998
- DARPA Significant Technical Achievement Award (with Chenming Hu and Jeffrey Bokor), 2000
- SRC Inventor Recognition Award, 2000, 2003, 2005
- Outstanding Teaching Award (EE Division, EECS Department, UC Berkeley), 2003
- MARCO/FCRP Inventor Recognition Award, 2006, 2007
- IEEE Electron Devices Society Distinguished Lecturer, 2005-2009
- National Academy of Engineering Lillian M. Gilbreth Lectureship, 2006
- IEEE Fellow, 2007
- Conexant Systems Distinguished Professorship, 2009-present
- IEEE Kiyo Tomiyasu Award, 2010
- UC Berkeley Distinguished Faculty Mentoring Award, 2010
- The Electrochemical Society Dielectric Science and Technology Division Thomas D. Callinan Award, 2011
- Intel Outstanding Researcher in Nanotechnology Award (2012)
- SIA University Researcher Award (2014)

**PERSONAL INFORMATION**

- U.S. citizen
- Married; two children

**PATENTS**

1. U.S. Patent 5,250,818, “Low Temperature Germanium-Silicon on Insulator Thin-Film Transistor” (with K. C. Saraswat), October 5, 1993.
2. U.S. Patent 5,401,982, “Reducing Leakage Current in a Thin-Film Transistor with Charge Carrier Densities that Vary in Two Dimensions” (with M. G. Hack), March 28, 1995.
3. U.S. Patent 5,707,744, “Solid Phase Epitaxial Crystallization of Amorphous Silicon Films on Insulating Substrates” (with J. H. Ho), January 13, 1998.
4. U.S. Patent 5,893,949, “Solid Phase Epitaxial Crystallization of Amorphous Silicon Films on Insulating Substrates” (with J. H. Ho), April 13, 1999.
5. U.S. Patent 6,210,988, “Polycrystalline silicon germanium films for forming micro-electro-mechanical systems” (with A. Franke and R. T. Howe), April 3, 2001.
6. U.S. Patent 6,413,802, "FinFET transistor structures having a double gate channel extending vertically from a substrate and methods of manufacture" (with C. Hu, V. Subramanian, L. Chang, X. Huang, Y.-K. Choi, J. T. Kedzierski, N. Lindert, J. Bokor, and W.-C. Lee), July 2, 2002.
7. Taiwan Patent 154458, “Multiple-Thickness Gate Oxide Formed by Oxygen Implantation” (with Y.-C. King and C. Hu), August 16, 2002.
8. U.S. Patent 6,448,622, “Polycrystalline silicon-germanium films for micro-electromechanical systems application” (with A. Franke and R. T. Howe), September 10, 2002.
9. U.S. Patent 6,479,862, “Charge trapping device and method for implementing a transistor having a negative differential resistance mode” (with D. K. Y. Liu), November 12, 2002.
10. U.S. Patent 6,512,274, “CMOS-process compatible, tunable NDR (negative differential resistance) device and method of operating same” (with D. K. Y. Liu), January 28, 2003.
11. U.S. Patent 6,518,589, “Dual mode FET & logic circuit having negative differential resistance mode,” February 11, 2003.
12. U.S. Patent 6,559,470, “Negative differential resistance field effect transistor (NDR-FET) and circuits using the same,” May 6, 2003.
13. U.S. Patent 6,567,292, “Negative differential resistance (NDR) element and memory with reduced soft error rate,” May 20, 2003.
14. U.S. Patent 6,594,193, “Charge pump for negative differential resistance transistor,” July 15, 2003.
15. U.S. Patent 6,596,617, “CMOS compatible process for making a tunable negative differential resistance (NDR) device” (with D. K. Y. Liu), July 22, 2003.
16. U.S. Patent 6,664,601, Method of operating a dual mode FET & logic circuit having negative differential resistance mode,” December 16, 2003.
17. U.S. Patent 6,680,245, "Method for making both a negative differential resistance (NDR) device and a non-NDR device using a common MOS process" (with D. K. Y. Liu), January 20, 2004.
18. U.S. Patent 6,686,267, “Method for fabricating a dual mode FET and logic circuit having negative differential resistance mode,” February 3, 2004.
19. U.S. Patent 6,686,631, "Negative differential resistance (NDR) device and method of operating same" (with D. K. Y. Liu), February 3, 2004.
20. U.S. Patent 6,693,027, "Method for configuring a device to include a negative differential resistance (NDR) characteristic" (with D. K. Y. Liu), February 17, 2004.
21. U.S. Patent 6,700,155, "Charge trapping device and method for implementing a transistor having a configurable threshold" (with D. K. Y. Liu), March 2, 2004.
22. U.S. Patent 6,724,024, “Field effect transistor pull-up/load element,” April 20, 2004.
23. U.S. Patent 6,724,655, “Memory cell using negative differential resistance field effect transistors,” April 20, 2004.
24. U.S. Patent 6,727,548, “Negative differential resistance (NDR) element and memory with reduced soft error rate,” April 27, 2004.
25. U.S. Patent 6,753,229, “Multiple-thickness gate oxide formed by oxygen implantation” (with Y.-C. King and C. Hu), June 22, 2004.
26. U.S. Patent 6,754,104, “Insulated-gate field-effect transistor integrated with negative differential resistance (NDR) FET,” June 22, 2004.
27. U.S. Patent 6,794,234, “Dual work function CMOS gate technology based on metal interdiffusion” (with I. Polishchuk, P. Ranade, and C. Hu), September 21, 2004.
28. U.S. Patent, 6,795,337, “Negative differential resistance (NDR) elements and memory device using the same,” September 21, 2004.
29. U.S. Patent 6,806,117, "Methods of testing/stressing a charge trapping device," October 19, 2004.
30. U.S. Patent 6,812,084, "Adaptive negative differential resistance device," November 2, 2004.
31. U.S. Patent 6,847,562, "Enhanced read and write methods for negative differential resistance (NDR) based

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