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## SPECIAL ISSUE ON ANALOG AND SIGNAL PROCESSING CIRCUITS

FOREWORD..... *R. P. Colbeck and R. R. Spencer* 1659

### SPECIAL PAPERS

An 8-b 650-MHz Folding ADC .....	<i>J. van Valburg and R. J. van de Plassche</i>	1662
A 12-b 5-MSample/s Two-Step CMOS A/D Converter.....	<i>B. Razavi and B. A. Wooley</i>	1667
Digital-Domain Calibration of Multistep Analog-to-Digital Converters .....	<i>S.-H. Lee and B.-S. Song</i>	1679
An Oversampling Converter for Strain Gauge Transducers.....	<i>D. A. Kerth and D. S. Piasecki</i>	1689
A 1.2- $\mu$ m BiCMOS Sample-and-Hold Circuit with a Constant-Impedance, Slew-Enhanced Sampling Gate .....	<i>M. H. Wakayama, H. Tanimoto, T. Tasai, and Y. Yoshida</i>	1697
A 100-MHz 100-dB Operational Amplifier with Multipath Nested Miller Compensation Structure .....	<i>R. G. H. Eschauzier, L. P. T. Kerklaan, and J. H. Huijsing</i>	1709
A Compact Bipolar Class-AB Output Stage Using 1-V Power Supply .....	<i>F. J. M. Thus</i>	1718
A Highly Efficient CMOS Line Driver with 80-dB Linearity for ISDN U-Interface Applications.....	<i>H. Khorramabadi, J. Aridjar, and F. R. Peterson</i>	1723
An Inherently Linear and Compact MOST-Only Current Division Technique .....	<i>K. Bult and G. J. G. M. Geelen</i>	1730
A 155-MHz Clock Recovery Delay- and Phase-Locked Loop .....	<i>T. H. Lee and J. F. Bulzacchelli</i>	1736
A Si Bipolar Phase and Frequency Detector IC for Clock Extraction up to 8 Gb/s .....	<i>A. Pottbäcker, U. Langmann, and H.-U. Schreiber</i>	1747
A 6-GHz Integrated Phase-Locked Loop Using AlGaAs/GaAs Heterojunction Bipolar Transistors .....	<i>A. W. Buchwald, K. W. Martin, A. K. Oki, and K. W. Kobayashi</i>	1752
NMOS IC's for Clock and Data Regeneration in Gigabit-per-Second Optical-Fiber Receivers .....	<i>S. K. Enam and A. A. Abidi</i>	1763
10-GHz Si Bipolar Amplifier and Mixer IC's for Coherent Optical Systems.....	<i>T. Okamura, C. Kurioka, Y. Kuraishi, O. Tsuzuki, T. Senba, M. Ushirozawa, and M. Fujimaru</i>	1775
Si Bipolar Chip Set for 10-Gb/s Optical Receiver .....	<i>T. Suzuki, M. Soda, T. Morikawa, H. Tezuka, C. Ogawa, S. Fujita, H. Takemura, and T. Tashiro</i>	1781
11.6-GHz 1:4 Regenerating Demultiplexer with Bit-Rotation Control and 6.1-GHz Auto-Latching Phase-Aligner IC's Using AlGaAs/GaAs HBT Technology.....	<i>M. Bagheri, K.-C. Wang, M.-C. F. Chang, R. B. Nubling, P. M. Asbeck, and A. Chen</i>	1787
A 3-mW 1.0-GHz Silicon-ECL Dual-Modulus Prescaler IC.....	<i>M. Mizuno, H. Suzuki, M. Ogawa, K. Sato, and H. Ichikawa</i>	1794
A Si Bipolar 28-GHz Dynamic Frequency Divider .....	<i>M. Kurisu, G. Uemura, M. Ohuchi, C. Ogawa, H. Takemura, T. Morikawa, and T. Tashiro</i>	1799
A Two-Chip 1.5-GBd Serial Link Interface .....	<i>R. C. Walker, C. L. Stout, J.-T. Wu, B. Lai, C.-S. Yen, T. Hornak, and P. T. Petrino</i>	1805
An Experimental 5-Gb/s 16 $\times$ 16 Si-Bipolar Crosspoint Switch .....	<i>H. J. Shin and M. J. Immediato</i>	1812



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# Polysilicon TFT Circuit Design and Performance

Alan G. Lewis, *Senior Member, IEEE*, David D. Lee, *Member, IEEE*, and Richard H. Bruce, *Member, IEEE*

**Abstract**—Polysilicon thin-film technology is becoming increasingly attractive for active-matrix liquid-crystal displays (AMLCD's) and other large-area electronic devices, primarily because polysilicon thin-film transistors (TFT's) can be used to build integrated drive and interface circuitry on large-area substrates. Both n- and p-channel polysilicon TFT's can be fabricated, allowing CMOS circuit techniques to be used. However, TFT characteristics are poor in comparison to conventional single-crystal MOSFET's, and relatively coarse design rules must be used to be compatible with processing on large-area glass plates (more than 30 cm × 30 cm), and these limitations present a number of challenges for circuit design. This paper examines these issues and describes the performance of a range of digital and analog circuit elements built using polysilicon TFT's. Digital circuit speeds in excess of 20 MHz are reported, along with operational amplifiers with over 80 dB of gain and more than 1-MHz unity-gain frequency. Several polysilicon TFT switched-capacitor circuits are also reported and shown to have adequate linearity, output swing, and settling time to form integrated data line drivers on an AMLCD.

## I. INTRODUCTION

INTEREST in circuits built using polysilicon thin-film transistors (TFT's) has recently increased for several reasons. Although the inferior performance of these devices in comparison to conventional single-crystal MOSFET's is well documented [1]–[4], they have the important advantage of being compatible with fabrication on large-area glass or quartz substrates (more than 30 cm × 30 cm). This makes TFT's usable in applications where the physical size of the circuit must be large, for example if the circuit is an active-matrix liquid-crystal display (AMLCD) [4]–[6], a page-width optical scanner [7], [8] or a page-width print head [9]. Although there have been many reports of particular devices incorporating polysilicon TFT's and TFT circuits [4]–[8], there has been little work published so far concentrating specifically on the underlying design issues and performance capabilities of polysilicon TFT circuits. This paper, like the ISSCC presentations on which it expands [2], [10], is intended to focus on these subjects. The work described here does not deal with a complete large-area polysilicon TFT electronic device, but rather examines the performance of a range of basic circuit elements, some of which are already used in applications, and some of which show promise for increased functionality on large-area substrates in the future.

The most common, and the most important, application of polysilicon TFT's remains AMLCD's. As the various circuit elements are discussed in this paper, therefore, their performance will be compared with AMLCD driving requirements. In order to do this, typical drive circuits for AMLCD's are briefly reviewed in Section IV. It should be noted, however, that there are other applications for these devices, and more are likely to present themselves as the technology matures and TFT circuit performance improves.

## II. POLYSILICON THIN-FILM TECHNOLOGY

In this section, the main features of polysilicon thin-film technologies are reviewed. Fig. 1 shows cross sections of n- and p-channel polysilicon TFT's along with an integrated capacitor. The TFT's themselves are very similar to single-crystal silicon-on-insulator (SOI) MOSFET's, except that the active silicon layer is polycrystalline instead of monocrystalline. Polysilicon technology also has several of the advantages of SOI, including excellent interdevice isolation and negligible parasitic capacitance. The capacitor is formed between the gate and active polysilicon layers by the addition of a single implant to dope the active polysilicon layer under the gate. The structure is similar in layout to a polysilicon-to-diffusion capacitor in a conventional single-crystal MOS technology, but in this case there is negligible parasitic capacitance associated with either electrode. Both plates of the capacitor can be sufficiently heavily doped that the series resistance remains low, and the capacitance does not vary significantly over the bias ranges typically found in large-area devices.

There are several broad types of polysilicon TFT technology, differentiated by the annealing process used to crystallize the active polysilicon layer and the maximum processing temperature used [3], [11]. High-temperature technologies typically use furnace annealing, and at least one high-temperature process step (often during the gate dielectric formation), and this restricts the choice of substrate material to quartz. Furnace annealed low-temperature technologies use a similar process to the high-temperature technologies, but keep the maximum processing temperature less than about 600°C in order to allow the use of lower cost glass substrates. A third technology variant uses laser annealing to achieve recrystallization and is also compatible with low-cost glass substrates. The laser annealed polysilicon TFT's have been shown to offer the best performance, although the technology is not

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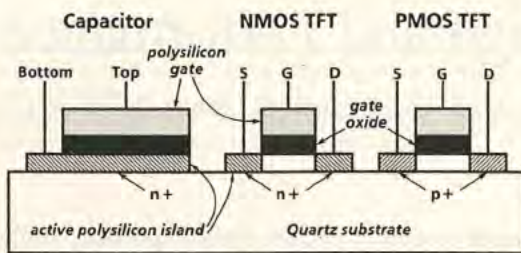


Fig. 1. Polysilicon TFT's with integrated capacitor.

yet mature and poor consistency and uniformity remain significant problems. High-temperature quartz-based technologies are relatively mature, offer good TFT performance, and are used for small viewfinder or projection displays. Low-temperature glass-based technologies offer low cost, although the TFT performance is not usually as good as can be achieved with high-temperature technologies [12].

The results reported in this paper were obtained using relatively conventional high- and low-temperature furnace recrystallized polysilicon thin-film devices fabricated at Xerox PARC. The experimental circuits were fabricated on quartz wafers, although the process conditions and design rules are the same as those used with large-area substrates. The device performance achieved is comparable with the best reported for similar technologies by other authors [1], [4]–[8], [11]. Although, as discussed below, the TFT characteristics are inferior to conventional single-crystal MOSFET's, useful circuit performance can still be achieved. As laser annealed technologies mature, even greater circuit functionality is likely to become possible.

The circuits reported below were all designed using layout rules that are relatively coarse in comparison with those used in single-crystal technologies. There are several reasons for this. First, of course, are the photolithographic and processing restrictions imposed by the need to fabricate the TFT's on very large-area substrates. Second, short-channel effects are relatively severe in polysilicon TFT's, particularly at high drain voltages [13]. Third, most large-area devices are constrained to operate at supply voltages of at least 15 V; an AMLCD pixel, for example, typically requires a total voltage swing of about 10 V to encompass both drive polarities [14], and with sufficient headroom to achieve this using polysilicon TFT drivers means a supply voltage of about 15 V.

### III. POLYSILICON TFT CHARACTERISTICS

Fig. 2 shows simple  $I$ - $V$  characteristics for n- and p-channel TFT's fabricated using the high-temperature process; devices fabricated with the low-temperature technology are qualitatively similar although the drive currents are lower. The poor saturation arises through a similar mechanism to that responsible for the kink effect in SOI MOSFET's [15], that is, channel avalanche multiplication occurring in the high-field region near the drain

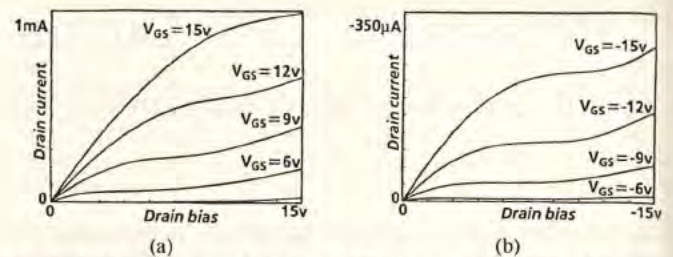


Fig. 2. High-temperature polysilicon TFT characteristics ( $W = 50 \mu\text{m}$ ,  $L = 10 \mu\text{m}$ ). (a) NMOS. (b) PMOS.

in polysilicon TFT's there is an additional mechanism related to the high trap state density that exaggerates the effect of avalanche multiplication still further [16]. Since the poor saturation characteristics are not related to punchthrough or other breakdown effects, the off-state current is not affected. The impact on digital circuits is only minor, and the extra drain current even increases switching speeds slightly. However, the low output impedance presents a greater problem for analog circuit design where high impedances are needed to achieve good voltage gain.

The main weakness of polysilicon TFT's in comparison with single-crystal devices is their relatively low drive current, particularly in low-temperature devices. This can be seen from Fig. 2, and is further illustrated in Fig. 3 where the effective channel mobility is plotted as a function of normalized gate bias for both an n-channel polysilicon TFT and a conventional 2- $\mu\text{m}$  gate length MOSFET. In each case the gate bias is normalized by the typical operating voltage for circuits built using the devices, 5 V for the MOSFET and 15 V for the polysilicon TFT. The peak MOSFET mobility is observed at a gate bias a little above threshold, and the degradation at higher gate bias is caused by increased surface scattering as the channel inversion layer is compressed by the increasing gate field. The TFT mobility is about an order of magnitude lower, and increases steadily as the gate drive rises until it saturates at a gate voltage of about 10 V; both the lower effective channel mobility and the gate bias dependence are due to the high trap state density in the device channel. The low drive current of the polysilicon TFT's has a significant effect on digital circuit speed, but in the analog case the effect is even more severe since transistors in amplifiers are typically biased with a low  $V_{GS}$  to keep  $V_{DSAT}$  low, and as Fig. 3 shows, under such conditions the effective TFT mobility is well below its peak value.

Another important device characteristic, particularly for analog circuit applications, is the noise performance, and in this respect polysilicon TFT's are again markedly inferior to single-crystal devices. Typical noise figures for polysilicon TFT's are about an order of magnitude higher than for conventional MOSFET's; at low frequencies (less than about 100 kHz) flicker noise dominates and shows roughly the same channel size dependence seen with MOSFET's. At higher frequencies, thermal noise domi-

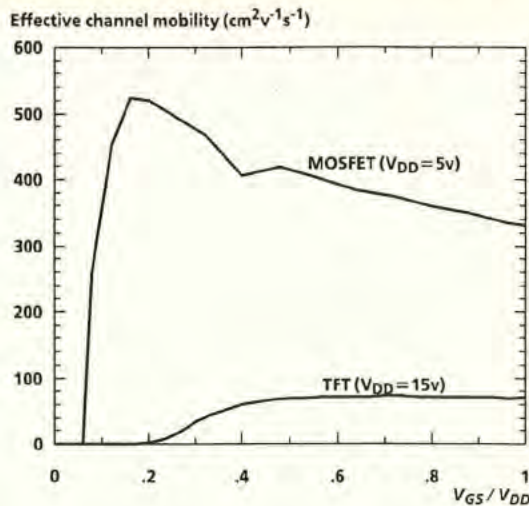


Fig. 3. Polysilicon TFT and single crystal MOSFET channel mobility.  $V_{DS} = 0.1$  V, n-channel.

TABLE I  
TECHNOLOGY COMPARISON

	Low-temperature poly-Si TFT	High-temperature poly-Si TFT	Conventional MOSFET
NMOS: $V_T$ (V)	2	2	0.7
$\mu$ ( $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ )	40	100	500
PMOS: $V_T$ (V)	-8	-3	-0.7
$\mu$ ( $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ )	20	50	200
Operating voltage (V)	18	15	5
Feature size ( $\mu\text{m}$ )	5	5	1
Substrate	LA glass	LA quartz	Si wafer

been discussed elsewhere [10], [17], and is not considered further here, except to note that since the frequency dependence is qualitatively similar to that obtained with conventional MOSFET's, the same switched-capacitor techniques used to suppress low-frequency noise in these devices are expected to be equally effective with TFT's.

Table I summarizes some of the main characteristics of polysilicon TFT's and compares them with typical values for conventional single-crystal MOSFET's. Data are shown for both low- and high-temperature processed TFT's. The low-temperature NMOS TFT's have lower channel mobility, and hence lower drive current, than their high-temperature counterparts, but otherwise are similar. However, the difference between low- and high-temperature p-channel TFT's is more marked. Not only is the channel mobility lower in the low-temperature device, but the threshold voltage is also much more negative, so that the drive current available from a low-temperature p-channel TFT is more than an order of magnitude lower than that available from a high-temperature device [12]. Despite the weak p-channel TFT's in the low-temperature technology, CMOS circuits are still often used for several

tion, good noise immunity, and the difficulty in fabricating depletion-mode NMOS devices to act as loads.

#### IV. DRIVE REQUIREMENTS FOR AMLCD'S

This section reviews the main driving requirements for AMLCD's. These displays represent the major application area for polysilicon TFT's, and their drive requirements will be used to add perspective to the measured performance described below. Fig. 4 shows the main circuit elements of an AMLCD along with typical drive waveforms. The active matrix is composed of orthogonal scan and data lines, and a single pixel is formed at each intersection. Each pixel contains a TFT and a capacitor. The capacitor is formed by a pair of transparent electrodes sandwiching the liquid-crystal material. Plane polarizers are placed on each side of the cell so that incoming light is first polarized, then passes through the liquid crystal, and finally leaves via the second polarizer. The voltage applied to the capacitor controls the orientation of the liquid-crystal molecules, and this in turn controls the twist in the plane of polarization of the light traveling through the cell. In this way, the transmission of light through the entire module (liquid-crystal cell and polarizers) can be controlled [14]. When a scan line goes high, each TFT along that line is turned on and the voltages present on the data lines are transferred in parallel into all the pixels along that line, setting the required transmission pattern. When the scan line goes low again, the TFT is turned off, the charge remains on the pixel capacitance, and the pixel voltage remains fixed until it is rewritten during the next frame. The liquid-crystal capacitance is strongly voltage dependent and may not be large enough to store the pixel voltage until the next frame (charge can leak off both through the TFT and the liquid-crystal material), and in practice an additional storage capacitor is often added to the pixel to improve the storage time and linearity.

Conventional amorphous-silicon TFT AMLCD's use single-crystal integrated circuits to generate the drive waveforms illustrated in Fig. 4. A full-color  $640 \times 480$ -pixel display requires about a dozen chips, and several thousand individual connections must be made between the active matrix substrate and the driver IC's. The driver IC's and the very large number of connections contribute significantly to the cost of the display, and also play an important role in determining long-term reliability. The use of polysilicon TFT's allows the driver circuits to be fabricated simultaneously with the active matrix on the same glass substrate, eliminating the need for external driver chips and greatly reducing the number of external connections needed to operate the display. In addition, integrated drivers allow much denser displays to be built, offering the possibility of physically small but high-pixel-count light valves for projection applications [18].

The function of the scan drivers is to generate the scan pattern, turning each scan line on in turn. This is usually accomplished by a simple shift register and buffers to drive

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