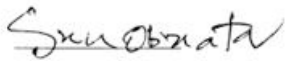


CERTIFICATION OF TRANSLATION

I, Shunsuke Obinata, hereby certify that I am well versed in both Japanese and English languages, that I have over 30 years of experience in translating Japanese technical documents into English, and vice versa, and that the following translation of the patent document *JPH_1990214818Horii* into English is accurate and complete to the best of my knowledge and ability.

January 31, 2015

A handwritten signature in black ink that reads "Shunsuke Obinata". The signature is written in a cursive, slightly slanted style.

Shunsuke Obinata

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| (54) Title of the Invention: Liquid Crystal Device and Method for Driving the Device (21) Application No.: H01-35067 (22) Filing date: February 16, 1989 | (72) Inventor: HORII, Juichi Central Research Institute, Hitachi Ltd., 1-280 Higashi Koigakubo, Kokubunji, Tokyo (72) Inventor: KANEKO, Yoshiyuki Central Research Institute, Hitachi Ltd., 1-280 Higashi Koigakubo, Kokubunji, Tokyo (72) Inventor: KOIKE, Norio Central Research Institute, Hitachi Ltd., 1-280 Higashi Koigakubo, Kokubunji, Tokyo (71) Applicant: Hitachi, Ltd. 4-6, Kanda Surugadai, Chiyoda-ku, Tokyo (74) Agent: NAKAMURA, Junnosuke, patent agent | |

SPECIFICATION

1. Title of the Invention: LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR DRIVING THE DEVICE

2. Claims

1. In a liquid crystal display device, comprising:

a first substrate on which multiple gate lines lined up in a row direction, multiple data lines lined up in a column direction in an orthogonal manner, and multiple thin film transistors that are

formed at the intersections of the rows, each of the intersections being formed as a pixel, are formed, and

a second substrate on which a transparent conductor is provided, wherein liquid crystal is sealed between the two substrates; a liquid crystal display device wherein the above multiple gate lines are divided into groups of k lines (where k is a positive integer not less than two), each of the k data lines of each of the columns being connected to the corresponding one of pixels connected respectively to the k gate lines making up each of the groups; and comprising means for applying the same drive pulse to the above divided k gate lines.

2. In the liquid crystal display device according to Claim 1,

a liquid crystal display device wherein the drive pulse applied to the k gate lines making up the group is supplied from k gate scan circuits independently of each other or one another.

3. In the liquid crystal display device according to Claim 1 or 2, a liquid crystal display device further comprising: k scan circuits for driving the data lines, or k line memories in a data scan circuit for driving the data lines, wherein image signal is written into the pixels of k rows connected respectively to the k gate lines driven independently of each other or one another and simultaneously.

4. In a liquid crystal display device, comprising: a first substrate on which multiple gate lines lined up in a row direction, multiple data lines lined up in a column direction in an orthogonal manner, and multiple thin film transistors that are formed at the intersections of the rows are provided, each of the intersections being formed as a pixel, and

a second substrate on which a transparent conductor is formed, wherein liquid crystal is sealed between the two substrates; a driving method for liquid crystal display device, wherein

the above multiple gate lines are driven simultaneously k gate lines at a time (where k is an integer that is not less than two), and wherein the operation of the k pixels that are driven simultaneously by column is controlled by the respectively connected data lines.

5. In the driving method of Claim 4, a driving method for liquid crystal display device wherein

a pair of odd-numbered gate lines (G_1, G_3) is driven simultaneously, and after the completion of writing, every other pair of numbered gate lines (G_5, G_7) and then the next pair (G_9, G_{11}), ..., are driven simultaneously and sequentially to conduct the write process to form a first field; wherein next, a pair of even-numbered gate lines (G_2, G_4) is driven simultaneously, and wherein driving operation in the same manner is performed to form a second field, thereby performing interlacing scan.

3. Detailed Description of the Invention

[Field of Industrial Application]

The present invention relates to an active-matrix liquid crystal display device and a method for driving the device, and more particularly to a liquid crystal display device and a method for driving the device suited for achieving good image quality.

[Conventional Technology]

An active-matrix liquid crystal display device is disclosed in, for example, Japanese Patent Application Publication No. S54-018886.

Fig. 2 is a circuit diagram of an example of an active-matrix liquid crystal display device.

In Fig. 2, the reference numerals 21 and 22 denote a liquid crystal cell and a charge storage capacitor, respectively. The numeral 23 denotes a thin film transistor (hereinafter abbreviated as TFT) connected to one of the two electrodes of the liquid crystal cell 21. These components make up each pixel. The numeral 24 denotes multiple data lines, the number of which is n , collectively. Each of the data lines D_1 to D_n is connected as a common data line to the TFTs of the corresponding column in the active matrix. The numeral 25 denotes multiple gate lines, the number of which is m , collectively. Each of the gate lines G_1 to G_m is connected as a common scanning line to the TFTs of the corresponding row in the active matrix. The numeral 26 denotes a driver circuit that applies scanning pulses to the gate lines G_1 to G_m sequentially (hereinafter referred to as "gate driver"). The numeral 27 denotes a scanning circuit that applies image signals

for the horizontal scan to the data lines D_1 to D_n in parallel (hereinafter referred to as "data driver"). The numeral 28 denotes a transparent common electrode that is connected on a common basis to the other electrode of the liquid crystal cell which is formed on the substrate facing across the substrate on which the TFT is formed and the liquid crystal.

Next, the drive operation of an active-matrix liquid crystal display device will now be explained.

Fig. 3 is a schematic view of an example drive waveforms.

In Fig. 3, in synchronization with the applying of a pulse V_{Gi} to the i -th gate line G_i , providing the voltage V_{on} necessary to turn on the TFT, an image signal voltage V_{Sj} is applied to the j -th data line D_j . As a result, a charge is stored at the liquid crystal capacitance and the storage capacitance of a pixel C_{ij} , and the writing of an image signal is performed. The writing is completed during a time period when the gate voltage is V_{ON} , that is, during $t_1 \sim t_1 + \Delta t$. The voltage of the pixel C_{ij} is retained at V_{Sj} until the next writing of a signal at time $t_1 + T$, that is, after the lapse of one field cycle T , and the gate voltage remains at V_{OFF} .

In line-sequential scan, all of the TFTs connected to the i -th gate line G_i are turned on at the same time, and signal writing is performed in the same manner as above. At the time of the completion of signal writing for the i -th row, a pulse V_{Gi+1} is applied to the $i+1$ -th gate line G_{i+1} . As a result, all of the TFTs connected to the $i+1$ -th gate line G_{i+1} are turned on at the same time, and signal writing is performed in the same manner as above.

Through sequential gate voltage application, TFTs are turned on sequentially, and pixels are driven by this line-sequential scan.

[Problems to be Solved by the Invention]

In principle, an active-matrix liquid crystal display device is driven as described above. In actual driving, however, a gate voltage pulse propagation delay must be taken into consideration.

Fig. 4 is a waveform chart of a gate pulse and a delayed gate pulse.

As illustrated in Fig. 4, even when a gate pulse applied to a gate line has a rectangular

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