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Transmitted herewith for filing is the patent application of under 37 CFR 1.53(b):  
INVENTOR(S): Yuh-Ren SHEN, Cheng-Jung CHEN, Chun-Chi CHEN

TITLE: LIQUID CRYSTAL DISPLAY DRIVING DEVICE OF MATRIX STRUCTURE TYPE AND ITS DRIVING METHOD

This application is being filed without the declaration of the inventor(s). Inventor information is as follows:

This is a continuing application of prior Application No.     /      
 Continuation  
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 Continuation-in-part

Enclosed are:

- Specification
- 26 Sheets of drawings
- Oath or Declaration signed by the inventor(s)
  - Newly Executed
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- Convention priority is claimed
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- An executed Assignment in favor of VAST VIEW TECHNOLOGY INC.
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- Preliminary Amendment
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The Filing Fee has been calculated as shown:

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Indep. Claims	7 - 3 = 4 x \$ 43 = \$172	x \$ 86 =
Multiple Dependent Claims Presented + \$145 = + \$290 =		
<b>TOTAL</b>	<b>\$881</b>	

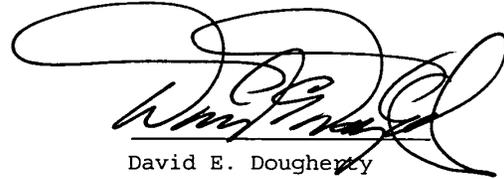
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TITLE: LIQUID CRYSTAL DISPLAY DRIVING DEVICE OF MATRIX  
STRUCTURE TYPE AND ITS DRIVING METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention

5           The present invention relates to a liquid crystal display driving device of matrix  
structure type and its driving method, especially to a display driving device and its  
driving method, which can simultaneously or synchronously drive a plurality of thin  
film transistors to increase the response speed, wherein the source and the gate of each  
thin film transistor in the driving device are respectively connected with different gate  
10 lines and data lines to let the specific transistor be driven by the gate drivers and the  
data drivers, and the predetermined voltage for over drive or the data voltage for the  
present frame interval is applied to accomplish the object of increasing the response  
speed. The present invention can suit for the picture treatment of various liquid crystal  
displays, organic light emitting diode (OLED) display or plasma display panel (PDP).

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2. Description of the Prior Art

          Because the liquid crystal display possesses the advantages of low power  
consumption, light of weight, thin thickness, without radiation and flickering, it  
gradually replaces the traditional cathode ray tube (CRT) display in the display market.  
20 The liquid crystal display is chiefly used as the screen of the digital television, the  
computer or the notebook computer. In particular, the large sized liquid crystal display  
is widely used in the amusements of the life, especially in the field in which the view  
angle, the response speed, the color number, and the image of high quality are in great  
request.

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          Referring to Fig.1A and 1B, they are the simple schematic views showing the  
internal structure of the prior liquid crystal display. Mark 10 is the display panel. The  
data driver 11 is installed above the display panel, which can change the data of the  
adjusted gray level signal into the corresponding data voltage. The image signal can  
30 be transferred to the display panel 10 through the plurality of data lines 111 connected  
with the data driver 11. The gate driver 12 is installed on one side of the display panel  
10, which can continuously provide scanning signal. The scanning signal can be  
transferred to the display panel 10 through the plurality of gate lines 121 connected  
with the gate driver 12. The data line 111 and the gate line 121 are orthogonally  
35 crossed and insulated with each other. The area enclosed in them is a pixel 13. After

the image signal is output from the data driver 11, it will get to the source of the thin film transistor  $Q_1$  in the pixel 13 through the data line  $D_1$ , and a control signal is correspondingly output from the gate driver 12, it will get to the gate of the thin film transistor  $Q_1$  through the gate line  $G_1$ . The circuit in the pixel 13 will output the output voltage to drive the liquid crystal molecular corresponding to the pixel 13, and a parallel plate type of capacitor  $C_{LC}$  (capacitor of liquid crystal) will be formed by the liquid crystal molecules between the two pieces of glass substrates in the display panel 10. Because the capacitor  $C_{LC}$  cannot keep the voltage to the next time of renewing the frame data, so there is a storage capacitor  $C_S$  provided for the voltage of the capacitor being able to be kept to the next time of renewing the frame data.

The image treatment of the display is affected by the properties of the liquid crystal molecular such as viscosity, dielectricity and elasticity etc. The brightness in the traditional CRT is displayed by the strike of the electron beam on the screen coated with phosphorescent material, but the brightness display in the liquid crystal display needs time for the liquid crystal molecular to react with the driving voltage, the time is called "response time". Taking the normally white (NW) mode as an example, the response time can be divided to two parts:

(1) The ascending response time: it is the time for the liquid crystal molecular to rotate with the application of the voltage when the brightness of the liquid crystal box in the liquid crystal display changes from 90% to 10%, simply called " $T_r$ "; and

(2) The descending response time: it is the time for the liquid crystal molecular to restore without the application of the voltage when the brightness of the liquid crystal box changes from 10% to 90%, simply called " $T_f$ ".

When the display speed of the frame is above 25 frames per second, human will regard the quickly changing frames as the continuous picture. In general above 60 frames per second is the display speed of the screen in the modern family amusements such as DVD films of high quality and electronic games of quick movement, in other words, the time of each frame interval is  $1/60 \text{ sec} = 16.67\text{ms}$ . If the response time of the liquid crystal display is longer than the frame interval time, the phenomena of residue image or skip lattice would happen in the screen so that the quality of the image is badly affected. At present the methods for decreasing the response time of the liquid crystal display have: lowering the viscosity, reducing the gap of the liquid crystal box, increasing the dielectricity and the driving voltage, wherein the methods of lowering the viscosity, reducing the gap of the liquid crystal box and increasing the

dielectricity can be executed from the material and the making process of the liquid crystal and the method of increasing the driving voltage can be executed from the driving method of liquid crystal panel. The latter can further improve the response speed of the gray level in no need of largely changing the structure of the display panel. It is called "overdrive" (OD) technique, wherein the increasing voltage can be transferred to the liquid crystal panel through the driver integrated circuit (driver IC) to increase the voltage for rotating the liquid crystal so that the expected brightness of the image data can be quickly obtained and the response time can be reduced due to the quick rotation and restoration of the liquid crystal.

Referring to Fig.2, the liquid crystal display has different brightness at different driving voltage. If  $L_1$  is the expected brightness of the image data and the liquid crystal molecular is driven by the present data voltage  $V_1$  to display the brightness, the brightness variation displayed by the driven liquid crystal molecular is shown as curve 21 and the time for obtaining the brightness is  $t_0$ . An increased driving voltage  $V_2$  is provided to reduce the time for obtaining the brightness according to the brightness variation of the display gray level, which has been measured in advance. The brightness variation is shown as curve 22. Therefore, the time for obtaining the expected brightness can be reduced from  $t_0$  to  $t_0'$ ; this is the so-called OD technique.

Referring to Fig.3A to 3C, if the expected brightness of an image in the preceding frame interval I-1 is code 32, and the expected brightness of the said image in the present frame interval I becomes code 120, the brightness variation of the liquid crystal display is shown as curve (a) without making use of OD technique. It is shown that the expected brightness cannot be obtained unless the I+1<sup>th</sup> frame interval is got. This would produce the problem of residue image. By use of OD technique, the driving voltage is increased to code 200 in the present frame interval I to be able to obtain the expected brightness at the end of the frame interval. Its brightness variation is shown as curve (b). In the driving process of the first gate line  $G_1$  and the first data line  $D_1$ , when the frame interval I begins, a control voltage pulse is given to the first gate line  $G_1$  by the gate driver and at the same time a driving voltage code 200 is given to the first data line  $D_1$  by the data driver so that the first pixel (not shown) connected with the first gate line and the first data line can change its brightness. If the sequential frame interval still display the brightness of code 120 and the next frame interval I+1 begins, a control voltage pulse is still given to the first gate line and the driving voltage given to the first data line is decreased to code 120 to keep the expected brightness. The present invention makes use of the "overdrive" concept and

discloses a novel liquid crystal display driving device of matrix structure type and its driving method to reduce the response time of the liquid crystal display.

#### SUMMARY OF THE INVENTION

5       The chief object of the present invention is to provide a liquid crystal display driving device of matrix structure type to increase the response speed of the liquid crystal display and the aspect ratio of the panel and to decrease the number of the data drivers and the data lines.

10       Another object of the present invention is to provide a driving method for the liquid crystal display of matrix structure type, which can simultaneously or synchronously start the plurality of thin film transistors in the display panel and drive the pixels controlled by the thin film transistors to reduce the response time of the liquid crystal display.

15       To achieve the above-stated objects of the present invention, the basic structure of the driving device of the present invention includes a group of thin film transistors with matrix array, gate lines connected with the gate drivers and insulated with each other, wherein the gates and the sources of all the thin film transistors are respectively  
20       connected with the gate lines and the data lines. The response time of the liquid crystal display can be reduced by the different arrangement design of the gate lines and the data lines and by the different connection location between the gate lines and the gates of the thin film transistors and between the data lines and the sources of the thin film transistors. The gate drivers can be respectively installed on the left side and  
25       the right side of the liquid crystal panel and the data drivers can be respectively installed on the upper side and the lower side. The gate driver can be a chip installed on glass or an integrated gate driver circuit installed on glass.

30       The driving method for the said driving device includes: the period of the predetermined voltage of the over drive received by the thin film transistors connected with the first gate line is set as a over exciting period and the period of the data voltage of the present frame interval received by the thin film transistor connected with the first gate line is set as a brightness keeping period.

35       When the over exciting period begins, two gate lines in the liquid crystal display are turned on in a time of one synchronous control signal or by the control signals simultaneously produced by the gate drivers. The predetermined voltage is given to

the thin film transistors connected with one of the gate lines which are simultaneously or synchronously turned on, the data voltage is given to the thin film transistors connected with the other of the gate lines which are simultaneously or synchronously turned on, and scanning continues in turn.

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When the brightness keeping period begins, two gate lines in the liquid crystal display are orderly turned on in a time of one synchronous control signal or by the control signals simultaneously produced by the gate drivers. One of the gate lines is the next gate line of the last gate line given to the said predetermined voltage. The predetermined voltage of over drive is given to the thin film transistors connected with the said gate line, and the data voltage of the present frame interval is given to the thin film transistors connected with the first gate line which is turned on orderly. Scanning continues in turn until the whole liquid crystal display is scanned, and the next frame interval begins.

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If the ratio of the number of the gate lines scanned in the over excited period to the number of the total gate lines is  $P$  and the period of the frame interval of the liquid crystal display is  $T$ , then the duration of the over exciting is  $PT$  and the duration of the brightness keeping is  $(1-P)T$ . The ratio  $P$  can be adjusted according to the characteristic of the display panel.

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From the statement stated above, the present invention possesses the characteristic of dividing the space of the gate lines of the display panel into a plurality of regions and the time of the frame interval into a plurality of sub-region times. Each region is orderly scanned in a time of one synchronous control signal. Therefore, the state of "frame in frame" is formed in the space and the time. The method of the present invention can suit for various picture treatments of liquid crystal display, organic light emitting diode (OLED) display or plasma display panel (PDP).

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To make the present invention be able to be clearly understood, there are some preferred embodiments and their accompanying draws described in detail as below.

#### BRIEF DESCRIPTION OF THE DRAWINGS

35 Fig.1A is a simple schematic view of the structure of the general liquid crystal display;

- Fig.1B is an enlarged schematic sectional view taken from Fig.1A, which shows the arrangement of the elements in the area enveloped in the data lines and the gate lines;
- 5 Fig.2 is a curve view showing the variation of the image brightness of the liquid crystal display with the time at different driving voltages;
- Fig.3A is a comparison view showing the variation of the expected brightness of a pixel with OD technique and without OD technique;
- 10 Fig.3B is a schematic view showing the control voltage pulse of the first gate line from the gate driver of the liquid crystal display in the frame interval of Fig.3A;
- 15 Fig.3C is a schematic view showing the driving voltage of the first data line from the data drivers of the liquid crystal display in the frame interval of Fig.3A;
- Fig.4A is a schematic view showing the arrangement of the gate lines and the data lines of the display panel of the first embodiment according to the present invention;
- 20 Fig.4B is an enlarged schematic sectional view taken from Fig.4A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected to the gate lines and the data lines, of each thin film transistor;
- 25 Fig.4C is an enlarged schematic sectional view taken from Fig.4A, which shows there is a space between the neighboring data lines for preventing them from short circuit;
- 30 Fig.5A is a schematic view of the arrangement of the gate lines and the data lines of the display panel of the first embodiment according to the present invention, which shows the state of the data drivers respectively installed on the upper side and the lower side of the display panel;
- 35 Fig.5B is an enlarged schematic sectional view taken from Fig.5A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected to the gate lines and the data lines, of each thin film transistor;

Fig.6A is a schematic view of the arrangement of the gate lines and the data lines of the display panel of the first embodiment according to the present invention, which shows the state of each pair of data lines connected to a data driver, which is connected to the electronic switch;

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Fig.6B is an enlarged schematic sectional view taken from Fig.6A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected to the gate lines and the data lines, of each thin film transistor;

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Fig.7 is a wave form view of the signal used in the driving method of the display device of the first embodiment according to the present invention, which shows the variation of the wave form of the signal of the gate lines and the data lines from the gate driver and the data drive at different frame interval time;

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Fig.8A is a schematic view of the arrangement of the gate lines and the data lines of the display panel of the second embodiment according to the present invention;

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Fig.8B is an enlarged schematic sectional view taken from Fig.8A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected with the gate lines and the data lines, of each thin film transistor;

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Fig.8C is an enlarged schematic sectional view taken from Fig.8A, which shows there is a space between the neighboring data lines for preventing them from short circuit;

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Fig.9A is a schematic view of the arrangement of the gate lines and the data lines of the display panel of the second embodiment according to the present invention, which shows the state of the data drivers respectively installed on the upper side and the lower side of the display panel;

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Fig.9B is an enlarged schematic sectional view taken from Fig.9A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected with the gate lines and the data lines, of each thin film transistor;

Fig.10A is a schematic view of the arrangement of the gate lines and the data lines of the display panel of the second embodiment according to the present invention, which shows the state of each pair of data lines connected to a data driver, which is connected to the electronic switch;

Fig.10B is an enlarged schematic sectional view taken from Fig.10A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected to the gate lines and the data lines, of each thin film transistor;

Fig.11 is a wave form view of the signal used in the driving method of the display device of the second embodiment according to the present invention, which shows the variation of the wave form of the signal of the gate lines and the data lines from the gate driver and the data driver at different frame interval time;

Fig.12A is a schematic view showing the arrangement of the gate lines and the data lines of the display panel of the third embodiment according to the present invention;

Fig.12B is an enlarged schematic sectional view taken from Fig.12A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected to the gate lines and the data lines, of each thin film transistor;

Fig.12C is an enlarged schematic sectional view taken from Fig.12A, which shows there is a space between the neighboring gate lines to prevent them from short circuit;

Fig.13A is a schematic view of the arrangement of the gate lines and the data lines of the display panel of the third embodiment according to the present invention, which shows the state of the gate drivers respectively installed on the left side and the right side of the display panel;

Fig.13B is an enlarged schematic sectional view taken from Fig.13A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected to the gate lines and the data lines, of each

thin film transistor;

5 Fig.14 is a wave form view of the signal used in the driving method of the display device of the third embodiment according to the present invention, which shows the variation of the wave form of the signal of the gate lines and the data lines from the gate drivers and the data drivers at different frame interval time;

10 Fig.15A is a schematic view showing the arrangement of the gate lines and the data lines of the display panel of the fourth embodiment according to the present invention;

15 Fig.15B is an enlarged schematic sectional view taken from Fig.15A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected to the gate lines and the data lines, of each thin film transistor;

20 Fig.15C is an enlarged schematic sectional view taken from Fig.15A, which shows another arrangement of the gate lines and the data lines of the display panel of the fourth embodiment according to the present invention;

25 Fig.16A is a schematic view of the arrangement of the gate lines and the data line of the display panel of the fourth embodiment according to the present invention, which shows the state of the gate drivers respectively installed the left side and the right side of the display panel;

30 Fig.16B is an enlarged schematic sectional view taken from Fig.16A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected to the gate lines and the data lines, of each thin film transistor;

35 Fig.17 is a wave form view of the signal used in the driving method of the display device of the fourth embodiment according to the present invention, which shows the variation of the wave form of the signal of the gate lines and the data lines from the gate drivers and the data drivers at different frame interval time;

Fig.18 is a wave form view of the signal used in another driving method of the display

device of the third embodiment according to the present invention, which shows the variation of the wave form of the signal of the gate lines and the data lines from the gate drivers and the data drivers at different frame interval time;

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Fig.19A is a schematic view showing the arrangement of the gate lines and the data lines of the display panel of the fifth embodiment according to the present invention;

10 Fig.19B is an enlarged schematic sectional view taken from Fig.19A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected to the gate lines and the data lines, of each thin film transistor;

15 Fig.19C is an enlarged schematic sectional view taken from Fig.19A, which shows there is a space between the neighboring gate lines to prevent them from short circuit;

20 Fig.20A is a schematic view of the arrangement of the gate lines and the data lines of the display panel of the fifth embodiment according to the present invention, which shows the state of the gate drivers respectively installed on the left side and the right side of the display panel;

25 Fig.20B is an enlarged schematic sectional view taken from Fig.20A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected to the gate lines and the data lines, of each thin film transistor;

30 Fig.21 is a wave form view of the signal used in the driving method of the display device of the fifth embodiment according to the present invention, which shows the variation of the wave form of the signal of the gate lines and the data lines from the gate drivers and the data drivers at different frame interval time;

35 Fig.22A is a schematic view showing the arrangement of the gate lines and the data lines of the display panel of the sixth embodiment according to the present invention;

Fig.22B is an enlarged schematic sectional view taken from Fig.22A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected to the gate lines and the data lines, of each thin film transistor;

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Fig.22C is an enlarged schematic sectional view taken from Fig.22A, which shows another arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected to the gate lines and the data lines, of each thin film transistor;

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Fig.22D is an enlarged schematic sectional view taken from Fig.22A, which shows there is a space between the neighboring data lines for preventing them from short circuit;

15 Fig.23A is a schematic view of the arrangement of the gate lines and the data lines of the display panel of the sixth embodiment according to the present invention, which shows the state of the data drivers respectively installed on the upper side and the lower side of the display panel;

20 Fig.23B is an enlarged schematic sectional view taken from Fig.23A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected to the gate lines and the data lines, of each thin film transistor;

25 Fig.24A is a schematic view of the arrangement of the gate lines and the data lines of the display panel of the sixth embodiment according to the present invention, which shows the state of each pair of data lines connected to a data driver, which is connected to the electronic switch;

30 Fig.24B is an enlarged schematic sectional view taken from Fig.24A, which shows the arrangement of the gate lines and the data lines and the state of the gate and the source, which are connected to the gate lines and the data lines, of each thin film transistor;

35 Fig.25 is a wave form view of the signal used in the driving method of the display device of the sixth embodiment according to the present invention, which shows the variation of the wave form of the signal of the gate lines and the data lines from the

gate driver and the data driver at different frame interval time;

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Fig.2, because each liquid crystal display panel has its characteristic and each of brightness of the liquid crystal display panel is produced by a preset driving voltage, it is necessary for the OD driving technique that the brightness variation of the panel at various driving voltages would be measured in advance. On the curve in the Fig.2, the brightness, which is marked 21, 22, 23, 24, and 25, is respectively produced by the voltage  $V_1$ ,  $V_2$ ,  $V_3$ ,  $V_4$ , and  $V_5$ . If need be, the number of the curves about the measured brightness can be increased. The variation data of the curve can be made into a lookup table, which can be stored in the electronic elements of the liquid crystal display and become the base on which the driver can select the voltage to produce the brightness of the panel. The means about this technique can be arbitrarily modified and varied by the persons skilled at this art.

#### The first embodiment

Referring to Fig.4A to 4C, they show a preferred embodiment of the liquid crystal display driving device of matrix structure type according to the present invention. The driving device includes a group of thin film transistors Q with matrix array, which consists of N rows and M columns of thin film transistors, wherein, each thin film transistor Q can drive one pixel, so  $N \times M$  pixels (shown by rectangle with dotted line) can be driven. The first gate line  $G_1$  is connected with the gates of all the thin film transistors Q of the first row, the second gate line  $G_2$  is connected with the gates of all the thin film transistors Q of the second row, and so are the others. Therefore, there are N gate lines connected to gate driver and they are insulated with each other.

The first and the second data lines  $D_1$ ,  $D_1$  of the first group of data lines are respectively connected with the sources of all the thin film transistors Q of the odd and the even rows of the first column. The first and the second data lines  $D_2$ ,  $D_2$  of the second group of data lines are respectively connected with the sources of all the thin film transistors Q of the odd and the even rows of the second column and so are the others. Therefore, in total there are M groups of data lines connected to the data drivers and they are insulated with each other. To prevent the neighboring data lines from short circuit, for example, the second data line  $D_1$  of the first group of data lines and the first data line  $D_2$  of the second group of data lines, a space is given between the neighboring data lines, of which arrangement is shown as Fig. 4C.

As shown in Fig. 4A, the data drivers connected with the data lines are installed on the same side of the display panel. If the scanning frequency is 60 Hz and there are two gate lines being turned on at the same time, the scanning time can be further decreased. Referring to Fig. 5A and 5B, the data drivers are respectively arranged on the upper and the lower sides of the liquid crystal display, and the first and the second data line of each group of data lines are respectively connected with the data drivers of the upper and the lower sides of the liquid crystal display, wherein, the scanning frequency of the data drivers is kept at 60 Hz. Referring to Fig. 6A and 6B, the first data line of each group of data lines and the neighboring second line of another group of data lines are connected with the same data drivers, and the data transfer is switched by an electronic switch S of which scanning frequency is a multiple of 60 Hz, such as 120 Hz, 180 Hz... etc. The form of the gate driver can be a chip on glass or an integrated gate driver circuit on glass.

Referring to Fig.7, in the driving method of the present invention executed by the said device, when time is at frame interval 1, the expected brightness is code120 and  $V_{LC}$  is the driving voltage pulse, the voltage wave form has positive and negative phases due to the driving voltage of the liquid crystal being alternating current. The voltage value will be expressed with code in the following statement. In Fig.7, curve (a) represents the brightness variation of the pixel in response to 5 milliseconds of over drive, curve (b) shows the brightness variation of the pixel in response to 16 milliseconds of over drive, and curve (c) displays the brightness variation of the pixel without over drive. If there are  $2(m+n)$ , i.e.  $N=2(m+n)$ , gate lines in the liquid crystal display, the period of the predetermined voltage of over drive for the thin film transistor connected with the first gate line is set as the over exciting period  $t_1$ , and the period of the data voltage of the present frame interval for the thin film transistor connected with the first gate line is set as the brightness keeping period  $t_2$ .

When the over exciting period  $t_1$  begins, the first gate line  $G_1$  and the  $2n^{\text{th}}$  gate line  $G_{2n}$  are simultaneously turned on, and the predetermined voltage code 200 of over drive for the frame is given to the thin film transistor connected to the first gate line  $G_1$ , the data voltage code 32 of the preceding frame is given to the thin film transistor Q connected to the  $2n^{\text{th}}$  gate line  $G_{2n}$ , in other words, the gate driver gives the control voltage pulse to the first gate line  $G_1$  and the  $2n^{\text{th}}$  gate line  $G_{2n}$  at the same time, the data driver gives the predetermined voltage code 200 to the thin film transistor Q connected to the first gate line  $G_1$ , the data voltage code 32 of the preceding frame is given to the thin film transistor Q connected to the  $2n^{\text{th}}$  gate

line  $G_{2n}$ .

5 In the same manner, the second and the  $(2n+1)^{\text{th}}$  gate lines, the third and the  $(2n+2)^{\text{th}}$  gate lines... the  $(2m-1)^{\text{th}}$  and the  $[2(n+m)-2]^{\text{th}}$  gate lines are turned on in order, and the predetermined voltage code 200 of over drive for the frame is given to the thin film transistors Q connected to the second to the  $(2m-1)^{\text{th}}$  gate lines, the data voltage code 32 of the preceding frame is given to the thin film transistors Q connected to the  $(2n+1)^{\text{th}}$  to the  $[2(m+n)-2]^{\text{th}}$  gate lines.

10 When the brightness keeping period  $t_2$  begins, the  $2m^{\text{th}}$  and the first gate lines  $G_{2m}$ ,  $G_1$  are simultaneously turned on, and the predetermined voltage code 200 is given to the thin film transistor Q connected to the  $2m^{\text{th}}$  gate line  $G_{2m}$ , the data voltage code 120 of the present frame interval is given to the thin film transistor Q connected to the first gate line  $G_1$ . In the same manner, the  $(2m+1)^{\text{th}}$  and the second gate lines, the  $(2m+2)^{\text{th}}$  and the third gate lines... the  $[2(m+n)]^{\text{th}}$  (the last) and the  $(2n-1)^{\text{th}}$  gate lines are turned on in order, and the predetermined voltage code 200 is given to the thin film transistors Q connected to the  $(2m+1)^{\text{th}}$  to the  $[2(m+n)]^{\text{th}}$  (the last) gate lines, the data voltage code 120 is given to the thin film transistors connected to the second to the  $(2n-1)^{\text{th}}$  gate lines by the steps stated above, the response speed of the liquid crystal display can be increased. If the ratio of the number of the gate lines which were scanned in the over exciting period  $t_1$  to the number of the total gate lines is P and the period of the frame interval of the liquid crystal display is T, then the duration of the over exciting is PT and the duration of the brightness keeping is  $(1-P)T$ . The ratio P can be adjusted according the characteristic of the display panel.

### The second embodiment

30 Referring to Fig.8A to 8C, the second embodiment of the liquid crystal display driving device of matrix structure type according to the present invention includes a group of thin film transistors with matrix array, which consist of  $2N$  rows and  $M$  columns of thin film transistors Q, wherein, each thin film transistor Q can drive one pixel so that  $2N \times M$  of pixels (shown by the rectangle with dotted line) can be driven. The first gate line  $G_1$  is connected with the gates of all the thin film transistors Q of the first and the second rows, the second gate line  $G_2$  is connected with the gates of all the thin film transistors Q of the third and the fourth rows, and so are the others. Therefore, total  $N$  gate lines connected to the gate drivers and insulated with each other.

The first and the second data lines  $D_1$ ,  $D_1$  of the first group of data lines are respectively connected with the sources of all the thin film transistors of the odd rows and the even rows of the first column, the first and the second data lines  $D_2$ ,  $D_2$  of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column and so are the others. Therefore, in total there are  $M$  groups of data lines connected to the data drivers and they are insulated with each other. To prevent the neighboring data lines from short circuit, for example, the second data line  $D_1$  of the first group of data lines and the first data line  $D_2$  of the second group of data lines, there is a space between the neighboring data lines, of which arrangement is shown in Fig.8C. By this design, the aspect ratio of the liquid crystal display can be increased.

Referring to Fig.8A, the data drivers connected with the data lines are installed on the same side of the display panel. If the scanning frequency is 60Hz and two gate lines are simultaneously turned on, the scanning time can be further reduced. The arrangement of the data drivers is shown as Fig.9A and 9B. The first and the second data lines of each group of data lines are respectively connected with the data drivers installed on the upper and the lower sides of the liquid crystal display, wherein the scanning frequency of the data drivers is kept at 60Hz. As shown in Fig.10A and 10B, the first data line of each group of data lines and the neighboring second line of another group of data lines are connected with the same drivers, and the data transfer is switched by an electronic switch, of which scanning frequency is a multiple of 60Hz, such as 120 Hz, 180 Hz... etc. The form of the gate driver can be a chip on glass or an integrated gate driver circuit on glass.

Referring to Fig.11, in the driving method of the present invention executed by the said device, when time is at frame interval 1, the expected brightness is code120 and  $V_{LC}$  is the driving voltage pulse. To prevent the driving voltage pulse from confusing with the alternating voltage for driving liquid crystal, the value of the driving voltage pulse will be expressed with code in the following statement. In Fig.11, curve (a) represents the brightness variation of the pixel in response to 5 milliseconds of over drive, curve (b) shows the brightness variation of the pixel in response to 16 milliseconds of over drive, and curve (c) displays the brightness variation of the pixel without over drive.

If there are  $m+n$ , i.e.  $N=m+n$ , gate lines in liquid crystal display, the period of the predetermined voltage of over drive for the thin film transistor connected with the first gate line is set as the over exciting period  $t_1$ , and the period of the data voltage of the

present frame interval for the thin film transistor connected with the first gate line is set as the brightness keeping period  $t_2$ .

5 When the over exciting period  $t_1$  begins, the first and the  $n^{\text{th}}$  gate lines  $G_1, G_n$  are orderly turned on in a synchronous control time. The predetermined voltage code 200 of over drive of the frame and the data voltage code 32 of the preceding frame are respectively given to the thin film transistors Q connected with the first and the  $n^{\text{th}}$  gate lines.

10 In the same manner, the second and the  $(n+1)^{\text{th}}$  gate lines, the third and the  $(n+2)^{\text{th}}$  gate lines... and the  $m^{\text{th}}$  and the  $(m+n-1)^{\text{th}}$  gate lines are turned on, and the predetermined voltage code 200 is given to the thin film transistors Q connected with the second to  $m^{\text{th}}$  gate lines, the data voltage code 32 of the preceding frame is given to the thin film transistors Q connected with the  $(n+1)^{\text{th}}$  to  $(m+n-1)^{\text{th}}$  gate lines.

15 When the brightness keeping period  $t_2$  begins, the  $(m+1)^{\text{th}}$  and the first gate lines  $G_{m+1}, G_1$  are orderly turned on in a synchronous control time. The predetermined voltage code 200 and the data voltage code 120 of the present frame interval are respectively given to the thin film transistors Q connected with the  $(m+1)^{\text{th}}$  and the first gate lines  $G_{m+1}, G_1$ . The  $(m+2)^{\text{th}}$  and the second gate lines, the  $(m+3)^{\text{th}}$  and the third gate lines... and the  $(m+n)^{\text{th}}$  (i.e. the last) and the  $(n-1)^{\text{th}}$  gate lines  $G_{m+n}, G_{n-1}$  are orderly and synchronously turned on. The predetermined voltage code 200 is given to the thin film transistors Q connected with the  $(m+2)^{\text{th}}$  to  $(m+n)^{\text{th}}$  (i.e. the last) gate lines, and the data voltage code 120 is given to the thin film transistors Q connected with the second to the  $(n-1)^{\text{th}}$  gate lines. By this way, the object of increasing response speed of the liquid crystal display can be accomplished.

30 If the ratio of the number of the gate lines scanned in the over exciting period  $t_1$  to the number of the total gate lines is P and the period of the frame interval of the liquid crystal display is T, then the duration of the over exciting is PT and the duration of the brightness keeping is  $(1-P)T$ . The ratio P can be adjusted according the characteristic of the display panel.

### **The third embodiment**

35 Referring to Fig.12A to 12C, the third embodiment of the liquid crystal display driving device of matrix structure type according to the present invention includes a group of thin film transistors with matrix array, which consists of N rows and 2M columns of thin film transistors Q, wherein each thin film transistor can drive one

pixel, so total  $N \times 2M$  of pixels (shown by the rectangle of dotted line). The first and the second gate lines  $G_1, G_1$  of the first group of the gate lines are respectively connected with the gates of all the thin film transistors of the odd columns and the even columns of the first row, the first and the second gate lines  $G_2, G_2$  of the second group of gate lines are respectively connected with the gates of all the transistors Q of the odd columns and the even columns of the second row... and the first and the second gate lines of the  $N^{\text{th}}$  group of gate lines are respectively connected with the gates of all the thin film transistors of the odd columns and the even columns of the  $N^{\text{th}}$  row, therefore, there are in total N groups of gate lines connected to the gate drivers and insulated with each other. The first data line  $D_1$  is connected with the sources of all the thin film transistors Q of the first and the second columns, the second data line  $D_2$  is connected with the sources of all the thin film transistors Q of the third and the fourth columns... and the  $M^{\text{th}}$  data line is connected with the sources of all the thin film transistors Q of the  $(2M-1)^{\text{th}}$  and the  $2M^{\text{th}}$  columns. Therefore, there are in total M data lines connected with the data drivers and insulated with each other. To prevent the neighboring gate lines from short circuit, for example, the first and the second gate lines  $G_1, G_1$  of the first group of gate lines, there is a space between the neighboring gate lines, of which arrangement is shown as Fig.12C. By the arrangement of the device stated above, the number of the data lines and the data drivers can be reduced.

Referring to Fig.12A, the gate drivers connected with the gate lines are installed on the same side of the display panel. Referring to Fig.13A and 13B, the first and the second gate lines of each group of gate lines are respectively given data by two groups of gate drivers, and the two groups of gate drivers are respectively installed on the left side and the right side of the liquid crystal display. The form of the gate driver can be a chip on glass, or an integrated gate driver circuit on glass.

Referring to Fig.14, in the driving method of the present invention executed by the said device, when time is at frame interval 1, the expected brightness is code 120 and  $V_{LC}$  is the driving voltage pulse. To prevent the driving voltage pulse from confusing with the alternating voltage for driving liquid crystal, the value of the driving voltage pulse is expressed with code. In Fig.14, curve (a) expresses the brightness variation of the pixel in response of the 5 milliseconds of over drive, curve (b) shows the brightness variation of the pixel in response of the 16 milliseconds of over drive, and curve (c) displays the brightness variation of the pixel without no over drive.

If there are  $2(m+n)$ , i.e.  $N=2(m+n)$ , gate lines in the liquid crystal display, the period of the predetermined voltage of over drive for the thin film transistor connected with the first gate line of the first group of gate lines is set as the over exciting period  $t_1$ , and the period of the data voltage of the present frame interval received by the thin film transistor connected to the first gate line of the first group of gate lines is set as the brightness keeping period  $t_2$ .

When the over exciting period  $t_1$  begins, the first and the second gate line  $G_1, G_1'$  of the first group of gate lines are orderly turned on in a time of one synchronous control signal. The predetermined voltage code 200 of over drive of the frame is given to the thin film transistors Q connected with the first and the second gate lines of the first group of gate lines, and the first and the second gate lines  $G_n, G_n'$  of the  $n^{\text{th}}$  group of gate lines are orderly turned on by the synchronous control signal. The data voltage code 32 of the preceding frame is given to the thin film transistor Q connected with the first and the second gate lines  $G_n, G_n'$  of the  $n^{\text{th}}$  group of gate lines.

In the same manner, the first and the second gate lines of the second group of gate lines, the first and the second gate lines of the  $(n+1)^{\text{th}}$  gate lines... the first and the second gate lines of the  $(m+n-1)^{\text{th}}$  group of gate lines, the first and the second gate line  $G_{m+1}, G_{m+1}'$  of the  $(m+1)^{\text{th}}$  gate lines are orderly and synchronously turned on. The predetermined voltage code 200 is given to the thin film transistors Q connected with the second to the  $(m+1)^{\text{th}}$  groups of gate lines. The data voltage code 32 of the preceding frame is given to the thin film transistors Q connected with the  $(n+1)^{\text{th}}$  to the  $(m+n-1)^{\text{th}}$  group of gate lines.

When the brightness keeping period  $t_2$  begins, in a time of one synchronous control signal the first and the second gate lines of the first group of gate lines are orderly turned on. The data voltage of the present frame interval is given to the thin film transistors connected with the said gate lines. The first and the second gate lines of the  $(m+2)^{\text{th}}$  group of gate lines are orderly turned on by the synchronous control signal. The predetermined voltage code 200 is given to the thin film transistors Q connected with the said gate lines. The first and the second gate lines of the second group of gate lines, the first and the second gate lines of the  $(m+3)^{\text{th}}$  group of gate lines... the first and the second (i.e. the last) of the  $(m+n)^{\text{th}}$  group of gate lines and the first and the second gate lines of the  $(n-1)^{\text{th}}$  gate lines are orderly and synchronously turned on. The data voltage code 32 of the present frame interval is given to the thin film transistors connected with the second to the  $(n-1)^{\text{th}}$  gate lines. The predetermined

voltage code 200 is given to the thin film transistors Q connected with the  $(m+3)^{\text{th}}$  to the  $(m+n)^{\text{th}}$  gate lines. By use of the steps stated above, the response speed of the liquid crystal display can be increased.

5        If the ratio of the number of the gate lines scanned in the over exciting period  $t_1$  to the number of the total gate lines is P and the period of the frame interval of the liquid crystal display is T, then the over exciting duration is PT and the brightness keeping duration is  $(1-P)T$ . The ratio P can be adjusted according to the characteristic of the display panel.

10

#### **The fourth embodiment**

Referring to Fig.15A and 15B, the fourth embodiment of the liquid crystal display driving device of matrix structure type according to the present invention includes a group of thin film transistors Q with matrix array, which consists of N rows and M columns of thin film transistors Q, wherein each thin film transistor Q can drive one pixel, so total  $2N \times M$  of pixels (shown by the rectangle with dotted line) can be driven. The first gate line  $G_1$  of the first group of gate lines is connected with the gates of all the thin film transistors Q of the first row, the second gate line  $G_2$  of the first group of gate lines is connected with the gates of all the thin film transistors Q of the second row... and the second gate line of the  $N^{\text{th}}$  group of gate lines is connected with the gates of all the thin film transistors Q of the  $2N^{\text{th}}$  row, therefore, there are in total N groups of gate lines connected to gate drivers and insulated with each other.

25        The first and the second data lines  $D_1, D_2$  are respectively connected with the sources of all the thin film transistors Q of the odd and the even rows of the first column, the second and the third data lines  $D_3, D_4$  are respectively connected with the sources of all the thin film transistors Q of the odd and the even rows of the second column... and the  $M^{\text{th}}$  and the  $(M+1)^{\text{th}}$  data lines are respectively connected with the sources of all the thin film transistors Q of the odd and the even rows of the  $M^{\text{th}}$  column, therefore there are in total  $M+1$  data lines connected to the data drivers and insulated with each other.

35        Referring to Fig.15C, which is the other form of the fourth embodiment. It also consists of  $2N$  rows and M columns of thin film transistors Q, wherein each thin film transistor Q can drive one pixel, so total  $2N \times M$  of pixels (shown by rectangle with dotted line) can be driven. The first gate line  $G_1$  of the first group of gate lines is connected with the gates of all the thin film transistors Q of the first row, the second

gate line  $G_2$  of the first group of gate lines is connected with the gates of all the thin film transistors  $Q$  of the second row... and the second gate line of the  $N^{\text{th}}$  gate lines is connected with the gates of all the thin film transistors of the  $N^{\text{th}}$  row, therefore, there are in total  $N$  groups of gate lines connected to the gate drivers and insulated with each other. The first data line  $D_1$  is connected with the sources of all the thin film transistors  $Q$  of the first column, the second data line  $D_2$  is connected with the sources of all the thin film transistors  $Q$  of the second column... and the  $M^{\text{th}}$  data line is connected with the sources of all the thin film transistors  $Q$  of the  $M^{\text{th}}$  column, therefore, there are in total  $M$  data lines connected to the data drivers and insulated with each other.

Referring to Fig.15A, the gate drivers connected with the gate lines are installed on the same side of the display panel. Referring to Fig.16, the first gate lines and the second gate lines of each group of gate lines are respectively given data by two groups of gate drivers, and the said two groups of gate drivers are respectively installed on the left and the right sides of the liquid crystal display. The form of the gate driver can be a chip on glass, or an integrated gate driver circuit on glass.

There are two methods to execute the two forms of the embodiments stated above. Referring to Fig.17, in the first driving method, when time is at frame interval 1, the expected brightness is code 120 and the  $V_{LC}$  is the driving voltage pulse. To prevent the driving voltage from confusing with the alternating voltage for driving liquid crystal, the value of the driving voltage is expressed with code in the following statement. In Fig.17, curve (a) expresses the brightness variation of the pixel in response of the 5 milliseconds of over drive, curve (b) shows the brightness variation of the pixel in response of the 16 milliseconds of over drive, and curve (c) displays the brightness variation of the pixel without no over drive.

If there are  $2(m+n)$ , i.e.  $N=2(m+n)$ , gate lines in liquid crystal display, the period of the predetermined voltage of over drive for the thin film transistors connected with the first gate line of the first group of gate lines is set as the over exciting period  $t_1$ , and the period of data voltage of the present frame interval for the thin film transistors connected with the first gate line of the first groups of gate lines is set as the brightness keeping period  $t_2$ .

When the over exciting period  $t_1$  begins, the first and the second gate lines  $G_1, G_2$  of the first group of gate lines are orderly turned on in a time of one synchronous control signal. The predetermined voltage code 200 of over driver of the

frame is given to the thin film transistors Q connected with the first and the second gate lines  $G_1, G_1'$  of the first group of gate lines.

5 The first and the second gate lines  $G_n, G_n'$  of the  $n^{\text{th}}$  group of gate lines are orderly turned on by the synchronous control signal. The data voltage code 32 of the preceding frame is given to the thin film transistor Q connected with the said gate lines. The first and the second gate lines of the second group of gate lines, the first and the second gate lines of the  $(n+1)^{\text{th}}$  group of gate lines... the first and the second gate lines of the  $(m+n-1)^{\text{th}}$  group of gate lines and the first and the second gate lines  $G_{m+1}, G_{m+1}'$  of the  $(m+1)^{\text{th}}$  group of gate lines are orderly and simultaneously  
10 turned on in a time of synchronous control signal. The predetermined voltage code 200 is given to the thin film transistors Q connected with the second to the  $(m+1)^{\text{th}}$  groups of gate lines. The data voltage code 32 of the preceding frame is given to the thin film transistors Q connected with the  $(n+1)^{\text{th}}$  to the  $(m+n-1)^{\text{th}}$  groups of gate lines.

15 When the brightness keeping period  $t_2$  begins, the first and the second gate lines  $G_1, G_1'$  of the first group of gate are orderly turned on in a time of one synchronous control signal. The data voltage code 120 of the present frame interval is given to the thin film transistors connected with the said gate lines. The first and the second gate lines of the  $(m+2)^{\text{th}}$  group of gate lines are orderly turned on by the synchronous control signal. The predetermined voltage code 200 is given to the thin film transistors connected with the said gate lines. The first and the second gate lines of the second group of gate lines, the first and the second gate lines of the  $(m+3)^{\text{th}}$  group of gate lines... the first and the second gate lines  $G_{m+n}, G_{m+n}'$  of the  $(m+n)^{\text{th}}$  group of gate lines and the first and the second gate lines  $G_{n-1}, G_{n-1}'$  of the  $(n-1)^{\text{th}}$  group of gate lines  
20 are orderly and synchronously turned on. The predetermined voltage code 200 is given to the thin film transistors Q connected with the  $(m+3)^{\text{th}}$  to the last gate lines. The data voltage code 120 of the present frame interval is given to the transistors Q connected with the second to the  $(n-1)^{\text{th}}$  group of gate lines. By use of the steps stated  
25 above, the response speed of the liquid crystal display can be increased.

Referring to Fig.18, it shows the second driving method of the present invention. When time is at frame interval 1, the expected brightness is code 120 and  $V_{LC}$  is the driving voltage pulse. The voltage value is expressed with code in the following  
35 statement to prevent the driving voltage from confusing with the alternating voltage for driving the liquid crystal. In Fig.18, curve (a) expresses the brightness variation of the pixel in response of the 5 milliseconds of over driver, curve (b) shows the brightness variation of the pixel in response of the 16 milliseconds of over driver, and

curve (c) displays the brightness variation of the pixel without over driver. If there are  $2m+2n$ , i.e.  $N=2m+2n$ , gate lines in the liquid crystal display, the period of the predetermined voltage of over driver for the thin film transistors connected with the first gate line of the first group of gate lines is set as the over exciting period  $t_1$ , and  
5 the period of the data voltage of the present frame interval for the thin film transistors connected with the first gate line of the first group of gate lines is set as the brightness keeping period  $t_2$ .

In the over exciting period  $t_1$ , the first gate line  $G_1$  of the first group of gate lines  
10 and the first gate line  $G_n$  of the  $n^{\text{th}}$  group of gate lines are orderly turned on in a time of one synchronous control signal. The predetermined voltage code 200 of over driver of one frame and the data voltage code 32 of the preceding frame are respectively given to the thin film transistors Q connected with the said gate lines. Then the second  
15 gate line  $G_1$  of the first group of gate lines and the second gate line  $G_n$  of the  $n^{\text{th}}$  group of gate lines, the first gate line of the second group of gate lines and the first gate line of the  $(n+1)^{\text{th}}$  group of gate lines... and the second gate line of the  $(m+n-1)^{\text{th}}$  group of gate lines and the second gate line of the  $(m+1)^{\text{th}}$  group of gate lines are  
20 orderly and synchronously turned on by the synchronous control signal. The predetermined voltage code 200 is given to the thin film transistors Q connected with the first to the  $(m+1)^{\text{th}}$  groups of gate lines. The data voltage code 32 of the preceding frame is given to the thin film transistors Q connected with the  $(n+1)^{\text{th}}$  to the  $(m+n-1)^{\text{th}}$  groups of gate lines.

When the brightness keeping period  $t_2$  begins, the first gate line  $G_1$  of the first  
25 group of gate lines and the first gate line of the  $(m+2)^{\text{th}}$  group of gate lines are orderly turned on in a time of one synchronous control signal. The data voltage code 120 of the frame interval and the predetermined voltage code 200 are respectively given to the thin film transistors Q connected with the said gate lines. The second gate line  
30  $G_1$  of the first group of gate lines and the second gate line of the  $(n+2)^{\text{th}}$  group of gate lines, the first gate line of the second group of gate lines and the first gate line of the  $(m+3)^{\text{th}}$  group of gate lines... and the second gate line  $G_{(n-1)}$  of the  $(n-1)^{\text{th}}$  group of  
gate lines and the second (i.e. the last) gate line  $G_{(m+n)}$  of the  $(m+n)^{\text{th}}$  group of gate  
lines are orderly and synchronously turned on. The predetermined voltage code 200 is  
35 given to the thin film transistors Q connected with the  $(m+2)^{\text{th}}$  group to the last gate line  $G_{(m+n)}$ . The data voltage code 120 is given to the thin film transistors Q

connected with the second group of gate lines to the  $(n-1)^{\text{th}}$  group of gate lines. By use of the steps stated above, the response speed of the liquid crystal display can be increased.

5        If the ratio of the number of the gate lines scanned in the over exciting period  $t_1$  to the number of the total gate lines is  $P$  and the period of the frame interval of the liquid crystal display is  $T$ , then the over exciting duration is  $PT$  and the brightness keeping duration is  $(1-P)T$ . The ratio  $P$  can be adjusted according to the characteristic of the display panel.

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#### **The fifth embodiment**

Referring to Fig.19A to 19C, the fifth embodiment of the liquid crystal display driving device of matrix structure type according to the present invention includes a group of thin film transistors  $Q$  with matrix array, which consists of  $N$  rows and  $2M$  columns of thin film transistors  $Q$ . One pixel is driven by two neighboring thin film transistors  $Q$ , therefore total  $N \times M$  of pixels (shown by rectangle with dotted line) can be driven. The first and the second gate lines  $G_1, G_1'$  of the first group of gate lines are respectively connected with the gates of all the thin film transistors  $Q$  of the odd and the even columns of the first row. The first and the second gate lines  $G_2, G_2'$  of the second group of gate lines are respectively connected with the gates of all the thin film transistors  $Q$  of the odd and the even columns of the second row... and the first and the second gate lines of the  $N^{\text{th}}$  group of gate lines are respectively connected with the gates of all the thin film transistors  $Q$  of the odd and the even columns of the  $N^{\text{th}}$  row. Therefore, there are in total  $N$  groups of gate lines connected to the gate drivers and insulated with each other.

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The first data line  $D_1$  is connected with the sources of all the thin film transistors  $Q$  of the first column. The second data line  $D_2$  is connected with the sources of all the thin film transistors  $Q$  of the second column... and the  $2M^{\text{th}}$  data line is connected with the sources of all the thin film transistors  $Q$  of the  $2M^{\text{th}}$  column. Therefore, there are in total  $2M$  data lines connected to the data drivers and insulated with each other. To prevent the neighboring gate lines from short circuit, for example, the first gate line  $G_1$  and the second gate line  $G_1'$  of the first group of gate lines, there is a space between the two neighboring gate lines, of which arrangement is shown as Fig.19C.

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Referring to Fig.19A, the gate drivers connected with the gate lines are installed on the same side of the display panel. Referring to Fig.20A and 20B, the first gate lines and the second gate lines of the each group of gate lines are respectively given

data by two groups of gate drivers, and the said two groups of gate drivers are respectively installed on the left and the right sides of the liquid crystal display. The form of the gate driver can be a chip on glass or an integrated gate driver circuit on glass.

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Referring to Fig.21, the driving method of the present invention can be executed by the device stated above. When time is at frame interval 1, the expected brightness is code 120 and  $V_{LC}$  is the driving voltage pulse. The value of the driving voltage pulse is expressed with code in the following statement to prevent the driving voltage from confusing the alternating voltage for driving liquid crystal. In Fig.21, curve (a) expresses the brightness variation of the pixel in response of 5 milliseconds of over driver, curve (b) shows the brightness variation of the pixel in response of 16 milliseconds of over driver, and curve (c) displays the brightness variation of the pixel without over driver.

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If there are  $2m+2n$ , i.e.  $N=2m+2n$ , gate lines in the liquid crystal display, the period of the predetermined voltage of over driver for the thin film transistors connected with the first gate line of the first group of gate lines is set as the over exciting period  $t_1$ , and the period of the data voltage of the present frame interval for the thin film transistors connected with the second gate line of the first group of gate lines is set as the brightness keeping period  $t_2$ .

20

When the over exciting period  $t_1$  begins, the first gate line  $G_1$  of the first group of gate lines and the second gate line  $G_n$  of the  $n^{\text{th}}$  group of gate lines are orderly turned on in a time of one synchronous control signal. The predetermined voltage code 200 of over driver of the frame and the data voltage code 32 of the preceding frame are respectively given to the thin film transistors Q connected with the said gate lines. The first gate line of the second group of gate lines and the second gate line of the  $(n+1)^{\text{th}}$  group of gate lines, the first gate line of the third group of gate lines and the second gate line of the  $(n+2)^{\text{th}}$  group of gate lines... and the second gate line of the  $(m+n-1)^{\text{th}}$  group of gate lines and the first gate line of the  $(m+1)^{\text{th}}$  group of gate lines are orderly and synchronously turned on in the time of synchronous control signal. The predetermined voltage code 200 is given to the thin film transistors Q connected with the first gate line of the second group to the  $(m+1)^{\text{th}}$  group of gate lines. The data voltage code 32 of the preceding frame is given to the thin film transistors Q connected with the second gate line of the  $(n+1)^{\text{th}}$  group to the  $(m+n-1)^{\text{th}}$  group of gate lines.

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When the brightness keeping period  $t_2$  begins, the second gate line  $G_1$  of the first group of gate lines and the first gate line of the  $(m+2)^{\text{th}}$  group of gate lines are orderly turned on in a time of one synchronous control signal. The data voltage code 120 of the frame interval and the predetermined voltage code 200 are respectively given to the thin film transistors Q connected with the said gate lines. The first gate line of the  $(m+3)^{\text{th}}$  group of gate lines and the second gate line of the second group of gate lines, the first gate line of the  $(m+4)^{\text{th}}$  group of gate lines and the second gate line of the third group of gate lines... and the first gate line of the  $(m+n)^{\text{th}}$  group of gate lines and the second gate line of the  $(n-1)^{\text{th}}$  group of gate lines are orderly and synchronously turned on. The data voltage code 120 of the present frame interval is given to the thin film transistors Q connected with the second gate line of the second group to the  $(n-1)^{\text{th}}$  group of gate lines. The predetermined voltage code 200 is given to the thin film transistors Q connected with the first gate lines of the  $(m+3)^{\text{th}}$  group to the  $(m+n)^{\text{th}}$  group of gate lines. By use of the steps stated above, the response speed of the liquid crystal display can be increased.

If the ratio of the number of the gate lines scanned in the over exciting period  $t_1$  to the number of the total gate lines is P and the frame interval period of the liquid crystal display is T, then the over exciting duration is PT and the brightness keeping duration is  $(1-P)T$ . The ratio P can be adjusted according to the characteristic of the display panel.

#### **The sixth embodiment**

Referring to Fig.22A to 22C, the sixth embodiment of the liquid crystal display driving device of matrix structure type according to the present invention includes a group of thin film transistors Q with matrix array, which consists of N rows and 2M columns of thin film transistors Q. One pixel is driven by two neighboring thin film transistors so that total  $N \times M$  of pixels (shown by the rectangle with dotted line) can be driven. The first and the second gate lines  $G_1, G_2$  are respectively connected with the gates of all the thin film transistors Q of the odd column and the even column of the first row. The second and the third gate lines  $G_2, G_3$  are respectively connected with gates of all the thin film transistors Q of the odd column and the even column of the second row... and the  $N^{\text{th}}$  and the  $(N+1)^{\text{th}}$  gate lines are respectively connected with the gates of all the thin film transistors Q of the odd column and the even column of the  $N^{\text{th}}$  row. Therefore, there are in total N gate lines connected to the gate drivers and insulated with each other.

The first data line  $D_1$  of the first group of data lines is connected with the sources

of all the thin film transistors Q of the first column. The second data line  $D_1$  of the first group of data lines is connected with the sources of all the thin film transistors Q of the second column... and the second data line of the  $M^{\text{th}}$  group of data lines is connected with the sources of all the thin film transistors Q of the  $2M^{\text{th}}$  column.  
5 Therefore, there are in total M groups of data lines connected to the data drivers and insulated with each other.

Referring to Fig.22C, a row of thin film transistors Q can be additionally installed above the first row of thin film transistors Q in the present embodiment.  
10 Each thin film transistor Q can control a pixel. The gates of the said row of thin film transistors Q are connected with the first gate line and their sources are connected with the second data line of each group of data lines. To prevent the neighboring data lines from short circuit, for example, the second data line  $D_1$  of the first group of data lines and the first data line  $D_2$  of the second group of data lines, there is a space  
15 between two neighboring data lines of which arrangement is shown as Fig.22D.

Referring to Fig.22A, the data drivers connected with the data lines are installed on the same side. If the scanning frequency is 60 Hz and two gate lines are simultaneously turned on, the scanning time can be further decreased. The data  
20 drivers can be arranged as shown in Fig.23A and 23B. The first data lines and the second data lines of each group of data lines are respectively connected with the data drivers installed on the upper side and the lower side of the liquid crystal display. The scanning frequency of the data drivers is kept at 60 Hz. As shown in Fig.24A and 24B,  
25 the first data lines and the second data lines of each group of data lines, which are neighboring, are connected with the same data driver. The data transfer is switched by an electronic switch. Its scanning frequency is a multiple of that of the said data driver, for examples, 120 Hz, 180 Hz... etc. The form of the gate driver can be a chip on glass, or an integrated gate driver circuit on glass.

30 The driving method of the present invention is executed by the device stated above. Referring to Fig.25, when time is at the frame interval 1, the expected brightness is code 120 and  $V_{LC}$  is the driving voltage pulse. The value of the driving voltage is expressed with code in the following statement to prevent the driving voltage from confusing the alternating voltage for driving liquid crystal. In Fig.25,  
35 curve (a) expresses the brightness variation of the pixel in response of the 5 milliseconds of over driver, curve (b) shows the brightness variation of the pixel in response of the 16 milliseconds of over driver. Curve (c) displays the brightness variation of the pixel without over driver.

If there are  $m+n$ , i.e.  $N=m+n$ , gate lines in the liquid crystal display, the period of the predetermined voltage of over driver for the thin film transistor connected with the first gate line is set as the over exciting period  $t_1$  and the period of the data voltage of the present frame interval received by the thin film transistors connected with the first gate line is set as the brightness keeping period  $t_2$ .

In the over exciting period  $t_1$ , the first and the  $(n+1)^{\text{th}}$  gate lines  $G_1, G_{n+1}$  are orderly turned on in a time of one synchronous control signal. The predetermined voltage code 200 and the data voltage code 32 of the preceding frame are respectively given to the thin film transistors Q connected with the said gate lines. The second and the  $(n+2)^{\text{th}}$  gate lines, the third and the  $(n+3)^{\text{th}}$  gate lines... and the  $(m+n-1)^{\text{th}}$  and the  $m^{\text{th}}$  gate lines are orderly and synchronously turned on in the time of synchronous control signal. The predetermined voltage code 200 is given to the thin film transistors connected with the second to the  $m^{\text{th}}$  gate lines. The data voltage code 32 of the preceding frame is given to the thin film transistors Q connected with the  $(n+2)^{\text{th}}$  to the  $(m+n-1)^{\text{th}}$  gate lines.

During the brightness keeping period  $t_2$ , the first gate line and the  $(m+1)^{\text{th}}$  gate line are orderly turned on in a time of one synchronous control signal. The data voltage code 120 of the frame interval and the predetermined voltage code 200 are respectively given to the thin film transistors Q connected with the said gate lines. The second and the  $(m+2)^{\text{th}}$  gate lines, the third and the  $(m+3)^{\text{th}}$  gate lines... and the  $(m+n)^{\text{th}}$  (i.e. the last) and the  $n^{\text{th}}$  gate lines are orderly turned on. The predetermined voltage code 200 is given to the thin film transistors Q connected with the  $(m+2)^{\text{th}}$  to the  $(m+n)^{\text{th}}$  (the last) gate lines. The data voltage code 120 is given to the thin film transistors Q connected with the second to the  $n^{\text{th}}$  gate lines. By use of the steps stated above, the response speed of the liquid crystal display can be increased.

If the number of the gate lines scanned in the over exciting period  $t_1$  to the number of the total gate lines is  $P$  and the frame interval time of the liquid crystal display is  $T$ , then the over exciting duration is  $PT$  and the brightness keeping duration is  $(1-p)T$ . The ratio  $P$  can be adjusted according to the characteristic of the display panel.

The present invention can quickly drive the liquid crystal display and increase the response speed of the image gray level by the division of the time (frame interval time) and space (gate lines) and the application of the predetermined voltage and data

voltage in the steps stated above. The driving method according to the present invention can suit for various liquid crystal display, active matrix type liquid crystal display, organic light emitting diode (OLED) display or plasma display panel (PDP).

5       The “frame in frame” technique of the present invention has been described by the above embodiments, but they cannot be used to limit the present invention. Any persons skilled at the art related to the present invention can make partial modification and variation without departing from the spirit and the scope of the present invention. The patent scope of the present invention should take the accompanying claims as the  
10       criterion.

Therefore, the present invention has the following advantages:

1. The liquid crystal display driving device of matrix structure type according to the present invention can increase both the response speed of the liquid crystal panel  
15       and the aspect ratio of the panel, but decrease both the number of the data drivers and the data lines and the production cost.
2. The driving method for the liquid crystal display of matrix structure type according to the present invention can simultaneously or synchronously turn on two rows of  
20       thin film transistors and the pixel of the panel can be driven by the thin film transistors, so the object of reducing the response time of the liquid crystal display can be accomplished.

To sum up, the present invention indeed can accomplish its expected object of  
25       providing a liquid crystal display driving device of matrix structure type and its driving method to increase the response speed. It has high utilization value in industry, so it is brought forward claiming patent right.

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WHAT IS CLAIMED IS:

1. A liquid crystal display driving device of matrix structure type including:
  - a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that  $N \times M$  of pixels can be driven;
  - a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row... and the N<sup>th</sup> gate line is connected with the gates of all the thin film transistors of the N<sup>th</sup> row; and
  - M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second data lines of the first group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column... and the first and the second data lines of the M<sup>th</sup> group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M<sup>th</sup> column.
2. The liquid crystal display driving device of matrix structure type as claimed in claim 1, wherein the first and the second data lines of each group of data lines are given data by two groups of source drivers, respectively, and the two groups of source drivers are respectively arranged on the upper and the lower sides of the liquid crystal display.
3. The liquid crystal display driving device of matrix structure type as claimed in claim 1, wherein the first data lines and the second data lines of each group of data lines are connected with the same source driver, each source driver is installed on the same side of the display panel and the data transfer is switched by an electronic switch.
4. The liquid crystal display driving device of matrix structure type as claimed in claim 1, wherein there is a space between the neighboring data lines to prevent them from short circuit.
5. The liquid crystal display driving device of matrix structure type as claimed in claim 1, wherein the gate driver is a chip installed on glass.

6. The liquid crystal display driving device of matrix structure type as claimed in claim 1, wherein the gate driver is an integrated gate driver circuit installed on glass.

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7. A driving method for the liquid crystal display of matrix structure type including:

a. making use of the liquid crystal display driving device as claimed in claim 1, wherein there are  $2(m+n)$ , i.e.  $N=2(m+n)$ , gate lines in the liquid crystal display, the period of the predetermined voltage of over drive received by the thin film transistor connected with the first gate line is set as a over exciting period, and the period of the data voltage of the present frame interval received by the thin film transistor connected with the first gate line is set as a brightness keeping period;

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b. when the over exciting period begins, the first gate line and the  $2n^{\text{th}}$  gate line are simultaneously turned on, the predetermined voltage of the over drive for the frame is given to the thin film transistor connected with the first gate line, the data voltage of the preceding frame is given to the thin film transistor connected with the  $2n^{\text{th}}$  gate line, and the second and the  $(2n+1)^{\text{th}}$  gate lines, the third and the  $(2n+2)^{\text{th}}$  gate lines... and the  $(2m-1)^{\text{th}}$  and the  $[2(m+n)-2]^{\text{th}}$  gate lines are orderly and simultaneously turned on, the predetermined voltage is given to the thin film transistors connected with the second to the  $(2m-1)^{\text{th}}$  gate lines, the data voltage of the preceding frame is given to the thin film transistors connected with the  $(2n+1)^{\text{th}}$  to the  $[2(m+n)-2]^{\text{th}}$  gate lines;

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c. when the brightness keeping period begins, the  $2m^{\text{th}}$  and the first gate lines are simultaneously turned on, the predetermined voltage is given to the thin film transistors connected with the  $2m^{\text{th}}$  gate line, the data voltage of the preceding frame interval is given to the thin film transistors connected with the first gate line, and the  $(2m+1)^{\text{th}}$  and the second gate lines, the  $(2m+2)^{\text{th}}$  and the third gate lines... and the  $[2(m+n)]^{\text{th}}$  (the last) and the  $(2n-1)^{\text{th}}$  gate lines are orderly and simultaneously turned on, the predetermined voltage is given to the thin film transistors connected with the  $(2m+1)^{\text{th}}$  to the  $[2(m+n)]^{\text{th}}$  (the last) gate lines, the data voltage of the present frame interval is given to the thin film transistors connected with the second and the  $(2n-1)^{\text{th}}$  gate lines;

by using of the steps stated above, the response speed of the liquid crystal display can be increased.

8. The driving method for liquid crystal display of matrix structure type as claimed in claim 7, wherein the driving method suits for the active matrix type liquid crystal display, the organic light emitting diode (OLED) display or plasma display panel (PDP).

9. A liquid crystal display driving device of matrix structure type including:  
a group of thin film transistors with matrix array consisting of  $2N$  rows and  $M$  columns of thin film transistors, wherein each transistor can drive one pixel, therefore, total  $2N \times M$  of pixels can be driven;

a group of  $N$  gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first and the second rows, the second gate line is connected with the gates of all the thin film transistors of the third and the fourth rows... and the  $N^{\text{th}}$  gate line is connected with the gates of all the thin film transistors of the  $(2N-1)^{\text{th}}$  and the  $(2N)^{\text{th}}$  rows; and

$M$  groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second data lines of the first group of data lines are respectively connected with the sources of all the thin film transistors of the odd rows and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd rows and the even rows of the second column... and the first and the second data lines of the  $M^{\text{th}}$  groups of data lines are respectively connected with the sources of all the thin film transistors of the odd rows and the even rows of the  $M^{\text{th}}$  column.

10. The liquid crystal display driving device of matrix structure type as claimed in claim 9, wherein the first data line of each group of data lines and the second data line of each group of data lines are respectively given data from two groups of source drivers, the two groups of source drivers are respectively installed on the upper side and the lower side of the liquid crystal display.

11. The liquid crystal display driving device of matrix structure type as claimed in claim 9, wherein the first data line and the second data line of each group of data lines are connected with the same source driver, each source driver is installed on the same side of the display panel and the data transfer is switched by an electronic switch.

12. The liquid crystal display driving device of matrix structure type as claimed in claim 9, wherein there is a space between the neighboring data lines to prevent them from short circuit.
- 5 13. The liquid crystal display driving device of matrix structure type as claimed in claim 9, wherein the gate driver is a chip installed on glass.
14. The liquid crystal display driving device of matrix structure type as claimed in claim 9, wherein the gate driver is an integrated gate driver circuit installed on  
10 glass.
15. A driving method for the liquid crystal display of matrix structure type including:
- 15 a. making use of the liquid crystal display driving device as claimed in claim 9, wherein there are  $m+n$ , i.e.  $N=m+n$ , gate lines in the liquid crystal display, the period of the predetermined voltage of the over drive received by the thin film transistors connected with the first gate line is set as a over exciting period, and the period of the data voltage of the present frame interval received by the thin film transistor connected with the first gate line is set as a brightness keeping period;
- 20 b. when the over exciting period begins, the first and the  $n^{\text{th}}$  gate lines are orderly turned on in a time of one synchronous control signal, the predetermined voltage of the over drive for the frame and the data voltage of the preceding frame are respectively given to the thin film transistor connected with the first and the  $n^{\text{th}}$  gate lines, and the second and the  $(n+1)^{\text{th}}$  gate lines, the third and the  $(n+2)^{\text{th}}$  gate lines... and the  $m^{\text{th}}$  and the  $(m+n-1)^{\text{th}}$  gate lines are orderly turned on in a time of synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the second to the  $m^{\text{th}}$  gate lines, the data voltage of the preceding frame is given to the thin film transistors  
25 connected with the  $(n+1)^{\text{th}}$  to the  $(m+n-1)^{\text{th}}$  gate lines;
- 30 c. when the brightness keeping period begins, the  $(m+1)^{\text{th}}$  and the first gate lines are orderly turned on in a time of one synchronous control signal, the predetermined voltage and the data voltage of the present frame interval are respectively given to the thin film transistors connected with the  $(m+1)^{\text{th}}$  and the first gate lines, and the  $(m+2)^{\text{th}}$  and the second gate lines, the  $(m+3)^{\text{th}}$  and the third gate lines... and the  $(m+n)^{\text{th}}$  (the last) and the  $(n-1)^{\text{th}}$  gate lines are orderly and synchronously turned on, the predetermined voltage is given to the thin film  
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transistors connected with the  $(m+2)^{\text{th}}$  to the  $(m+n)^{\text{th}}$  (the last) gate lines, the data voltage of the present frame interval is given to the thin film transistors connected with the second to the  $(n-1)^{\text{th}}$  gate lines;

5           by using of the steps stated above, the response speed of the liquid crystal display can be increased.

16. The driving method for the liquid crystal display of matrix structure type as claimed in claim 15, wherein the driving method suits for the active matrix type liquid crystal display, the organic light emitting diode (OLED) display or the plasma display panel (PDP).

17. A liquid crystal display driving device of matrix structure type including:  
a group of thin film transistors with matrix array consisting of  $N$  rows and  $2M$  columns of thin film transistors, wherein each thin film transistor can drive one pixel, therefore total  $N \times 2M$  of pixels can be driven;  
 $N$  groups of gate lines connected with the gate drivers and insulated with each other, wherein the first and the second gate lines of the first group of gate lines are respectively connected with the gates of all the thin film transistors of the odd column and the even column of the first row, the first and the second gate lines of the second group of gate lines are respectively connected with the gates of all the thin film transistors of the odd column and the even column of the second row... and the first and the second gate lines of the  $N^{\text{th}}$  group of gate lines are respectively connected with the gates of all the thin film transistors of the odd column and the even column of the  $N^{\text{th}}$  row; and  
a group of  $M$  data lines connected with the source drivers and insulated with each other, wherein the first date line is connected with the sources of all the thin film transistors of the first column and the second column, the second date lines is connected with the sources of all the thin film transistors of the third column and the fourth column... and the  $M^{\text{th}}$  data line is connected with the sources of all the thin film transistors of the  $(2M-1)^{\text{th}}$  column and the  $2M^{\text{th}}$  column.

18. The liquid crystal display driving device of matrix structure type as claimed in claim 17, wherein the first gate lines and second gate lines of each group of gate lines are respectively given data by two groups of gate drivers, the two groups of gate drivers are respectively installed on the left side and the right side of the liquid crystal display.

19. The liquid crystal display driving device of matrix structure type as claimed in claim 17, wherein there is a space between the neighboring gate lines to prevent them from short circuit.
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20. The liquid crystal display driving device of matrix structure type as claimed in claim 17, wherein the gate driver is a chip installed on glass.
21. The liquid crystal display driving device of matrix structure type as claimed in claim 17, wherein the gate driver is an integrated gate driver circuit installed on glass.
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22. A driving method for the liquid crystal display of matrix structure type including:
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- a. making use of the liquid crystal display driving device as claimed in claim 17, wherein there are  $2(m+n)$ , i.e.  $N=2(m+n)$ , gate lines in the liquid crystal display, the period of predetermined voltage of the over drive received by the thin film transistors connected with the first gate line of the first group of gate lines is set as a over exciting period, and the period of the data voltage of the present frame interval received by the thin film transistors connected with the first gate line of the first group of gate lines is set as a brightness keeping period;
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- b. when the over exciting period begins, the first and the second gate lines of the first group of gate lines are orderly turned on in a time of synchronous control signal, the predetermined voltage of the over drive for the frame is given to the thin film transistors connected with the gate lines, and the first and the second gate lines of the  $n^{\text{th}}$  group of gate lines are orderly turned on by the synchronous control signal, the data voltage of the preceding frame is given to the thin film transistors connected with the gate lines, and the first and second gate lines of the second group of gate lines, the first and the second gate lines of the  $(n+1)^{\text{th}}$  group of gate lines... the first and the second gate lines of the  $(m+n)^{\text{th}}$  group of gate lines are orderly turned on in a time of synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the second group to the  $(m+1)^{\text{th}}$  group of gate lines, the data voltage of the preceding frame is given to the thin film transistors connected with the  $(n+1)^{\text{th}}$  group to the  $(m+n-1)^{\text{th}}$  group of gate lines;
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- c. when the brightness keeping period begins, the first and the second gate lines of the first group of gate lines are orderly turned on in a time of one synchronous

control signal, the data voltage of the present frame interval is given to the thin film transistors connected with the gate lines, and the first and the second gate lines of the  $(m+2)^{\text{th}}$  group of gate lines are orderly turned on by the synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the gate lines, and the first and the second gate lines of the second group of gate lines, the first and the second gate lines of the  $(m+3)^{\text{th}}$  group of gate lines... the first and the second gate lines of the  $(n-1)^{\text{th}}$  group of gate lines and the first and the second (i.e. the last) gate lines of the  $(m+n)^{\text{th}}$  group of gate lines are orderly and synchronously turned on, the data voltage of the present frame interval is given to the thin film transistors connected with the second group to the  $(n-1)^{\text{th}}$  group of gate lines, the predetermined voltage is given to the thin film transistors connected with the  $(m+4)^{\text{th}}$  group to the  $(m+n)^{\text{th}}$  group of gate lines;

by using of the steps stated above, the response speed of the liquid crystal display can be increased.

23. The driving method for the liquid crystal display of matrix structure type as claimed in claim 22, wherein the driving method suits for the active matrix type liquid crystal display, the organic light emitting diode (OLED) display or plasma display panel (PDP).

24. A the liquid crystal display driving device of matrix structure type including:  
a group of thin film transistors with matrix array consisting of  $2N$  rows and  $M$  columns of thin film transistors, wherein each transistor can drive one pixel, therefore total  $2N \times M$  of pixels can be driven;

$N$  groups of gate lines connected with the gate drivers and insulated with each other, wherein the first gate line of the first group of gate lines is connected with the gates of all the thin film transistors of the first row, the second gate line of the first group of gate lines is respectively connected with the gates of all the thin film transistors of the second row... and the second gate line of the  $N^{\text{th}}$  group of gate lines is respectively connected with the gates of all the thin film transistors of the  $2N^{\text{th}}$  row; and

a group of  $M+1$  data lines connected with the source drivers and insulated with each other, wherein the first and the second data lines are respectively connected with the sources of all the thin film transistors of the odd rows and the even rows

of the first column, the second and the third data lines are respectively connected with the sources of all the thin film transistors of the odd rows and the even rows of the second column... and the  $M^{\text{th}}$  and the  $(M+1)^{\text{th}}$  gate lines are respectively connected with the sources of all the thin film transistors of the odd rows and the even rows of the  $M^{\text{th}}$  column.

25. A the liquid crystal display driving device of matrix structure type as claimed in claim 24, wherein the first gate lines and the second gate lines of each group of gate lines are respectively given data by two groups of gate drivers, the two groups of gate drivers are respectively installed on the left side and the right side of the liquid crystal display.

26. A the liquid crystal display driving device of matrix structure type as claimed in claim 24, wherein the gate driver is a chip installed on glass.

27. A the liquid crystal display driving device of matrix structure type as claimed in claim 24, wherein the gate driver is an integrated gate driver circuit installed on glass.

28. A the liquid crystal display driving device of matrix structure type including:  
a group of thin film transistors with matrix array consisting of  $2N$  rows and  $M$  columns of thin film transistors, wherein each transistor can drive one pixel, therefore total  $2N \times M$  of pixels can be driven;

$N$  groups of gate lines connected with the gate drivers and insulated with each other, wherein the first gate line of the first group of gate lines is connected with the gates of all the thin film transistors of the first row, the second gate line of the first group of gate lines is respectively connected with the gates of all the thin film transistors of the second row... and the second gate line of the  $N^{\text{th}}$  group of gate lines is respectively connected with the gates of all the thin film transistors of the  $N^{\text{th}}$  row; and

a group of  $M$  data lines connected with the source drivers and insulated with each other, wherein the first data line is connected with the sources of all the thin film transistors of the first column, the second data line is connected with the sources of all the thin film transistors of the second column... and the  $M^{\text{th}}$  gate line is respectively connected with the sources of all the thin film transistors of the  $M^{\text{th}}$  column.

29. A the liquid crystal display driving device of matrix structure type as claimed in claim 28, wherein the first gate lines and the second gate lines of each group of gate lines are respectively given data by two groups of gate drivers, the two groups of gate drivers are respectively installed on the left side and the right side of the liquid crystal display.
30. The liquid crystal display driving device of matrix structure type as claimed in claim 28, wherein the gate driver is a chip installed on glass.
31. The liquid crystal display driving device of matrix structure type as claimed in claim 28, wherein the gate driver is an integrated gate driver circuit installed on glass.
32. A driving method for liquid crystal display of matrix structure type including:
- a. making use of the liquid crystal display driving device as claimed in claim 24 or 28, wherein there are  $2m+2n$ , i.e.  $N=2m+2n$ , gate lines in the liquid crystal display, the period of predetermined voltage of the over drive received by the thin film transistors connected with the first gate line of the first group of gate lines is set as a over exciting period, the period of the data voltage of the present frame interval received by the thin film transistors connected with the first gate line of the first group of gate lines is set as a brightness keeping period;
  - b. when the over exciting period begins, the first and the second gate lines of the first group of gate lines are orderly turned on in a time of one synchronous control signal, the predetermined voltage of the over drive for the frame is given to the thin film transistors connected with the gate lines, and the first and the second gate lines of the  $n^{\text{th}}$  group of gate lines are orderly turned on by the synchronous control signal, the data voltage of the preceding frame is given to the thin film transistors connected with the gate lines, and the first and the second gate lines of the second group of gate lines, the first and the second gate lines of the  $(n+1)^{\text{th}}$  group of gate lines... the first and the second gate lines of the  $(m+n-1)^{\text{th}}$  group of gate lines and the first and the second gate lines of the  $(m+1)^{\text{th}}$  group of gate lines are orderly turned on in a time of the synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the second group to the  $(m+1)^{\text{th}}$  group of gate lines, the data voltage of the preceding frame is given to the thin film transistors connected with the  $(n+1)^{\text{th}}$  group to the  $(m+n-1)^{\text{th}}$  group of gate lines;

5 c. when the brightness keeping period begins, the first and the second gate lines of the first group of gate lines are orderly turned on in a time of one synchronous control signal, the data voltage of the present frame interval is given to the thin film transistors connected with the gate lines, and the first and the second gate lines of the (m+2)<sup>th</sup> group of gate lines are orderly turned on by the synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the gate lines, and the first and the second gate lines of the second group of gate lines, the first and the second gate lines of the (m+3)<sup>th</sup> group of gate lines... the first and the second gate lines of the (m+n)<sup>th</sup> group of gate lines and the first and the second gate lines of the (n-1)<sup>th</sup> group of gate lines are orderly and synchronously turned on, the predetermined voltage is given to the thin film transistors connected with the (m+3)<sup>th</sup> group to the last gate line, the data voltage of the present frame interval is given to the thin film transistors connected with the second group to the (n-1)<sup>th</sup> group of gate lines;

by using of the steps stated above, the response speed of the liquid crystal display can be increased.

20 33. The driving method for liquid crystal display of matrix structure type as claimed in claim 32, wherein the driving method suits for the active matrix type liquid crystal display, the organic light emitting diode (OLED) display or plasma display panel (PDP).

25 34. A driving method for liquid crystal display of matrix structure type including:  
a. making use of the liquid crystal display driving device as claimed in claim 24 or 28, wherein there are  $2m+2n$ , i.e.  $N=2m+2n$ , gate lines in the liquid crystal display, the period of predetermined voltage of the over drive received by the thin film transistors connected with the first gate line of the first group of gate lines is set as a over exciting period, the period of the data voltage of the present frame interval received by the thin film transistors connected with the first gate line of the first group of gate lines is set as a brightness keeping period;

30  
35 b. when the over exciting period begins, the first gate line of the first group of gate lines and the first gate line of the n<sup>th</sup> group of gate lines are orderly turned on in a time of one synchronous control signal, the predetermined voltage of the over drive for the frame and the data voltage of the preceding frame are

5 respectively given to the thin film transistors connected with the gate lines,  
and the second gate line of the first group of gate lines and the second gate line  
of the  $n^{\text{th}}$  group of gate lines, the first gate line of the second group of gate  
lines and the first gate line of the  $(n+1)^{\text{th}}$  group of gate lines... and the second  
10 gate line of the  $(m+n-1)^{\text{th}}$  group of gate lines and the second gate lines of the  
 $(m+1)^{\text{th}}$  group of gate lines are orderly and synchronously turned on by the  
synchronous control signal, the predetermined voltage is given to the thin film  
transistors connected with the first group to the  $(m+1)^{\text{th}}$  group of gate lines, the  
data voltage of the preceding frame is given to the thin film transistors  
15 connected with the  $(n+1)^{\text{th}}$  group to the  $(m+n-1)^{\text{th}}$  group of gate lines;

20 c. when the brightness keeping period begins, the first gate line of the first group  
of gate lines and the first gate line of the  $(m+2)^{\text{th}}$  group of gate lines are  
orderly turned on in a time of one synchronous control signal, the data voltage  
of the frame interval and the predetermined voltage are respectively given to  
the thin film transistors connected with the gate lines, and the second gate line  
of the first group of gate lines and the second gate line of the  $(m+2)^{\text{th}}$  group of  
gate lines, the first gate line of the second group of gate lines and the first gate  
line of the  $(m+3)^{\text{th}}$  group of gate lines... and the second gate line of the  $(n-1)^{\text{th}}$   
25 group of gate lines and the second (i.e. the last) gate line of the  $(m+n)^{\text{th}}$  group  
gate lines are orderly and synchronously turned on, the data voltage of the  
present frame interval is given to the thin film transistors connected with the  
second group to the  $(n-1)^{\text{th}}$  group of gate lines, the predetermined voltage is  
given to the thin film transistors connected with the  $(m+2)^{\text{th}}$  group to the last  
gate lines;

by using of the steps stated above, the response speed of the liquid crystal  
display can be increased.

30 35. The driving method for the liquid crystal display of matrix structure type as  
claimed in claim 34, wherein the driving method suits for the active matrix type  
liquid crystal display, the organic light emitting diode (OLED) display or the  
plasma display panel (PDP).

35 36. A liquid crystal display driving device of matrix structure type including:  
a group of thin film transistors with matrix array consisting of  $N$  rows and  $2M$   
columns of thin film transistors, wherein each pair of neighboring thin film  
transistors can drive one pixel, therefore, total  $N \times M$  of pixels can be driven;

5 N groups of gate lines connected with the gate drivers and insulated with each other, wherein the first and the second gate line of the first group of gate lines are respectively connected with the gates of all the thin film transistors of the odd column and the even column of the first row, the first and the second gate lines of the second group of gate lines are respectively connected with the gates of all the thin film transistors of the odd column and the even column of the second row... and the first and the second gate lines of the N<sup>th</sup> group of gate lines are respectively connected with the gates of all the thin film transistors of the odd column and the even column of the N<sup>th</sup> row; and

15 a group of 2M data lines connected with the source drivers and insulated with each other, wherein the first data line is connected with the sources of all the thin film transistors of the first column, the second data line is connected with the sources of all the thin film transistors of the second column... and the 2M<sup>th</sup> data line is connected with the sources of all the thin film transistors of the 2M<sup>th</sup> column.

20 37. The liquid crystal display driving device of matrix structure type as claimed in claim 36, wherein the first gate lines and the second gate lines of each group of gate lines are respectively given data by two groups of gate drivers, the two groups of gate drivers are respectively installed on the left side and the right side of the liquid crystal display.

25 38. The liquid crystal display driving device of matrix structure type as claimed in claim 36, wherein there is a space between the neighboring gate lines to prevent them from short circuit.

30 39. The liquid crystal display driving device of matrix structure type as claimed in claim 36, wherein the gate driver is a chip installed on glass.

35 40. The liquid crystal display driving device of matrix structure type as claimed in claim 36, wherein the gate drive is an integrated gate driver circuit installed on glass.

41. A driving method for the liquid crystal display driving device of matrix structure type including:  
a. making use of the liquid crystal display driving device as claimed in claim 36,

wherein there are  $2(m+n)$ , i.e.  $N=2(m+n)$ , gate lines in the liquid crystal display, the period of the predetermined voltage of the over drive received by the thin film transistors connected with the first gate line of the first group of gate lines is set as a over exciting period, and the period of the data voltage of the present frame interval received by the thin film transistors connected with the second gate line of the first group of gate lines is set as a brightness keeping period;

b. when the over exciting period begins, the first gate line of the first group of gate lines and the second gate line of the  $n^{\text{th}}$  group of gate lines are orderly turned on in a time of one synchronous control signal, the predetermined voltage of the over drive for the frame and the data voltage of the preceding frame are respectively given to the thin film transistors connected with the gate lines, and the first gate line of the second group of gate lines and the second gate line of the  $(n+1)^{\text{th}}$  group of gate lines, the first gate line of the third group of gate lines and the second gate line of the  $(n+2)^{\text{th}}$  group of gate lines... and the second gate line of the  $(m+n-1)^{\text{th}}$  group of gate lines and the first gate line of the  $(m+1)^{\text{th}}$  group of gate lines are orderly turned on in a time of the synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the first gate line of the second group to the  $(m+1)^{\text{th}}$  group of gate lines, the data voltage of the preceding frame is given to the thin film transistors connected with the second gate line of the  $(n+1)^{\text{th}}$  group to the  $(m+n-1)^{\text{th}}$  group of gate lines;

c. when the brightness keeping period begins, the second gate line of the first group of gate lines and the first gate line of the  $(m+2)^{\text{th}}$  group of gate lines are orderly turned on in a time of one synchronous control signal, the data voltage of the frame interval and the predetermined voltage are respectively given to the thin film transistors connected with the gate lines, and the first gate line of the  $(m+3)^{\text{th}}$  group of gate lines and the second gate line of the second group of gate lines, the first gate line of the  $(m+4)^{\text{th}}$  group of gate lines and the second gate line of the third group of gate lines... and the first gate line of the  $(m+n)^{\text{th}}$  group of gate lines and the second gate line of the  $(n-1)^{\text{th}}$  group of gate lines are orderly and synchronously turned on, the data voltage of the present frame interval is given to the thin film transistors connected with the second gate line of the second group to the  $(n-1)^{\text{th}}$  group of gate lines, the predetermined voltage is given to the thin film transistors connected with the first gate line of the  $(m+3)^{\text{th}}$  group to the  $(m+n)^{\text{th}}$  group of gate lines;

by using of the steps stated above, the response speed of the liquid crystal display can be increased.

5 42. The driving method for the liquid crystal display of matrix structure type as claimed in claim 41, wherein the driving method suits for the active matrix type liquid crystal display, the organic light emitting diode (OLED) display or plasma display panel (PDP).

10 43. A liquid crystal display driving device of matrix structure type including:  
a group of thin film transistors with matrix array consisting of N rows and 2M columns of thin film transistors, wherein each pair of neighboring thin film transistors can drive one pixel, therefore total  $N \times M$  of pixels can be driven;  
a group of N gate lines connected with the gate drivers and insulated with each other, wherein the first and the second gate lines are respectively connected with  
15 the gates of all the thin film transistors of the odd column and the even column of the first row, the second and the third gate lines are respectively connected with the gates of all the thin film transistors of the odd columns and the even columns of the second row... and the  $N^{\text{th}}$  and the  $(N+1)^{\text{th}}$  gate lines are respectively connected with the gates of all the thin film transistors of the odd columns and  
20 the even columns of the  $N^{\text{th}}$  row; and  
M group of data lines connected with the source drivers and insulated with each other, wherein the first data line of the first group of data lines is connected with the sources of all the thin film transistors of the first column, the second data line of the first group of data lines is connected with the sources of all the thin film  
25 transistors of the second column... and the second data line of the  $M^{\text{th}}$  group of data lines is connected with the sources of all the thin film transistors of the odd rows and the even rows of the  $2M^{\text{th}}$  column.

30 44. The liquid crystal display driving device of matrix structure type as claimed in claim 43, wherein there further is one row of thin film transistors installed above the first row of thin film transistors, each thin film transistor can control one pixel, the gates of the row of thin film transistors are connected with the first gate line and their sources are connected with the second data line of each group of data lines.

35 45. The liquid crystal display driving device of matrix structure type as claimed in claim 43, wherein the first data lines and the second data lines of each group of data lines are respectively given data by two groups of source drivers, and the two

groups of source drivers are respectively installed on the upper side and the lower side of the liquid crystal display.

5 46. The liquid crystal display driving device of matrix structure type as claimed in claim 44, wherein the first data line and the second data lines of each group of data lines are respectively given data by two groups of source drivers, and the two groups of source drivers are respectively installed on the upper side and the lower side of the liquid crystal display.

10 47. The liquid crystal display driving device of matrix structure type as claimed in claim 43, wherein the first data lines of each group of data lines and the second data lines of each group of data lines are connected with the same source driver, each source driver is installed on the same side of the display panel, and there is an electronic switch installed on the source driver for switching the data transfer.

15 48. The liquid crystal display driving device of matrix structure type as claimed in claim 44, wherein the first data lines of each group of data lines and the second data lines of each group of data lines are connected with the same source driver, each source driver is installed on the same side of the display panel, and there is an electronic switch installed on the source driver for switching the data transfer.

20 49. The liquid crystal display driving device of matrix structure type as claimed in claim 43, wherein there is a space between the neighboring gate lines to prevent them from short circuit.

25 50. The liquid crystal display driving device of matrix structure type as claimed in claim 44, wherein there is a space between the neighboring gate lines to prevent them from short circuit.

30 51. The liquid crystal display driving device of matrix structure type as claimed in claim 43, wherein the gate driver is a chip installed on glass.

52. The liquid crystal display driving device of matrix structure type as claimed in claim 44, wherein the gate driver is a chip installed on glass.

35 53. The liquid crystal display driving device of matrix structure type as claimed in claim 43, wherein the gate driver is an integrated gate driver circuit installed on glass.

54. The liquid crystal display driving device of matrix structure type as claimed in claim 44, wherein the gate driver is an integrated gate driver circuit installed on glass.

5

55. A driving method for the liquid crystal display driving device of matrix structure type including:

10 a. making use of the liquid crystal display driving device as claimed in claim 43 or 44, wherein there are  $m+n$ , i.e.  $N=m+n$ , gate lines in the liquid crystal display, the period of predetermined voltage of the over drive received by the thin film transistors connected with the first gate line is set as a over exciting period, and the period of data voltage of the present frame interval received by the thin film transistors connected with the first gate line is set as a brightness keeping period;

15 b. when the over exciting period begins, the first and the  $(n+1)^{\text{th}}$  gate lines are orderly turned on in a time of one synchronous control signal, the predetermined voltage of over drive for the frame and the data voltage for the preceding frame are given to the thin film transistors connected with the gate lines, and the second and the  $(n+2)^{\text{th}}$  gate lines, the third and the  $(n+3)^{\text{th}}$  gate lines... and the  $(m+n-1)^{\text{th}}$  and the  $m^{\text{th}}$  gate lines are orderly and synchronously turned on in a time of the synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the second to the  $m^{\text{th}}$  gate lines, the data voltage for the preceding frame is given to the thin film transistors connected with the  $(n+2)^{\text{th}}$  to the  $(m+n-1)^{\text{th}}$  gate line;

25

30 c. when the brightness keeping period begins, the first and the  $(m+1)^{\text{th}}$  gate lines are orderly turned on in a time of one synchronous control signal, the data voltage of the frame interval and the predetermined voltage are given to the thin film transistors connected with the gate lines, and the second and the  $(m+2)^{\text{th}}$  gate lines, the third and the  $(m+3)^{\text{th}}$  gate lines... and the  $(m+n)^{\text{th}}$  (i.e. the last) and the  $n^{\text{th}}$  gate lines are orderly and synchronously turned on, the predetermined voltage is given to the thin film transistors connected with the  $(m+2)^{\text{th}}$  to the  $(m+n)^{\text{th}}$  (i.e. the last) gate line, the data voltage of the present frame interval is given to the thin film transistors connected with the second to the  $n^{\text{th}}$  gate line;

35

by using of the steps stated above, the response speed of the liquid crystal display can be increased.

56. The driving method for the liquid crystal display of matrix structure type as claimed in claim 55, wherein the driving method suits for the active matrix type liquid crystal display, the organic light emitting diode (OLED) display or plasma display panel (PDP).

5

LIQUID CRYSTAL DISPLAY DRIVING DEVICE OF MATRIX STRUCTURE  
TYPE AND ITS DRIVING METHOD

ABSTRACT OF THE DISCLOSURE

A liquid crystal display driving device of matrix structure type and its driving  
5 method are disclosed in the present invention. The driving device consists of a group  
of thin film transistors with matrix array, a plurality of gate lines and a plurality of  
data lines. The object of increasing response speed can be accomplished by the  
different arrangement of gate lines and data lines and the different connection between  
each thin film transistor and the gate and data lines. The driving method for the said  
10 driving device includes: each pair of gate lines in the display panel are simultaneously  
and orderly turned on at different time of driving transistor, and the different driving  
voltages are orderly applied to the thin film transistors connected to the gate lines. The  
structure and method can suit for picture treating of various displays such as liquid  
crystal display, organic light-emitting diode (OLED) display or plasma display panel  
15 (PDP).

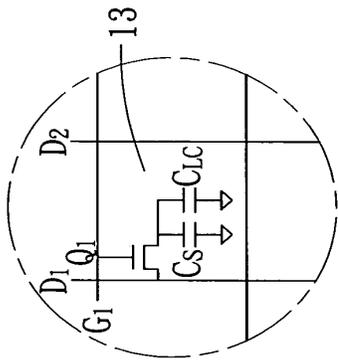


Fig. 1B (Prior Art)

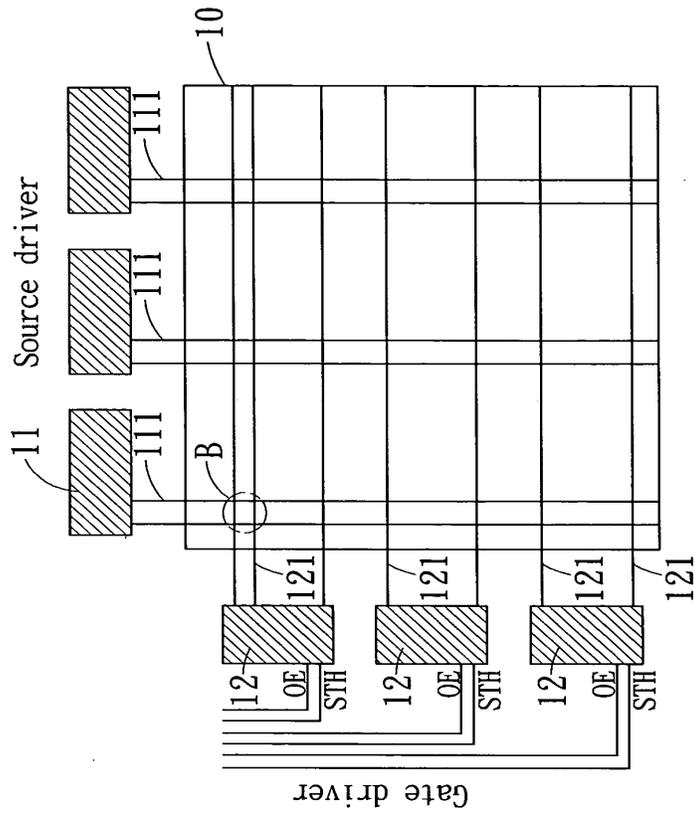


Fig. 1A (Prior Art)

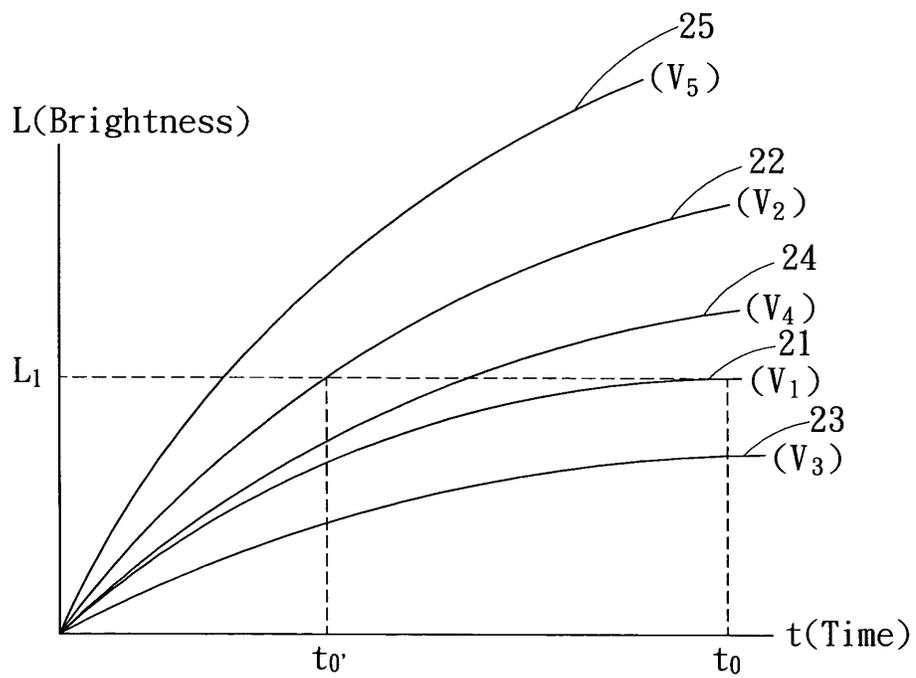


Fig. 2 (Prior Art)

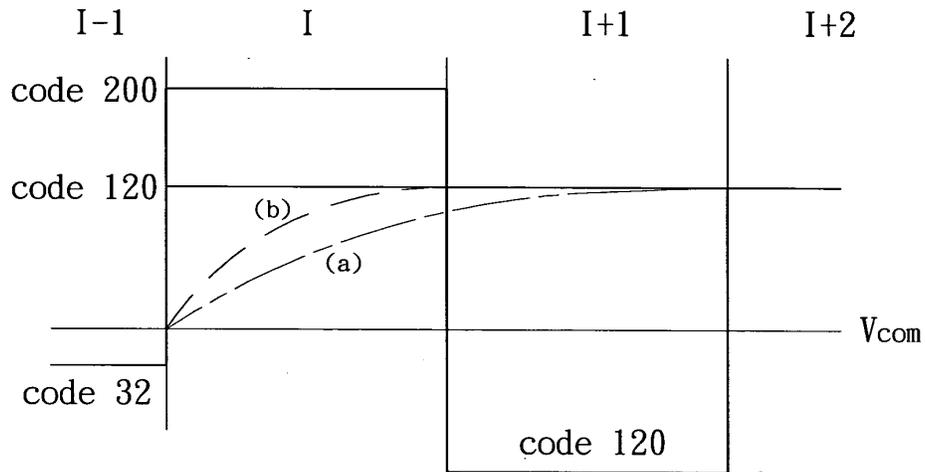


Fig. 3A (Prior Art)

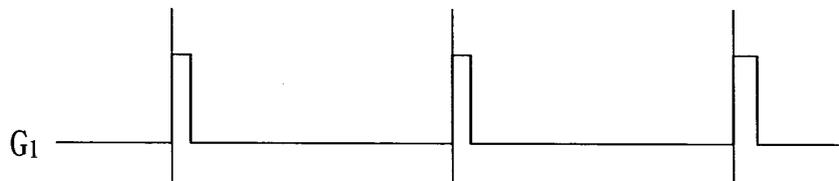


Fig. 3B (Prior Art)

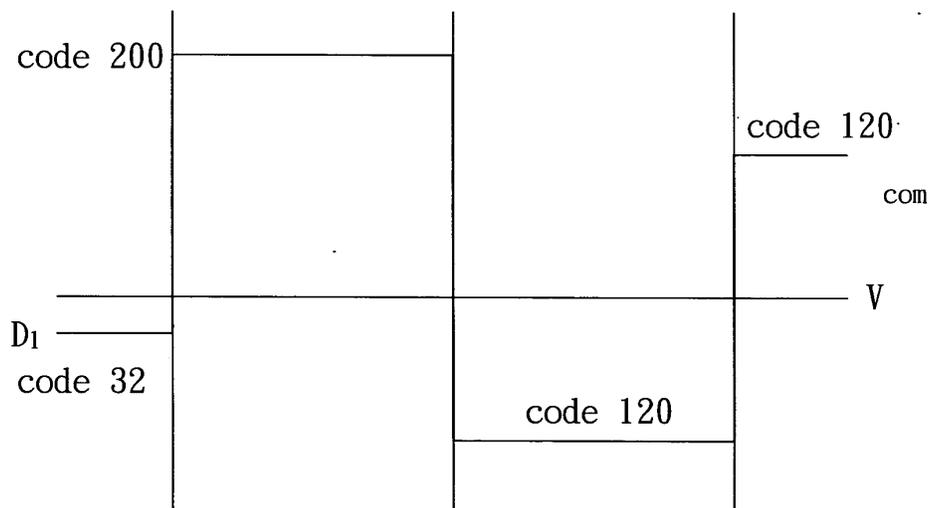


Fig. 3C (Prior Art)

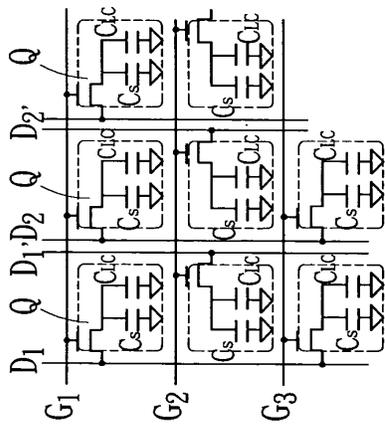


Fig. 4B

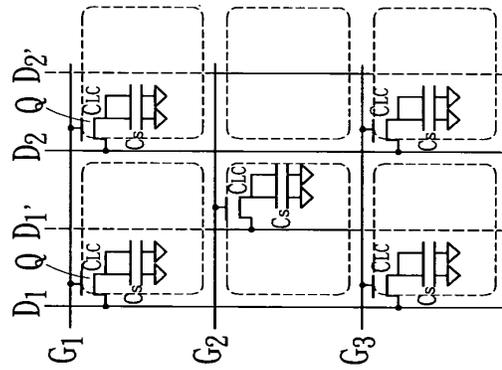


Fig. 4C

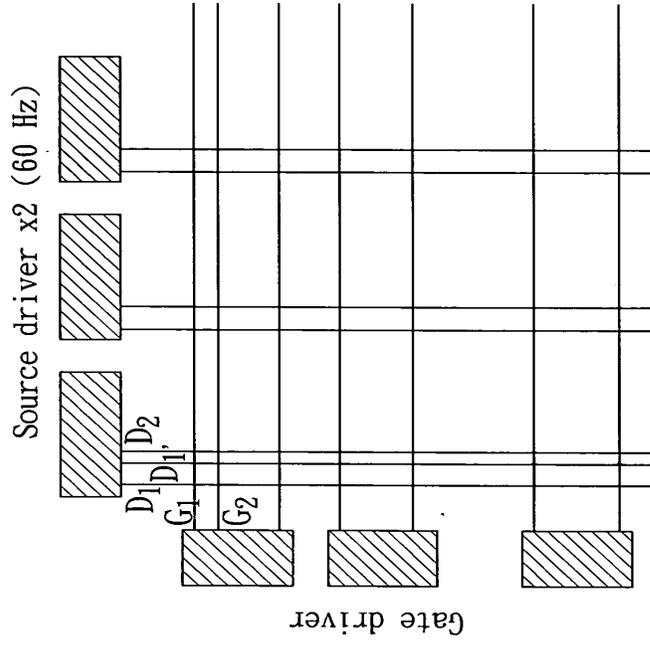


Fig. 4A

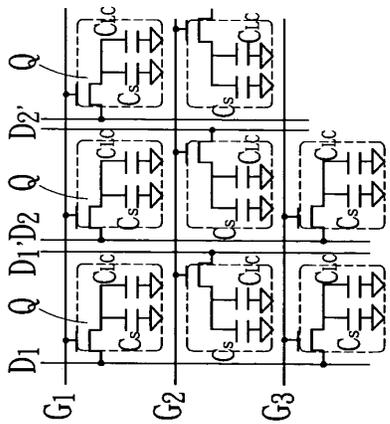


Fig. 5B

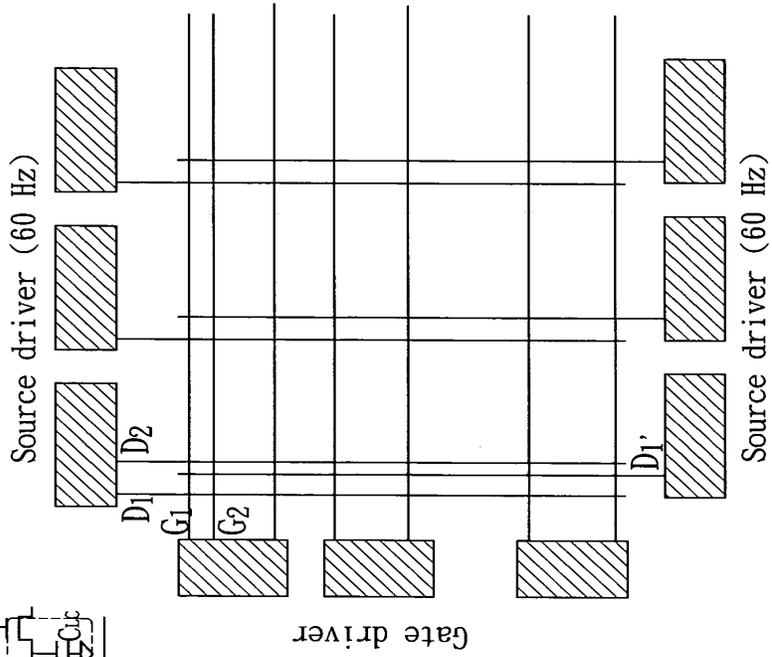


Fig. 5A



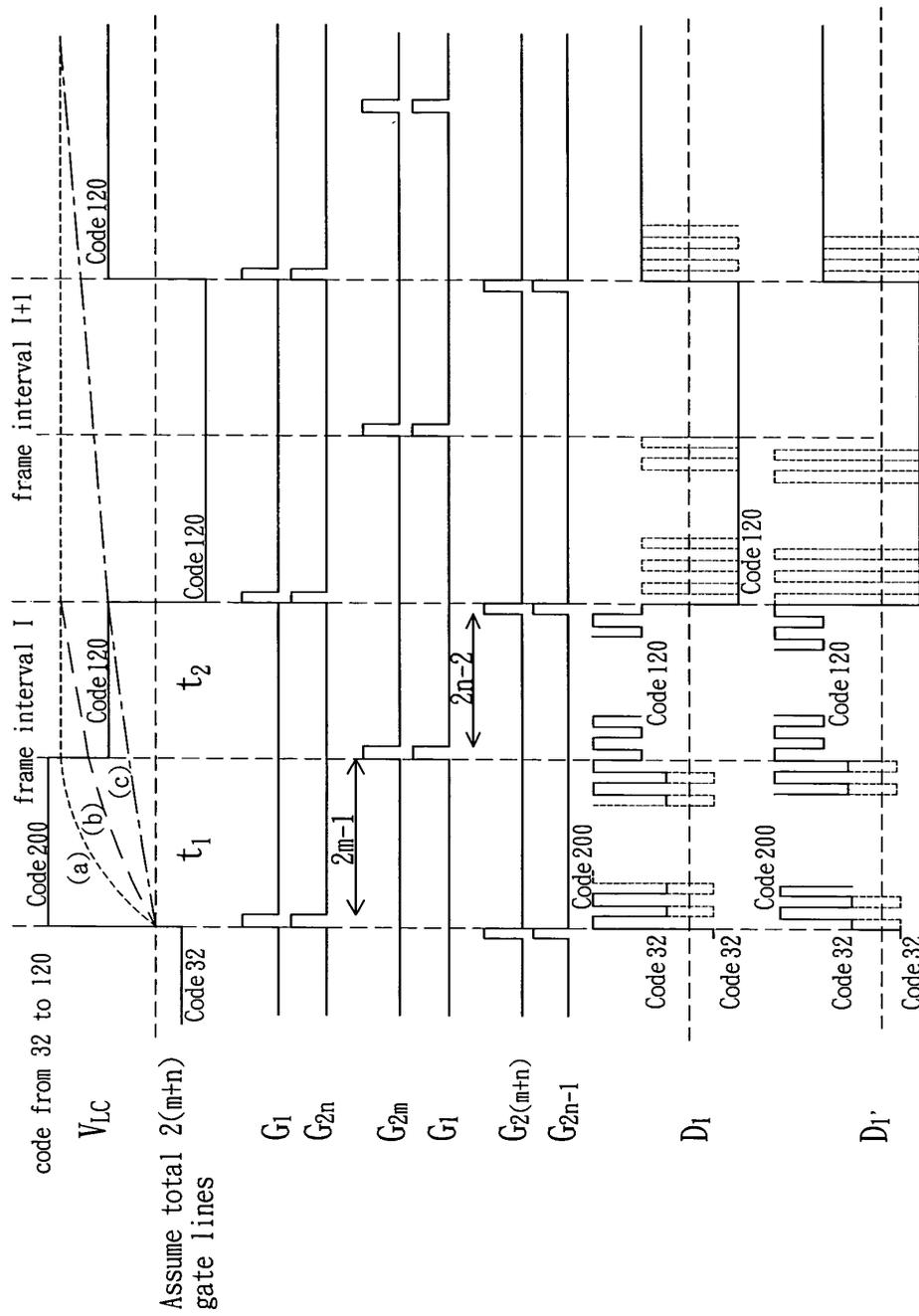


Fig. 7

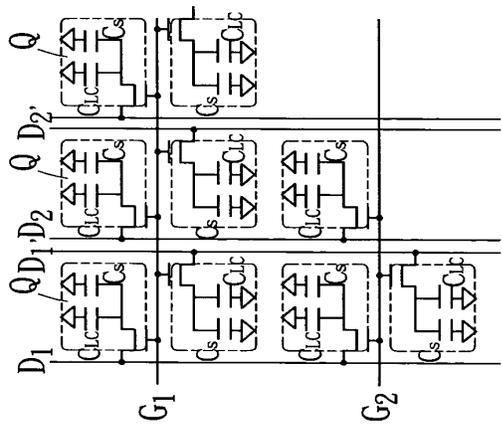


Fig. 8B

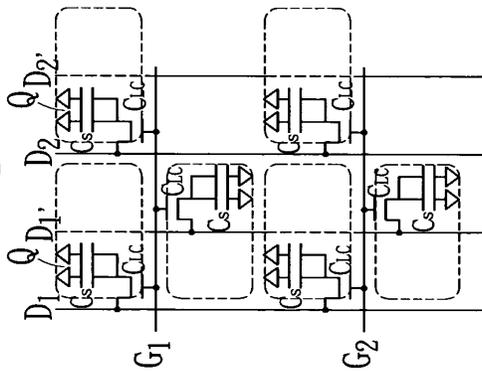


Fig. 8C

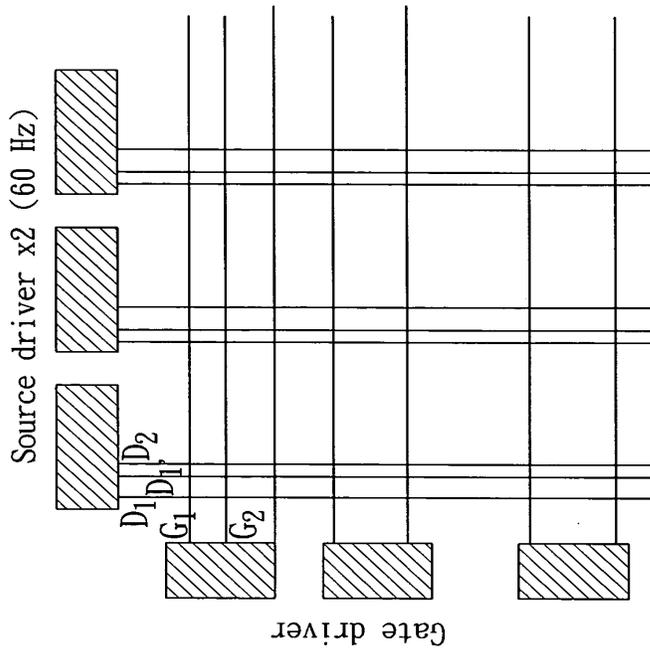


Fig. 8A

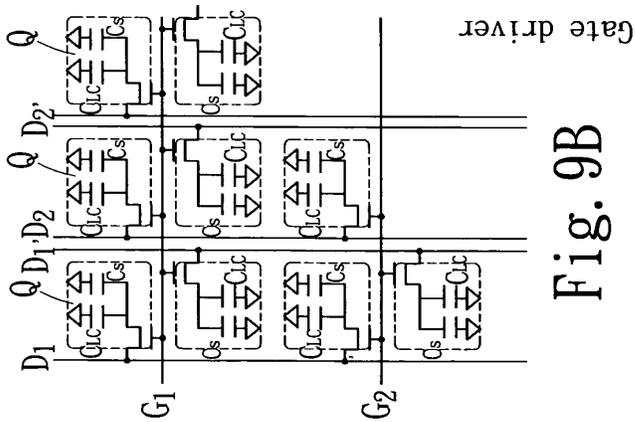


Fig. 9B

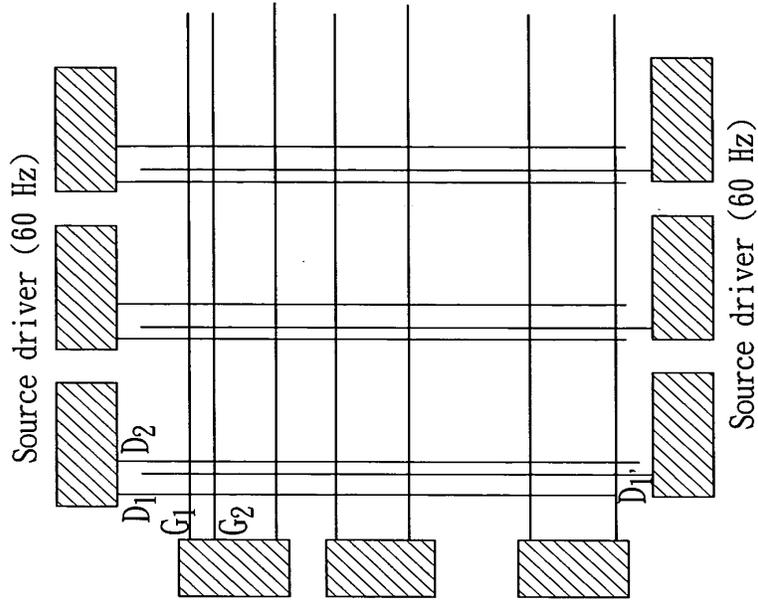


Fig. 9A

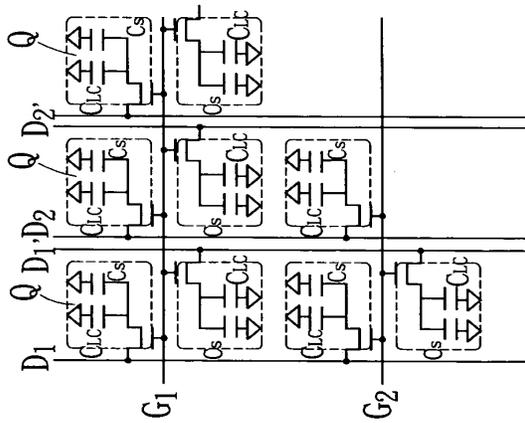


Fig. 10B

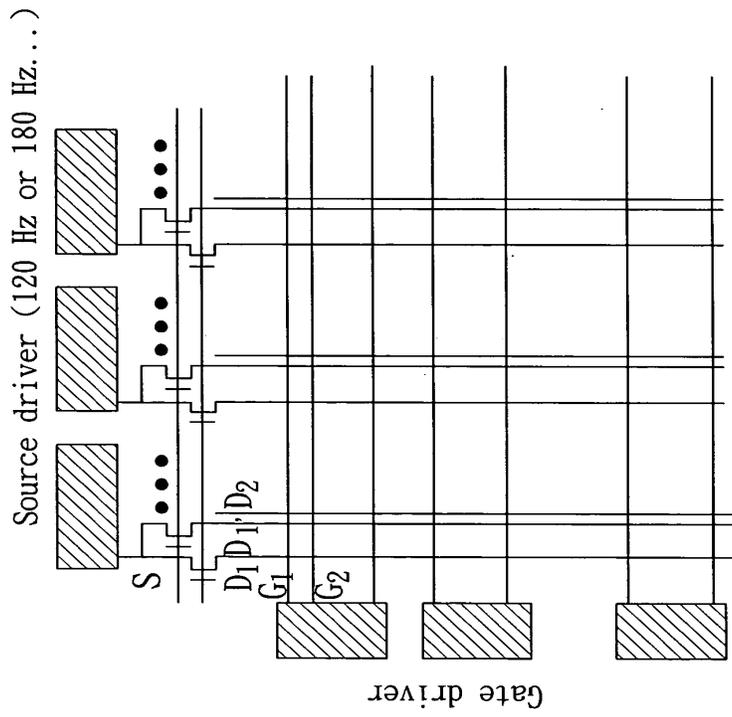


Fig. 10A



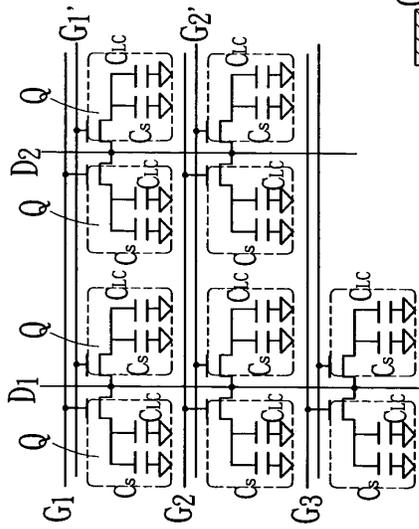


Fig. 12B

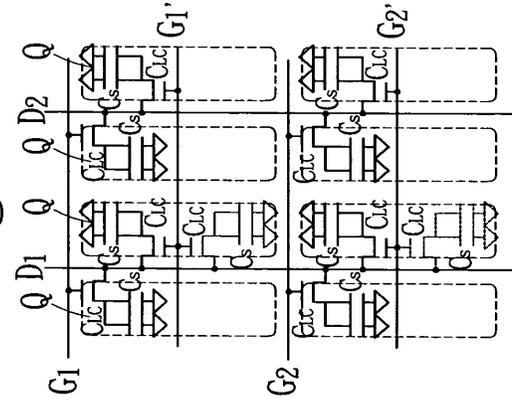


Fig. 12C

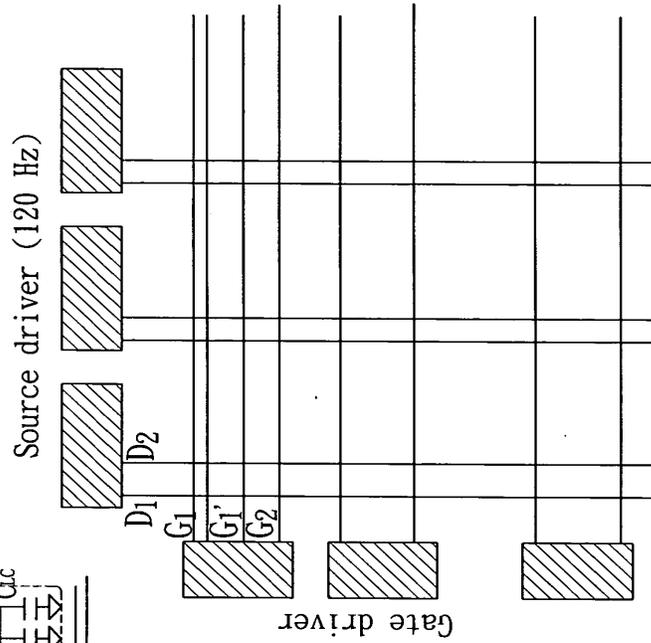


Fig. 12A



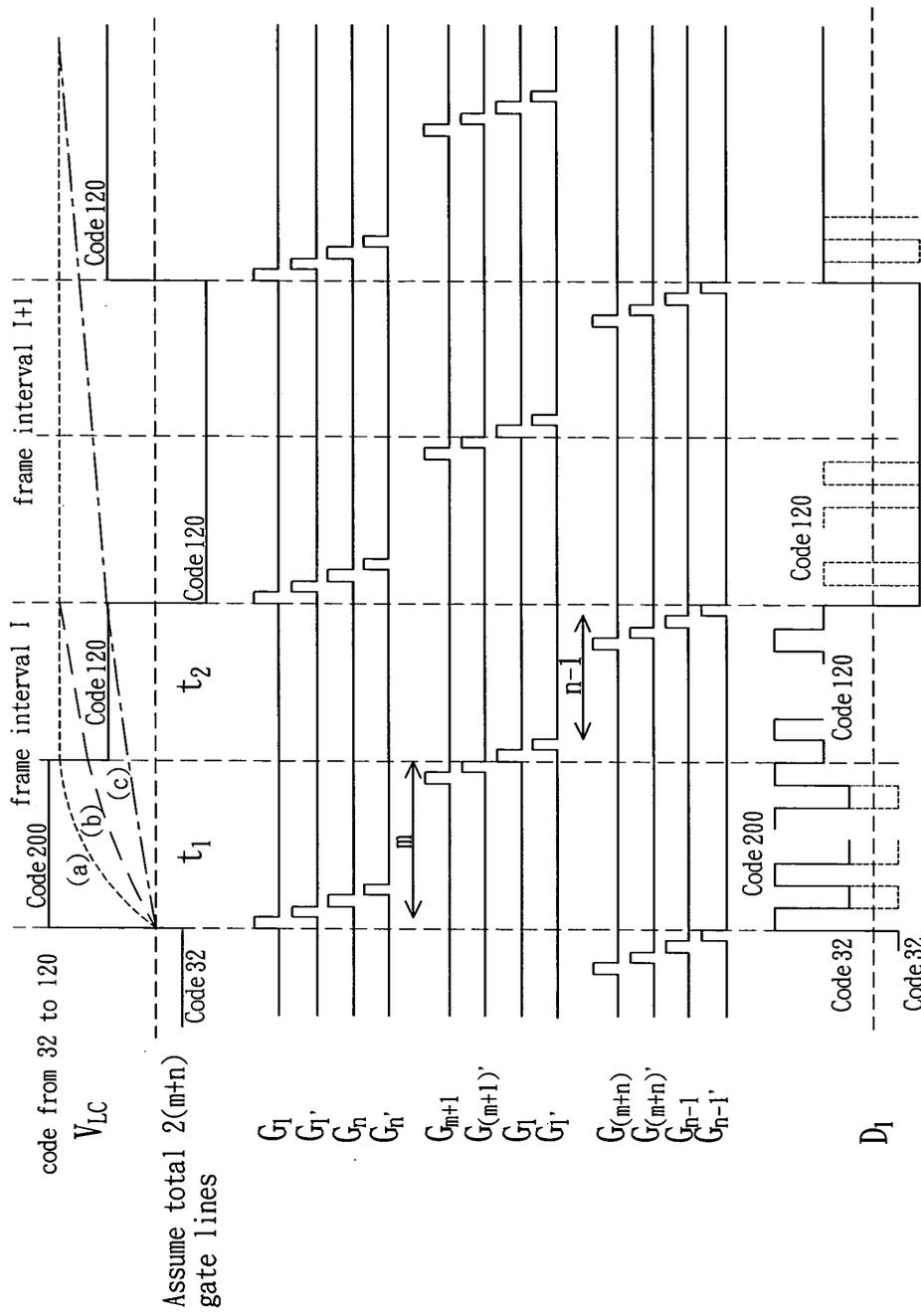


Fig. 14

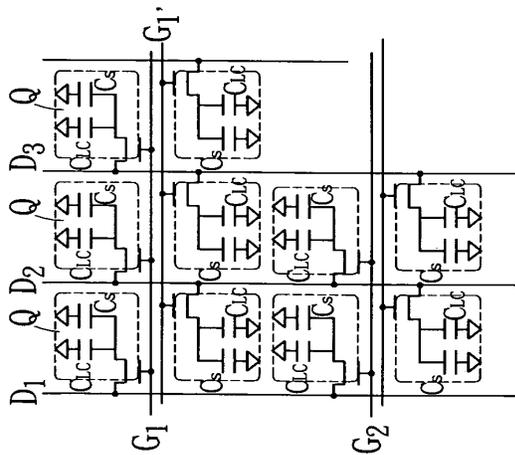


Fig. 15B

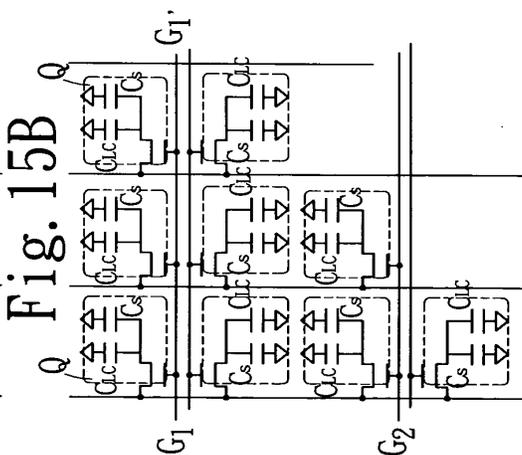


Fig. 15C

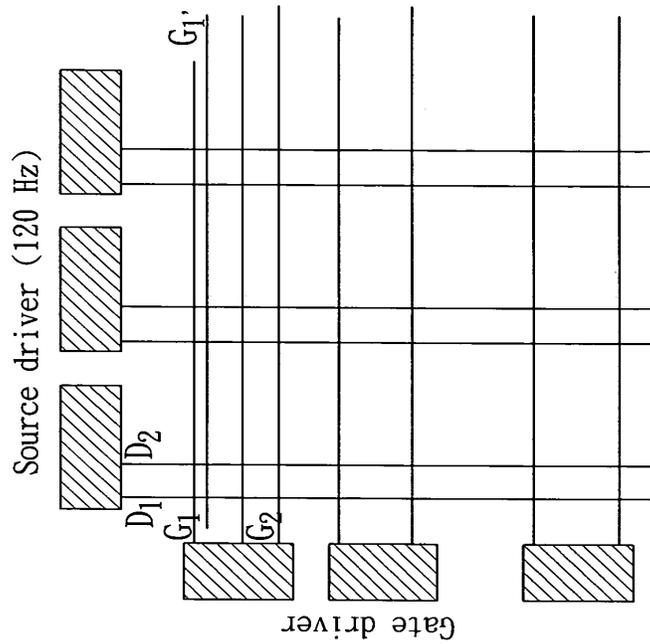


Fig. 15A

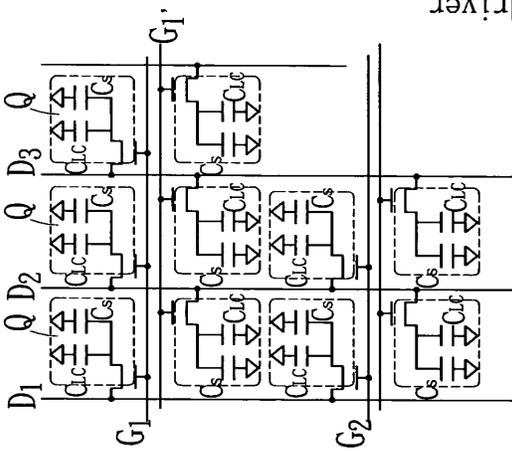


Fig. 16B

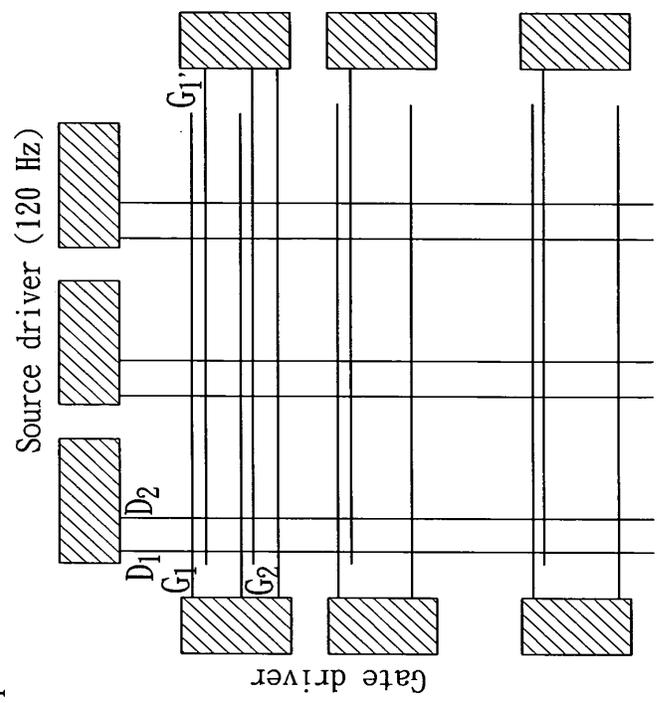


Fig. 16A

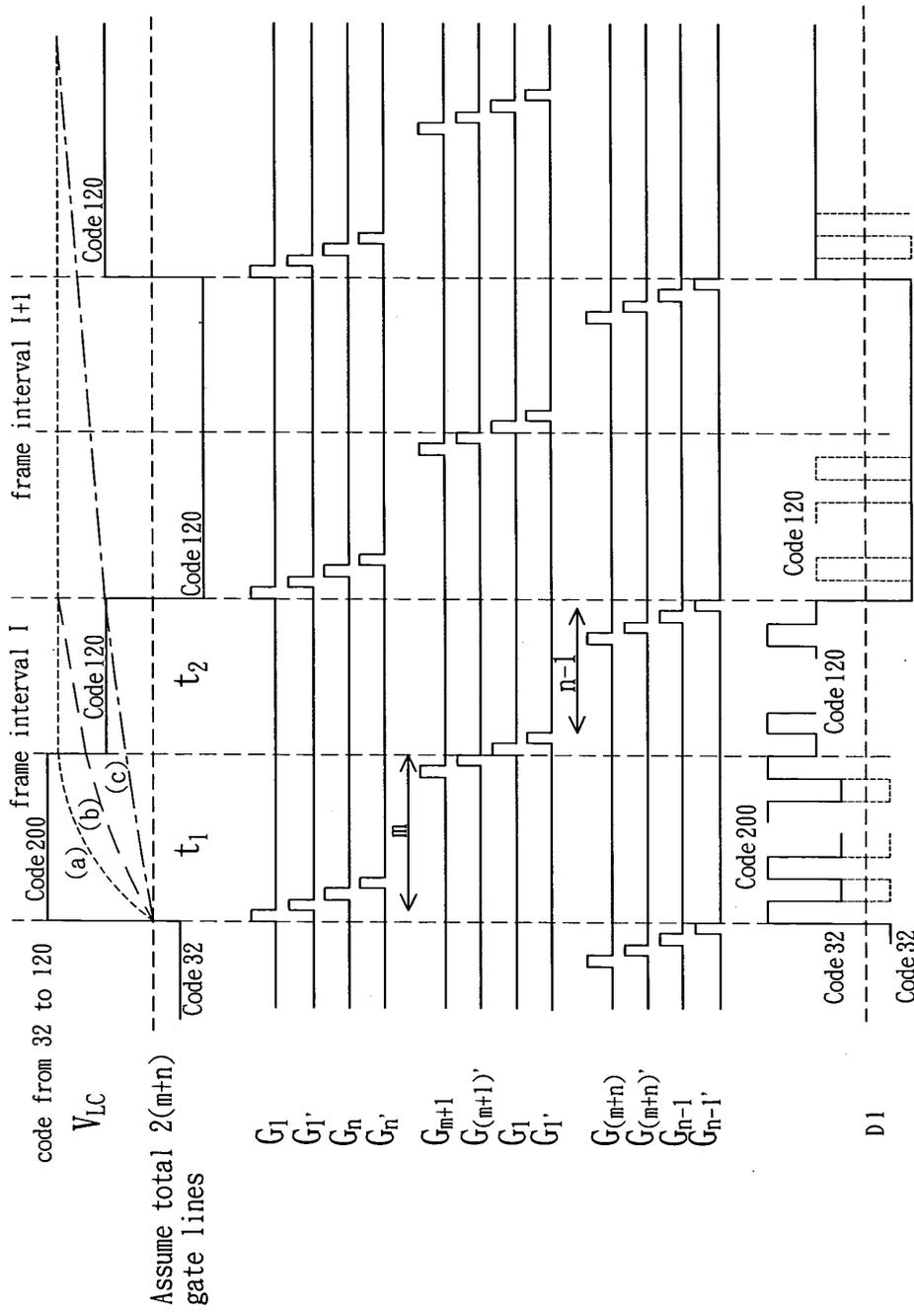


Fig. 17



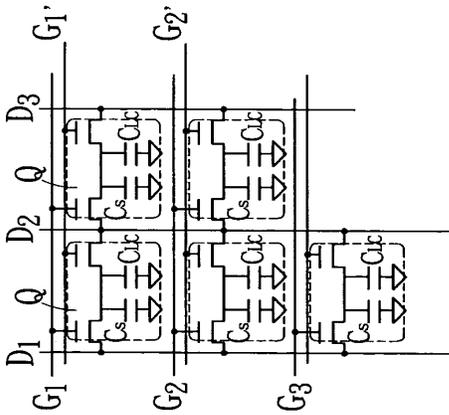


Fig. 19B

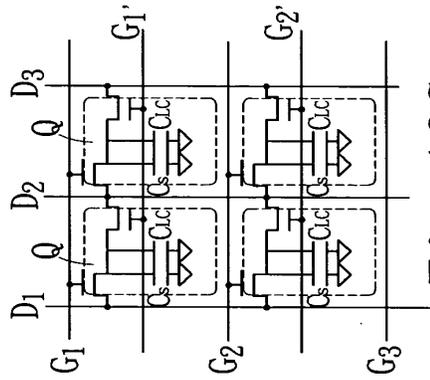


Fig. 19C

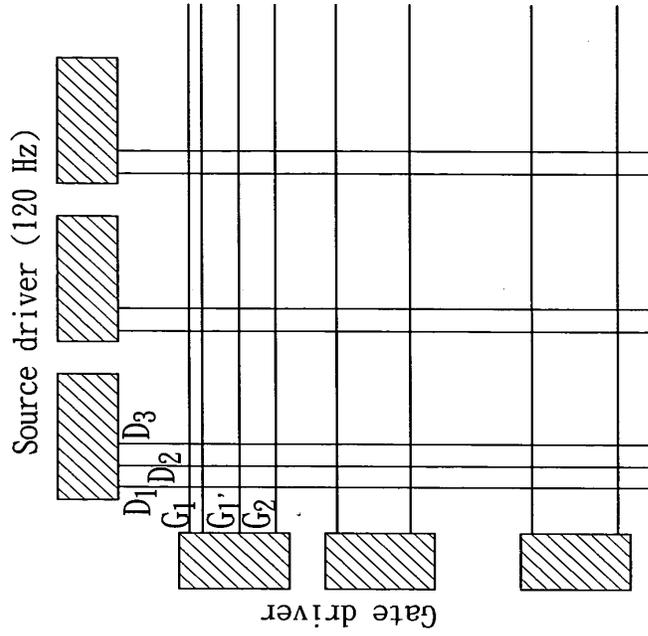


Fig. 19A

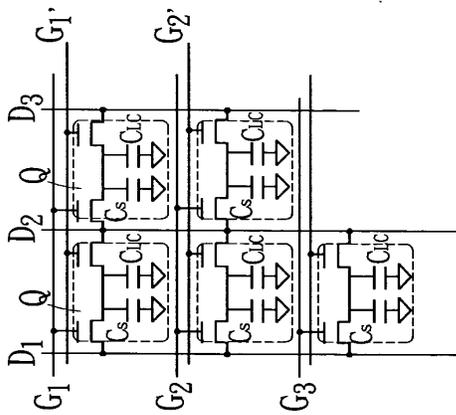


Fig. 20B

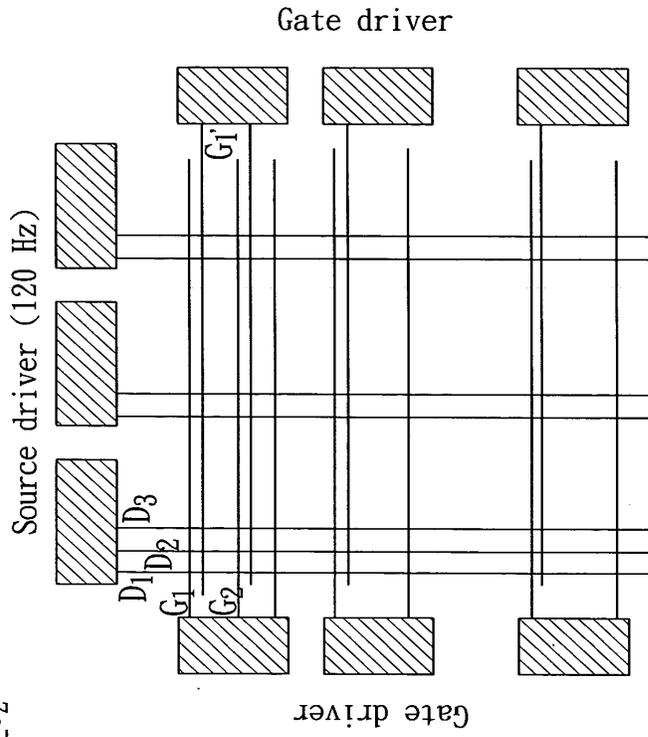


Fig. 20A

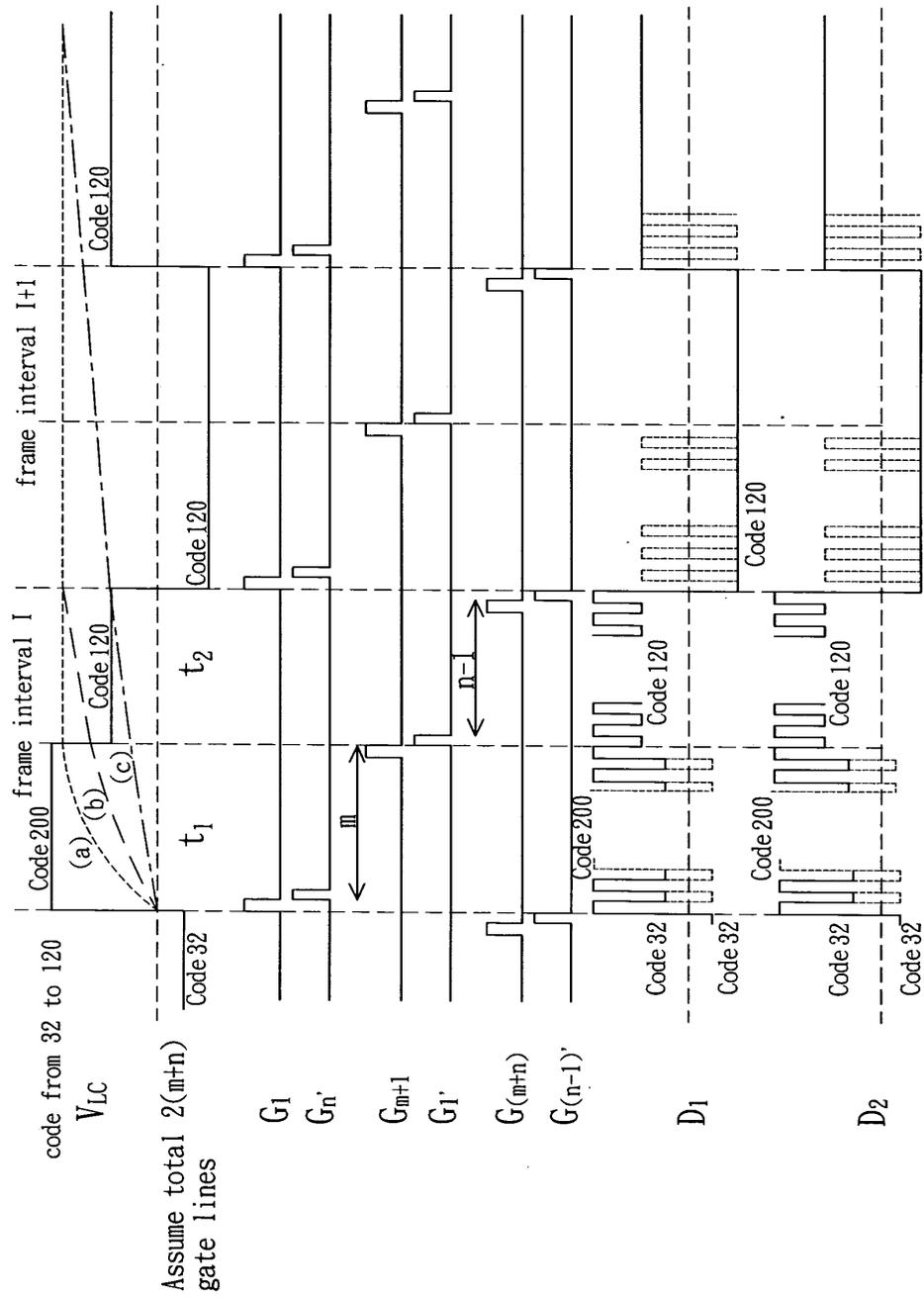


Fig. 21

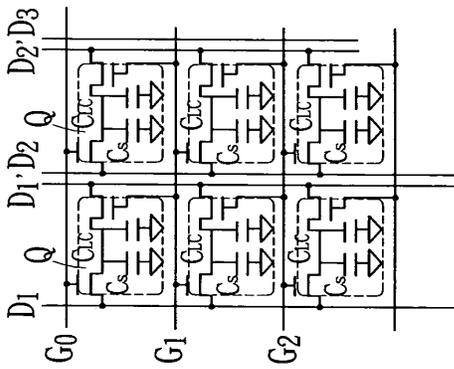


Fig. 22B

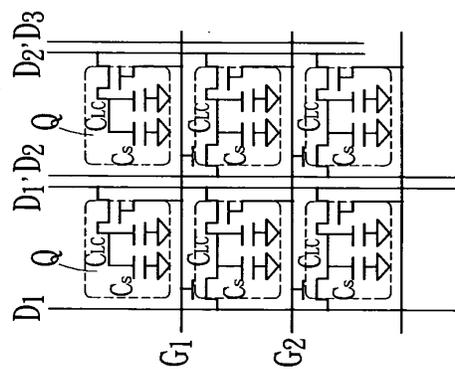


Fig. 22C

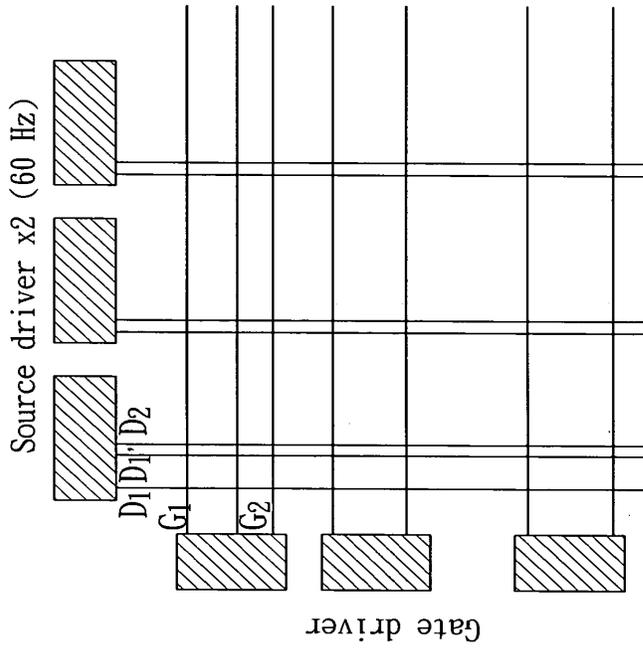


Fig. 22A

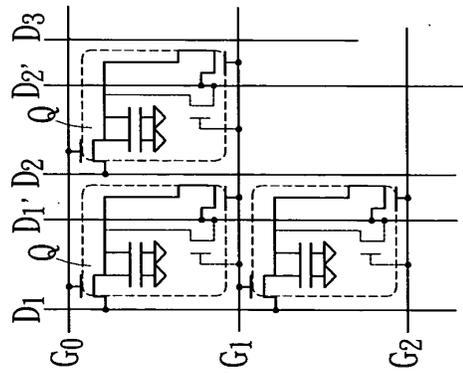


Fig. 22D

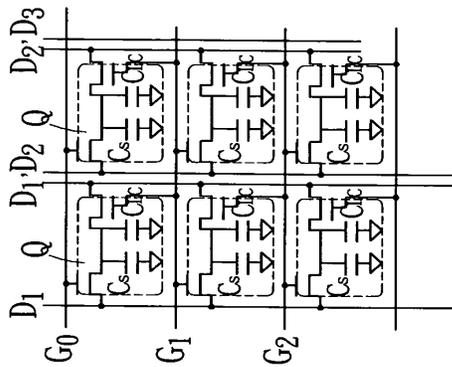


Fig. 23B

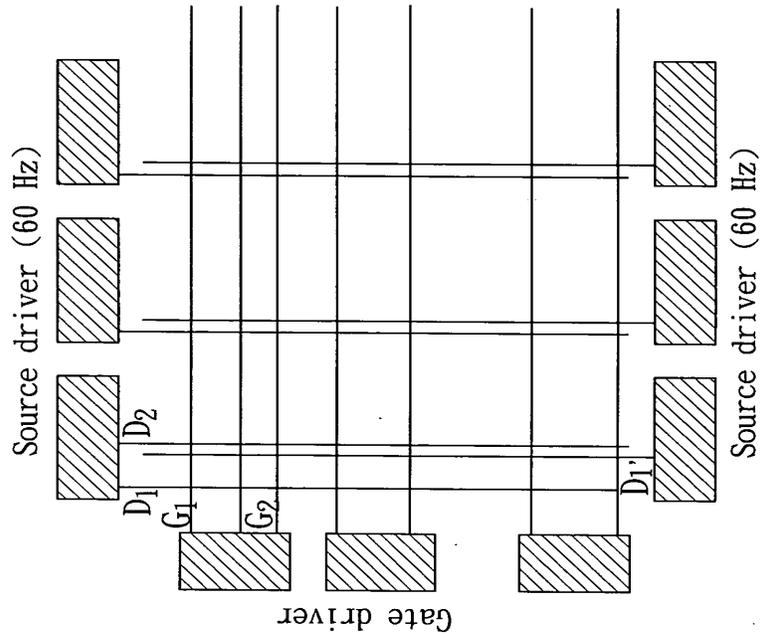


Fig. 23A

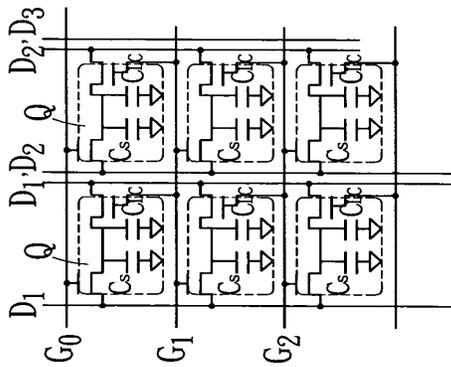


Fig. 24B

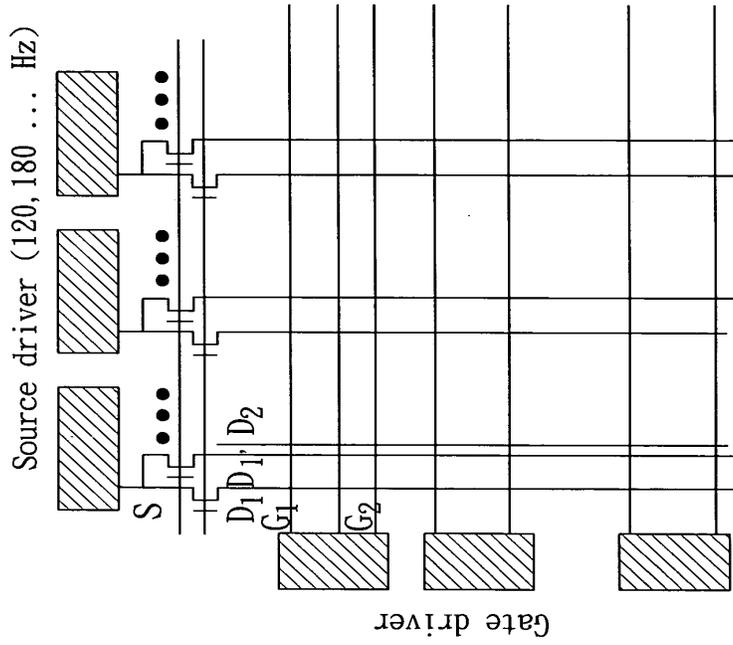


Fig. 24A

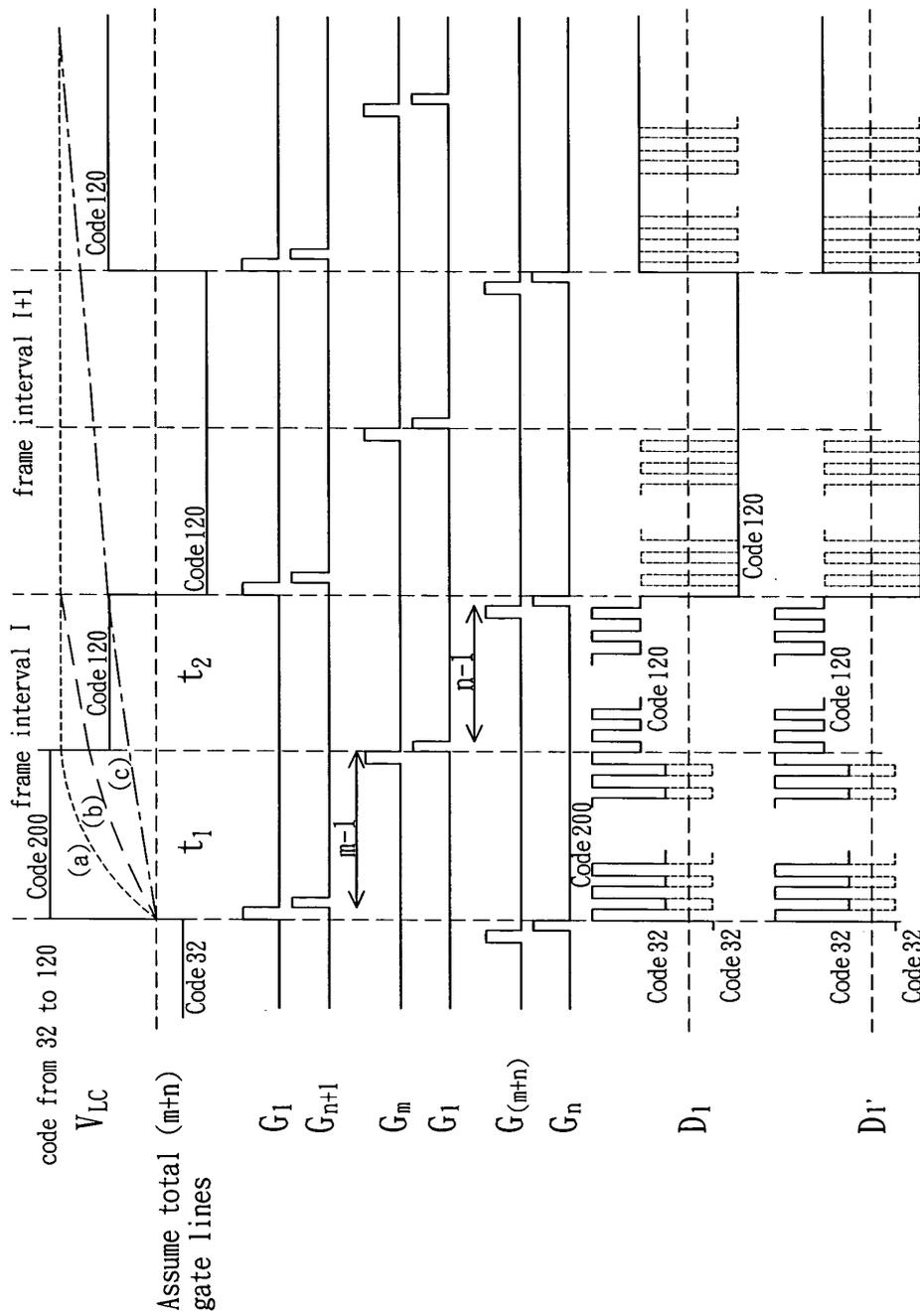


Fig. 25

**DECLARATION FOR PATENT APPLICATION AND APPOINTMENT OF ATTORNEY**

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention (Design, if applicable) entitled:

LIQUID CRYSTAL DISPLAY DRIVING DEVICE OF MATRIX STRUCTURE TYPE AND ITS DRIVING the specification of which (check one):

is attached hereto; or  was filed on: METHOD as U.S. Application Number or PCT International Application

Number: and (if applicable) was amended on:

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56. I hereby claim foreign priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN APPLICATION(S)			PRIORITY CLAIMED	
Number	Country	Day/Month/Year Filed	Yes	No

Additional Priority Application(s) Listed on Following Page(s)

I HEREBY CLAIM THE BENEFIT UNDER TITLE 35 U.S. CODE § 119(E) OF ANY U.S. PROVISIONAL APPLICATIONS LISTED BELOW.	
Application Number	Day/Month/Year Filed

Additional Provisional Application(s) Listed on Following Page(s)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or PCT international application(s) designating The United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Number	Filing Date	Status - Patented, Pending or Abandoned

Additional US/PCT Priority Application(s) listed on Following Page(s)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: I (We) hereby appoint as my (our) attorneys, with full powers of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

**David E. Dougherty, Reg. No. 19,576**

I (we) authorize my (our) attorneys to accept and follow instructions from \_\_\_\_\_ regarding any matter related to the preparation, examination, grant and maintenance of this application, any continuation, continuation-in-part or divisional based thereon, and any patent resulting therefrom, until I (we) or my (our) assigns withdraw this authorization in writing.

SEND CORRESPONDENCE TO: DENNISON, SCHULTZ, DOUGHERTY & MACDONALD  
SUITE 105, 1727 KING STREET  
ALEXANDRIA, VIRGINIA 22314-2700

TELEPHONE CALLS TO: DENNISON, SCHULTZ, DOUGHERTY & MACDONALD  
Tel: 703-837-9600

FULL NAME OF FIRST OR SOLE INVENTOR Shen Yuh-Ren	CITIZENSHIP Taiwan, R.O.C.
RESIDENCE ADDRESS No. 33, Lane 185, Yufong St., Ling 19, Shih Tong Li, East District,	POST OFFICE ADDRESS IS THE SAME AS RESIDENCE ADDRESS UNLESS OTHERWISE SHOWN BELOW same as residence
DATE July 30, 2004	SIGNATURE Yuhren Shen

See following page(s) for additional joint inventors

## CONTINUATION OF DECLARATION FOR PATENT APPLICATION AND APPOINTMENT OF ATTORNEY

Page 2

PRIOR FOREIGN APPLICATION(S)			PRIORITY CLAIMED	
Number	Country	Day/Month/Year Filed	Yes	No

PRIOR PROVISIONAL APPLICATIONS 35 U.S. CODE § 119(E)		
Application Number	Filing Date	Status - Patented, Pending or Abandoned

PRIOR U.S. OR PCT INTERNATIONAL APPLICATIONS (35 U.S. CODE § 120)		
Application Number	Filing Date	Status - Patented, Pending or Abandoned

Full Name of Joint Inventor	Chen Cheng-Jung	Citizenship	Taiwan, R.O.C.
Residence Address	No.2, Sanming St., Ling 13, Chungwai Li, Chunan Town, Miaoli Hsien,	Post Office Address Is the Same as Residence Address Unless Otherwise Shown below	same as residence
Date	July 30, 2004 Taiwan, R.O.C.	Signature	Chen Cheng Jung

Full Name of Joint Inventor	Chen Chun-Chi	Citizenship	Taiwan, R.O.C.
Residence Address	No.90, Houping Rd., Cianjhen District, Kaohsiung City, Taiwan, R.O.C.	Post Office Address Is the Same as Residence Address Unless Otherwise Shown below	same as residence
Date	July 30, 2004	Signature	Chen Chun Chi

Full Name of Joint Inventor		Citizenship	
Residence Address		Post Office Address Is the Same as Residence Address Unless Otherwise Shown below	
Date		Signature	

Full Name of Joint Inventor		Citizenship	
Residence Address		Post Office Address Is the Same as Residence Address Unless Otherwise Shown below	
Date		Signature	

 See following pages for additional joint inventors/priority applications.

PATENT APPLICATION SERIAL NO. \_\_\_\_\_

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE  
FEE RECORD SHEET

09/01/2004 HTECKLU1 00000045 10929473

01 FC:2001	385.00	DP
02 FC:2202	324.00	DP
03 FC:2201	172.00	DP

PTO-1556  
(5/87)

\*U.S. Government Printing Office: 2002 — 489-267/69033

SAMSUNG EX. 1002 - 77/188

**PATENT APPLICATION FEE DETERMINATION RECORD**  
Effective October 1, 2003

Application or Docket Number

10929473

**CLAIMS AS FILED - PART I**

	(Column 1)	(Column 2)
TOTAL CLAIMS	56	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	56 minus 20 =	36
INDEPENDENT CLAIMS	7 minus 3 =	4
MULTIPLE DEPENDENT CLAIM PRESENT <input type="checkbox"/>		

\* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE

OR OTHER THAN SMALL ENTITY

RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
XS 9=	324	OR	XS18=	
X43=	172	OR	X86=	
+145=		OR	+290=	
TOTAL	881	OR	TOTAL	

**CLAIMS AS AMENDED - PART II**

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	Minus **	=
	Independent	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪ ⑫ ⑬ ⑭ ⑮ ⑯ ⑰ ⑱ ⑲ ⑳ ㉑ ㉒ ㉓ ㉔ ㉕ ㉖ ㉗ ㉘ ㉙ ㉚ ㉛ ㉜ ㉝ ㉞ ㉟ ㊱ ㊲ ㊳ ㊴ ㊵ ㊶ ㊷ ㊸ ㊹ ㊺ ㊻ ㊼ ㊽ ㊾ ㊿

SMALL ENTITY OR

OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	Minus **	=
	Independent	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	Minus **	=
	Independent	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

\* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.  
 \*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."  
 \*\*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."  
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Small

**PATENT APPLICATION FEE DETERMINATION RECORD**  
Effective October 1, 2003

Application or Docket Number

10/929473

**CLAIMS AS FILED - PART I**

	(Column 1)	(Column 2)
TOTAL CLAIMS	56	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	62 minus 20=	* 42
INDEPENDENT CLAIMS	7 minus 3 =	* 4
MULTIPLE DEPENDENT CLAIM PRESENT <input checked="" type="checkbox"/>		

\* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE  OR

OTHER THAN SMALL ENTITY

RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
XS 9=	378	OR	XS18=	
X43=	172	OR	X86=	
+145=	145	OR	+290=	
TOTAL	1080	OR	TOTAL	

**CLAIMS AS AMENDED - PART II**

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	* Minus **	=
	Independent	* Minus ***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>		

SMALL ENTITY OR

OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

**BEST AVAILABLE COPY**

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	* Minus **	=
	Independent	* Minus ***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>		

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	* Minus **	=
	Independent	* Minus ***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>		

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

\* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.  
 \*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."  
 \*\*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."  
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

PATENT APPLICATION SERIAL NO. \_\_\_\_\_

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE  
FEE RECORD SHEET

09/01/2004 HTECKLU1 00000045 10929473

01 FC:2001	385.00	OP
02 FC:2202	324.00	OP
03 FC:2201	172.00	OP

10/29/2004 HMDHAMM1 00000014 040753 10929473

01 FC:2203	145.00	DA
02 FC:2202	45.00	DA

PTO-1556  
(5/87)

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\*U.S. Government Printing Office: 2002 — 489-287/88033

10 929473

**Deposit Account Maintenance**

Deposit Account Window Help

**Deposit Account**

Number: 040753 Balance Amount: 454

**Holder**

Name: DENNISON.SCHULTZ, DOUGHERTY & MACDONALD

**Address**

Attention: [ ]

Street: SUITE 105  
1727 KING STREET

Province: [ ]

City: ALEXANDRIA

State: VA Postal Code: 22314

Country: US

Telephone: 703-837-9600 Fax: 703-837-0980

**Details**

Category Code: NONGOVNMNT Type: REGULAR

Notification Amt: 0.00 Status:  Active  Closed

Access Code: 4040

HMOHAMM1 | 10/29/2004

10929473


**UNITED STATES PATENT AND TRADEMARK OFFICE**

 UNITED STATES DEPARTMENT OF COMMERCE  
 United States Patent and Trademark Office  
 Address: COMMISSIONER FOR PATENTS  
 P.O. Box 1450  
 Alexandria, Virginia 22313-1450  
 www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/929,473	08/31/2004	Yuh-Ren Shen	3079/255

 DENNISON, SCHULTZ, DOUGHERTY & MACDONALD  
 SUITE 105  
 1727 KING STREET  
 ALEXANDRIA, VA 22314-2700

**CONFIRMATION NO. 6164**
**FORMALITIES LETTER**


\*OC000000014256515\*

Date Mailed: 11/01/2004

**NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION**
**FILED UNDER 37 CFR 1.53(b)**
***Filing Date Granted***
**Items Required To Avoid Abandonment:**

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given TWO MONTHS from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- Additional claim fees of \$9 as a small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

**SUMMARY OF FEES DUE:**

Total additional fee(s) required for this application is \$9 for a Small Entity

- Total additional claim fee(s) for this application is \$9
  - \$9 for 42 total claims over 20.

 Replies should be mailed to: Mail Stop Missing Parts  
 Commissioner for Patents  
 P.O. Box 1450  
 Alexandria VA 22313-1450

*A copy of this notice **MUST** be returned with the reply.*

*M. Duong*

---

Customer Service Center  
Initial Patent Examination Division (703) 308-1202

PART 3 - OFFICE COPY



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
 United States Patent and Trademark Office  
 Address: COMMISSIONER FOR PATENTS  
 P.O. Box 1450  
 Alexandria, Virginia 22313-1450  
 www.uspto.gov

*IPM*

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/929,473	08/31/2004	Yuh-Ren Shen	3079/255

DENNISON, SCHULTZ, DOUGHERTY & MACDONALD  
 SUITE 105  
 1727 KING STREET  
 ALEXANDRIA, VA 22314-2700



CONFIRMATION NO. 6164  
 FORMALITIES LETTER



\*OC000000014256515\*

Date Mailed: 11/01/2004

**NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION**

FILED UNDER 37 CFR 1.53(b)

*Filing Date Granted*

**Items Required To Avoid Abandonment:**

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given TWO MONTHS from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- Additional claim fees of \$9 as a small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

**SUMMARY OF FEES DUE:**

Total additional fee(s) required for this application is \$9 for a Small Entity

- Total additional claim fee(s) for this application is \$9
  - \$9 for 42 total claims over 20.

Replies should be mailed to: Mail Stop Missing Parts  
 Commissioner for Patents  
 P.O. Box 1450  
 Alexandria VA 22313-1450

*A copy of this notice **MUST** be returned with the reply.*

12/30/2004 NNGUYEN1 00000028 040753 10929473

01 FC:2202 16.00 DA 9.00 OP

*MDWong*

---

Customer Service Center  
Initial Patent Examination Division (703) 308-1202

PART 2 - COPY TO BE RETURNED WITH RESPONSE



Attorney Docket No. 3079/255

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :
Yuh-Ren SHEN et al. : Group Art Unit: 2871
Serial No: 10/929,473 : Examiner: To Be Assigned
Filed: August 31, 2004 :

For: LIQUID CRYSTAL DISPLAY DRIVING DEVICE OF
MATRIX STRUCTURE TYPE AND ITS DRIVING METHOD

RESPONSE TO NOTICE TO FILE MISSING PARTS
OF NONPROVISIONAL APPLICATION

Commissioner For Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice to File Missing Parts of Nonprovisional Application dated
November 1, 2004 (a copy of which is hereby attached), Applicants submit the additional claim
fee of \$9.00 as requested.

Please charge the \$9.00 claim fee to the credit card identified on the credit card
authorization form submitted herewith. If for any reason charges to this credit card are denied,
you are hereby authorized to charge the \$9.00, and any additional claim charge fees to
Deposit Account No. 04-0753.

Respectfully submitted,

December 29, 2004
Date

By: [Signature]
Ira J. Schultz
Reg. No. 28,666

Dennison, Schultz, Dougherty & MacDonald
1727 King Street , Suite 105
Alexandria, VA 22314-2700
Tel: (703) 837-9700
Fax: (703) 837-0980

182

Attorney Docket No. 3079/255



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Yuh-Ren SHEN et al.

:  
:  
: Group Art Unit: 2871

Serial No: 10/929,473

:  
: Examiner: unassigned

Filed: August 31, 2004

:  
:

For: **LIQUID CRYSTAL DISPLAY DRIVING DEVICE OF MATRIX  
STRUCTURE TYPE AND ITS DRIVING METHOD**

PRELIMINARY AMENDMENT

Commissioner For Patents and Trademarks  
Alexandria, VA 22313-11450

Sir:

Prior to initial examination, please amend the above-identified application as follows:

LAW OFFICES  
DENNISON, SCHULTZ, DOUGHERTY & MACDONALD  
SUITE 105  
1727 KING STREET  
ALEXANDRIA, VIRGINIA 22314-2700  
703 837-9600

**IN THE CLAIMS:**

Please amend claim 55 as follows:

55. (Currently Amended) A driving method for the liquid crystal display driving device of matrix structure type including:

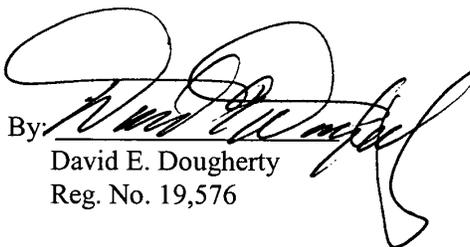
- a. making use of the liquid crystal display driving device as claimed in claim 43 ~~or 44~~, wherein there are  $m+n$ , i.e.  $N=m+n$ , gate lines in the liquid crystal display, the period of predetermined voltage of the over drive received by the thin film transistors connected with the first gate line is set as a over exciting period, and the period of data voltage of the present frame interval received by the thin film transistors connected with the first gate line is set as a brightness keeping period;
  - b. when the over exciting period begins, the first and the  $(n+1)^{\text{th}}$  gate lines are orderly turned on in a time of one synchronous control signal, the predetermined voltage of over drive for the frame and the data voltage for the preceding frame are given to the thin film transistors connected with the gate lines, and the second and the  $(n+2)^{\text{th}}$  gate lines, the third and the  $(n+3)^{\text{th}}$  gate lines... and the  $(m+n-1)^{\text{th}}$  and the  $m^{\text{th}}$  gate lines are orderly and synchronously turned on in a time of the synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the second to the  $m^{\text{th}}$  gate lines, the data voltage for the preceding frame is given to the thin transistors connected with the  $(n+2)^{\text{th}}$  to the  $(m+n-1)^{\text{th}}$  gate line;
  - c. when the brightness keeping period begins, the first and the  $(m+1)^{\text{th}}$  gate lines are orderly turned on in a time of one synchronous control signal the data voltage of the frame interval and the predetermined voltage are given to the thin film transistors connected with the gate lines, and the second and the  $(m+2)^{\text{th}}$  gate lines, the third and the  $(m+3)^{\text{th}}$  gate lines... and the  $(m+n)^{\text{th}}$  (i.e. the last) and the  $n^{\text{th}}$  gate lines are orderly and synchronously turned on, the predetermined voltage is given to the thin film transistors connected with the  $(m+2)^{\text{th}}$  to the  $(m+n)^{\text{th}}$  (i.e. the last) gate line, the data voltage of the present frame interval is given to the thin film transistors connected with the second to the  $n^{\text{th}}$  gate line;
- by using of the steps stated above, the response speed of the liquid crystal display can be increased.

**REMARKS**

By this Preliminary Amendment, Applicant has amended claim 55 in order to eliminate multiple dependencies.

Prompt favorable action is requested.

Respectfully submitted,

By:   
David E. Dougherty  
Reg. No. 19,576

February 7, 2005

Date

LAW OFFICES  
DENNISON, SCHULTZ, DOUGHERTY & MACDONALD  
SUITE 105  
1727 KING STREET  
ALEXANDRIA, VIRGINIA 22314-2700  
703 897-9600

**PATENT APPLICATION FEE DETERMINATION RECORD**  
Effective October 1, 2003

Application or Docket Number

10/929473

**CLAIMS AS FILED - PART I**

(Column 1) (Column 2)

TOTAL CLAIMS	56	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	62 minus 20 =	42
INDEPENDENT CLAIMS	7 minus 3 =	4
MULTIPLE DEPENDENT CLAIM PRESENT <input checked="" type="checkbox"/>		

\* If the difference in column 1 is less than zero, enter "0" in column 2

*2/7/03'* **CLAIMS AS AMENDED - PART II**

(Column 1) (Column 2) (Column 3)

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	62	Minus 62	=
	Independent	7	Minus 7	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

**BEST AVAILABLE COPY**

(Column 1) (Column 2) (Column 3)

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total		Minus	=
	Independent		Minus	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

(Column 1) (Column 2) (Column 3)

AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total		Minus	=
	Independent		Minus	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

\* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.  
 \*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."  
 \*\*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."  
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SMALL ENTITY TYPE  OR

OTHER THAN SMALL ENTITY

RATE	FEE
BASIC FEE	385.00
XS 9=	378
X43=	172
+145=	145
TOTAL	1080

RATE	FEE
BASIC FEE	770.00
XS18=	
X86=	
+290=	
TOTAL	

SMALL ENTITY OR

OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL	
ADDITIONAL FEE	

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL	
ADDITIONAL FEE	

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL	
ADDITIONAL FEE	

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL	
ADDITIONAL FEE	

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL	
ADDITIONAL FEE	

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL	
ADDITIONAL FEE	



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
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Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/929,473	08/31/2004	Yuh-Ren Shen	3079/255	6164
7590	02/18/2005		EXAMINER	
DENNISON, SCHULTZ, DOUGHERTY & MACDONALD SUITE 105 1727 KING STREET ALEXANDRIA, VA 22314-2700			ART UNIT	PAPER NUMBER
			2871	

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.



10/929473

COMMISSIONER FOR PATENTS  
UNITED STATES PATENT AND TRADEMARK OFFICE  
P.O. Box 1450  
ALEXANDRIA, VA 22313-1450  
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Notice of Non-Compliant Amendment (37 CFR 1.121)

The amendment document filed on 2/7/09 is considered non-compliant because it has failed to meet the requirements of 37 CFR 1.121. In order for the amendment document to be compliant, correction of the following item(s) is required. **Only the corrected section of the non-compliant amendment document must be resubmitted (in its entirety), e.g., the entire "Amendments to the claims" section of applicant's amendment document must be re-submitted.** 37 CFR 1.121(h).

THE FOLLOWING CHECKED (X) ITEM(S) CAUSE THE AMENDMENT DOCUMENT TO BE NON-COMPLIANT:

- 1. Amendments to the specification:
  - A. Amended paragraph(s) do not include markings.
  - B. New paragraph(s) should not be underlined.
  - C. Other \_\_\_\_\_
- 2. Abstract:
  - A. Not presented on a separate sheet. 37 CFR 1.72.
  - B. Other \_\_\_\_\_
- 3. Amendments to the drawings: \_\_\_\_\_
- 4. Amendments to the claims:
  - A. A complete listing of all of the claims is not present.
  - B. The listing of claims does not include the text of all pending claims (including withdrawn claims)
  - C. Each claim has not been provided with the proper status identifier, and as such, the individual status of each claim cannot be identified. Note: the status of every claim must be indicated after its claim number by using one of the following 7 status identifiers: (Original), (Currently amended), (Canceled), (Withdrawn), (Previously presented), (New) and (Not entered).
  - D. The claims of this amendment paper have not been presented in ascending numerical order.
  - E. Other: \_\_\_\_\_

For further explanation of the amendment format required by 37 CFR 1.121, see MPEP Sec. 714 and the USPTO website at <http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/officeflyer.pdf>.

If the non-compliant amendment is a **PRELIMINARY AMENDMENT**, applicant is given ONE MONTH from the mail date of this letter to supply the corrected section which complies with 37 CFR 1.121. Failure to comply with 37 CFR 1.121 will result in non-entry of the preliminary amendment and examination on the merits will commence without consideration of the proposed changes in the preliminary amendment(s). This notice is not an action under 35 U.S.C. 132, and **this ONE MONTH time limit is not extendable.**

If the non-compliant amendment is a reply to a **NON-FINAL OFFICE ACTION (including a submission for an RCE)**, and since the amendment appears to be a *bona fide* attempt to be a reply (37 CFR 1.135(c)), applicant is given a TIME PERIOD of ONE MONTH from the mailing of this notice within which to re-submit the corrected section which complies with 37 CFR 1.121 in order to avoid abandonment. **EXTENSIONS OF THIS TIME PERIOD ARE AVAILABLE UNDER 37 CFR 1.136(a).**

If the amendment is a reply to a **FINAL REJECTION**, this form may be an attachment to an Advisory Action. The period for response to a final rejection continues to run from the date set in the final rejection, and is not affected by the non-compliant status of the amendment.

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Attorney Docket No. 3079/255

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :  
 :  
**Yuh-Ren SHEN et al.** : Group Art Unit: 2871  
 :  
 Serial No: 10/929,473 : Examiner: **unassigned**  
 :  
 Filed: **August 31, 2004** :  
 :  
 For: **LIQUID CRYSTAL DISPLAY DRIVING DEVICE OF MATRIX  
 STRUCTURE TYPE AND ITS DRIVING METHOD**

RESPONSE TO NOTICE OF NON-COMPLIANT AMENDMENT

Commissioner For Patents and Trademarks  
Alexandria, VA 22313-11450

Sir:

In response to the Notice of Non-Complaint Amendment dated February 18, 2005,  
please amend the claims as follows prior to initial examination.

**IN THE CLAIMS:**

Please amend claim 55 as follows:

1. (Original) A liquid crystal display driving device of matrix structure type including: a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N x M of pixels can be driven;

a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row. . . and the N<sup>th</sup> gate line is connected with the gates of all the thin film transistors of the N<sup>th</sup> row; and

M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second data lines of the first group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column. . . and the first and the second data lines of the M<sup>th</sup> group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M<sup>th</sup> column.

2. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 1, wherein the first and the second data lines of each group of data lines are given data by two groups of source drivers, respectively, and the two groups of source drivers are respectively arranged on the upper and the lower sides of the liquid crystal display.

3. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 1, wherein the first data lines and the second data lines of each group of data lines

are connected with the same source driver, each source driver is installed on the same side of the display panel and the data transfer is switched by an electronic switch.

4. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 1, wherein there is a space between the neighboring data lines to prevent them from short circuit.

5. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 1, wherein the gate driver is a chip installed on glass.

6. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 1, wherein the gate driver is an integrated gate driver circuit installed on glass.

7. (Original) A driving method for the liquid crystal display of matrix structure type including:

a. making use of the liquid crystal display driving device as claimed in claim 1, wherein there are  $2(m+n)$ , i.e.  $N=2(m+n)$ , gate lines in the liquid crystal display, the period of the predetermined voltage of over drive received by the thin film transistor connected with the first gate line is set as a over exciting period, and the period of the data voltage of the present frame interval received by the thin film transistor connected with the first gate line is set as a brightness keeping period;

b. when the over exciting period begins, the first gate line and the  $2n^{\text{th}}$  gate line are simultaneously turned on, the predetermined voltage of the over drive for the frame is given to the thin film transistor connected with the first gate line, the data voltage of the preceding frame is given to the thin film transistor connected with the  $2n^{\text{th}}$  gate line, and the second and the  $(2n+1)^{\text{th}}$  gate lines, the third and the  $(2n+2)^{\text{th}}$  gate lines... and the  $(2m-1)^{\text{th}}$  and the  $[2(n+m)-2]^{\text{th}}$  gate lines are orderly and simultaneously turned on, the predetermined

voltage is given to the thin film transistors connected with the second to the  $(2m-1)^{\text{th}}$  gate lines, the data voltage of the preceding frame is given to the thin film transistors connected with the  $(2n+1)^{\text{th}}$  to the  $[2(m+n)-2]^{\text{th}}$  gate lines;

c. (Original) when the brightness keeping period begins, the  $2m^{\text{th}}$  and the first gate lines are simultaneously turned on, the predetermined voltage is given to the thin film transistors connected with the  $2m^{\text{th}}$  gate line, the data voltage of the preceding frame interval is given to the thin film transistors connected with the first gate line, and the  $(2m+1)^{\text{th}}$  and the second gate lines, the  $(2m+2)^{\text{th}}$  and the third gate lines... and the  $[2(m+n)]^{\text{th}}$  (the last) and the  $(2n-1)^{\text{th}}$  gate lines are orderly and simultaneously turned on, the predetermined voltage is given to the thin film transistors connected with the  $(2m+1)^{\text{th}}$  to the  $[2(m+n)]^{\text{th}}$  (the last) gate lines, the data voltage of the present frame interval is given to the thin film transistors connected with the second and the  $(2n-1)^{\text{th}}$  gate lines;

by using of the steps stated above, the response speed of the liquid crystal display can be increased.

8. (Original) The driving method for liquid crystal display of matrix structure type as claimed in claim 7, wherein the driving method suits for the active matrix type liquid crystal display, the organic light emitting diode (OLED) display or plasma display panel (PDP).

9. (Original) A liquid crystal display driving device of matrix structure type including:  
a group of thin film transistors with matrix array consisting of  $2N$  rows and  $M$  columns of thin film transistors, wherein each transistor can drive one pixel, therefore, total  $2N \times M$  of pixels can be driven;

a group of  $N$  gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first and the second rows, the second gate line is connected with the gates of all the thin film

transistors of the third and the fourth rows. . . and the  $N^{\text{th}}$  gate line is connected with the gates of all the thin film transistors of the  $(2N-1)^{\text{th}}$  and the  $(2N)^{\text{th}}$  rows; and

M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second data lines of the first group of data lines are respectively connected with the sources of all the thin film transistors of the odd rows and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd rows and the even rows of the second column. . . and the first and the second data lines of the  $M^{\text{th}}$  groups of data lines are respectively connected with the sources of all the thin film transistors of the odd rows and the even rows of the  $M^{\text{th}}$  column.

10. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 9, wherein the first data line of each group of data lines and the second data line of each group of data lines are respectively given data from two groups of source drivers, the two groups of source drivers are respectively installed on the upper side and the lower side of the liquid crystal display.

11. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 9, wherein the first data line and the second data line of each group of data lines are connected with the same source driver, each source driver is installed on the same side of the display panel and the data transfer is switched by an electronic switch.

12. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 9, wherein there is a space between the neighboring data lines to prevent them from short circuit.

13. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 9, wherein the gate driver is a chip installed on glass.

14. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 9, wherein the gate driver is an integrated gate driver circuit installed on glass.

15. (Original) A driving method for the liquid crystal display of matrix structure type including:

a. making use of the liquid crystal display driving device as claimed in claim 9, wherein there are  $m+n$ , i.e.  $N=m+n$ , gate lines in the liquid crystal display, the period of the predetermined voltage of the over drive received by the thin film transistors connected with the first gate line is set as a over exciting period, and the period of the data voltage of the present frame interval received by the thin film transistor connected with the first gate line is set as a brightness keeping period;

b. when the over exciting period begins, the first and the  $n^{\text{th}}$  gate lines are orderly turned on in a time of one synchronous control signal, the predetermined voltage of the over drive for the frame and the data voltage of the preceding frame are respectively given to the thin film transistor connected with the first and the  $n^{\text{th}}$  gate lines, and the second and the  $(n+1)^{\text{th}}$  gate lines, the third and the  $(n+2)^{\text{th}}$  gate lines. . . and the  $m^{\text{th}}$  and the  $(m+n-1)^{\text{th}}$  gate lines are orderly turned on in a time of synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the second to the  $m^{\text{th}}$  gate lines, the data voltage of the preceding frame is given to the thin film transistors connected with the  $(n+1)^{\text{th}}$  to the  $(m+n-1)^{\text{th}}$  gate lines;

c. when the brightness keeping period begins, the  $(m+1)^{\text{th}}$  and the first gate lines are orderly turned on in a time of one synchronous control signal, the predetermined voltage and the data voltage of the present frame interval are respectively given to the thin film transistors connected with the  $(m+1)^{\text{th}}$  and the first gate lines, and the  $(m+2)^{\text{th}}$  and the second gate lines, the  $(m+3)^{\text{th}}$  and the third gate lines. . . and the  $(m+n)^{\text{th}}$  (the last) and the  $(n-1)^{\text{th}}$  gate lines are orderly and synchronously turned on, the predetermined voltage is

given to the thin film transistors connected with the  $(m+2)^{\text{th}}$  to the  $(m+n)^{\text{th}}$  (the last) gate lines, the data voltage of the present frame interval is given to the thin film transistors connected with the second to the  $(n-1)^{\text{th}}$  gate lines;

by using of the steps stated above, the response speed of the liquid crystal display can be increased.

16. (Original) The driving method for the liquid crystal display of matrix structure type as claimed in claim 15, wherein the driving method suits for the active matrix type liquid crystal display, the organic light emitting diode (OLED) display or the plasma display panel (PDP).

17. (Original) A liquid crystal display driving device of matrix structure type including:  
a group of thin film transistors with matrix array consisting of  $N$  rows and  $2M$  columns of thin film transistors, wherein each thin film transistor can drive one pixel, therefore total  $N \times 2M$  of pixels can be driven;

$N$  groups of gate lines connected with the gate drivers and insulated with each other, wherein the first and the second gate lines of the first group of gate lines are respectively connected with the gates of all the thin film transistors of the odd column and the even column of the first row, the first and the second gate lines of the second group of gate lines are respectively connected with the gates of all the thin film transistors of the odd column and the even column of the second row. . . and the first and the second gate lines of the  $N^{\text{th}}$  group of gate lines are respectively connected with the gates of all the thin film transistors of the odd column and the even column of the  $N^{\text{th}}$  row; and

a group of  $M$  data lines connected with the source drivers and insulated with each other, wherein the first data line is connected with the sources of all the thin film transistors of the first column and the second column, the second data line is connected with the sources of all the thin film transistors of the third column and the fourth column. . . and the

$M^{\text{th}}$  data line is connected with the sources of all the thin film transistors of the  $(2M-1)^{\text{th}}$  column and the  $2M^{\text{th}}$  column.

18. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 17, wherein the first gate lines and second gate lines of each group of gate lines are respectively given data by two groups of gate drivers, the two groups of gate drivers are respectively installed on the left side and the right side of the liquid crystal display.

19. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 17, wherein there is a space between the neighboring gate lines to prevent them from short circuit.

20. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 17, wherein the gate driver is a chip installed on glass.

21. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 17, wherein the gate driver is an integrated gate driver circuit installed on glass.

22. (Original) A driving method for the liquid crystal display of matrix structure type including:

a. making use of the liquid crystal display driving device as claimed in claim 17, wherein there are  $2(m+n)$ , i.e.  $N=2(m+n)$ , gate lines in the liquid crystal display, the period of predetermined voltage of the over drive received by the thin film transistors connected with the first gate line of the first group of gate lines is set as a over exciting period, and the period of the data voltage of the present frame interval received by the thin film transistors connected with the first gate line of the first group of gate lines is set as a brightness keeping period;

b. when the over exciting period begins, the first and the second gate lines of the first group of gate lines are orderly turned on in a time of synchronous control signal, the predetermined voltage of the over drive for the frame is given to the thin film transistors connected with the gate lines, and the first and the second gate lines of the  $n^{\text{th}}$  group of gate lines are orderly turned on by the synchronous control signal, the data voltage of the preceding frame is given to the thin film transistors connected with the gate lines, and the first and second gate lines of the second group of gate lines, the first and the second gate lines of the  $(n+1)^{\text{th}}$  group of gate lines... the first and the second gate lines of the  $(m+n)^{\text{th}}$  group of gate lines are orderly turned on in a time of synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the second group to the  $(m+1)^{\text{th}}$  group of gate lines, the data voltage of the preceding frame is given to the thin film transistors connected with the  $(n+1)^{\text{th}}$  group to the  $(m+n-1)^{\text{th}}$  group of gate lines;

c. when the brightness keeping period begins, the first and the second gate lines of the first group of gate lines are orderly turned on in a time of one synchronous control signal, the data voltage of the present frame interval is given to the thin film transistors connected with the gate lines, and the first and the second gate lines of the  $(m+2)^{\text{th}}$  group of gate lines are orderly turned on by the synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the gate lines, and the first and the second gate lines of the second group of gate lines, the first and the second gate lines of the  $(m+3)^{\text{th}}$  group of gate lines... the first and the second gate lines of the  $(n-1)^{\text{th}}$  group of gate lines and the first and the second (i.e. the last) gate lines of the  $(m+n)^{\text{th}}$  group of gate lines are orderly and synchronously turned on, the data voltage of the present frame interval is given to the thin film transistors connected with the second group to the  $(n-1)^{\text{th}}$  group of gate lines, the predetermined voltage is given to the thin film transistors connected with the  $(m+4)^{\text{th}}$  group to the  $(m+n)^{\text{th}}$  group of gate lines;

by using of the steps stated above, the response speed of the liquid crystal display can be increased.

23. (Original) The driving method for the liquid crystal display of matrix structure type as claimed in claim 22, wherein the driving method suits for the active matrix type liquid crystal display, the organic light emitting diode (OLED) display or plasma display panel (PDP).

24. (Original) A the liquid crystal display driving device of matrix structure type including:

a group of thin film transistors with matrix array consisting of  $2N$  rows and  $M$  columns of thin film transistors, wherein each transistor can drive one pixel, therefore total  $2N \times M$  of pixels can be driven;

$N$  groups of gate lines connected with the gate drivers and insulated with each other, wherein the first gate line of the first group of gate lines is connected with the gates of all the thin film transistors of the first row, the second gate line of the first group of gate lines is respectively connected with the gates of all the thin film transistors of the second row. . . and the second gate line of the  $N^{\text{th}}$  group of gate lines is respectively connected with the gates of all the thin film transistors of the  $2N^{\text{th}}$  row; and

a group of  $M+1$  data lines connected with the source drivers and insulated with each other, wherein the first and the second data lines are respectively connected with the sources of all the thin film transistors of the odd rows and the even rows of the first column, the second and the third data lines are respectively connected with the sources of all the thin film transistors of the odd rows and the even rows of the second column. . . and the  $M^{\text{th}}$  and the  $(M+1)^{\text{th}}$  gate lines are respectively connected with the sources of all the thin film transistors of the odd rows and the even rows of the  $M^{\text{th}}$  column.

25. (Original) A the liquid crystal display driving device of matrix structure type as claimed in claim 24, wherein the first gate lines and the second gate lines of each group of gate lines are respectively given data by two groups of gate drivers, the two groups of gate

drivers are respectively installed on the left side and the right side of the liquid crystal display.

26. (Original) A the liquid crystal display driving device of matrix structure type as claimed in claim 24, wherein the gate driver is a chip installed on glass.

27. (Original) A the liquid crystal display driving device of matrix structure type as claimed in claim 24, wherein the gate driver is an integrated gate driver circuit installed on glass.

28. (Original) A the liquid crystal display driving device of matrix structure type including:

a group of thin film transistors with matrix array consisting of  $2N$  rows and  $M$  columns of thin film transistors, wherein each transistor can drive one pixel, therefore total  $2N \times M$  pixels can be driven;

$N$  groups of gate lines connected with the gate drivers and insulated with each other, wherein the first gate line of the first group of gate lines is connected with the gates of all the thin film transistors of the first row, the second gate line of the first group of gate lines is respectively connected with the gates of all the thin film transistors of the second row. . . and the second gate line of the  $N^{\text{th}}$  group of gate lines is respectively connected with the gates of all the thin film transistors of the  $N^{\text{th}}$  row; and

a group of  $M$  data lines connected with the source drivers and insulated with each other, wherein the first data line is connected with the sources of all the thin film transistors of the first column, the second data line is connected with the sources of all the thin film transistors of the second column. . . and the  $M^{\text{th}}$  data line is respectively connected with the sources of all the thin film transistors of the  $M^{\text{th}}$  column.

29. (Original) A the liquid crystal display driving device of matrix structure type as claimed in claim 28, wherein the first gate lines and the second gate lines of each group of gate lines are respectively given data by two groups of gate drivers, the two groups of gate drivers are respectively installed on the left side and the right side of the liquid crystal display.

30. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 28, wherein the gate driver is a chip installed on glass.

31. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 28, wherein the gate driver is an integrated gate driver circuit installed on glass.

32. (Original) A driving method for liquid crystal display of matrix structure type including:

a. making use of the liquid crystal display driving device as claimed in claim 24 or 28, wherein there are  $2m+2n$ , i.e.  $N=2m+2n$ , gate lines in the liquid crystal display, the period of predetermined voltage of the over drive received by the thin film transistors connected with the first gate line of the first group of gate lines is set as a over exciting period, the period of the data voltage of the present frame interval received by the thin film transistors connected with the first gate line of the first group of gate lines is set as a brightness keeping period;

b. when the over exciting period begins, the first and the second gate lines of the first group of gate lines are orderly turned on in a time of one synchronous control signal, the predetermined voltage of the over drive for the frame is given to the thin film transistors connected with the gate lines, and the first and the second gate lines of the  $n$ th group of gate lines are orderly turned on by the synchronous control signal, the data voltage of the preceding frame is given to the thin film transistors connected with the gate lines, and

the first and the second gate lines of the second group of gate lines, the first and the second gate lines of the  $(n+1)$ <sup>th</sup> group of gate lines. . . the first and the second gate lines of the  $(m+n-1)$ <sup>th</sup> group of gate lines and the first and the second gate lines of the  $(m+1)$ <sup>th</sup> group of gate lines are orderly turned on in a time of the synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the second group to the  $(m+1)$ <sup>th</sup> group of gate lines, the data voltage of the preceding frame is given to the thin film transistors connected with the  $(n+1)$ <sup>th</sup> group to the  $(m+n-1)$ <sup>th</sup> group of gate lines;

c. when the brightness keeping period begins, the first and the second gate lines of the first group of gate lines are orderly turned on in a time of one synchronous control signal, the data voltage of the present frame interval is given to the thin film transistors connected with the gate lines, and the first and the second gate lines of the  $(m+2)$ <sup>th</sup> group of gate lines are orderly turned on by the synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the gate lines, and the first and the second gate lines of the second group of gate lines, the first and the second gate lines of the  $(m+3)$ <sup>th</sup> group of gate lines. . . the first and the second gate lines of the  $(m+n)$ <sup>th</sup> group of gate lines and the first and the second gate lines of the  $(n-1)$ <sup>th</sup> group of gate lines are orderly and synchronously turned on, the predetermined voltage is given to the thin film transistors connected with the  $(m+3)$ <sup>th</sup> group to the last gate line, the data voltage of the present frame interval is given to the thin film transistors connected with the second group to the  $(n-1)$ <sup>th</sup> group of gate lines;

by using of the steps stated above, the response speed of the liquid crystal display can be increased.

33. (Original) The driving method for liquid crystal display of matrix structure type as claimed in claim 32, wherein the driving method suits for the active matrix type liquid

crystal display, the organic light emitting diode (OLED) display or plasma display panel (PDP).

34. (Original) A driving method for liquid crystal display of matrix structure type including:

a. making use of the liquid crystal display driving device as claimed in claim 24 or 28, wherein there are  $2m+2n$ , i.e.  $N=2m+2n$ , gate lines in the liquid crystal display, the period of predetermined voltage of the over drive received by the thin film transistors connected with the first gate line of the first group of gate lines is set as a over exciting period, the period of the data voltage of the present frame interval received by the thin film transistors connected with the first gate line of the first group of gate lines is set as a brightness keeping period;

b. when the over exciting period begins, the first gate line of the first group of gate lines and the first gate line of the  $n^{\text{th}}$  group of gate lines are orderly turned on in a time of one synchronous control signal, the predetermined voltage of the over drive for the frame and the data voltage of the preceding frame are respectively given to the thin film transistors connected with the gate lines, and the second gate line of the first group of gate lines and the second gate line of the  $n^{\text{th}}$  group of gate lines, the first gate line of the second group of gate lines and the first gate line of the  $(n+1)^{\text{th}}$  group of gate lines... and the second gate line of the  $(m+n-1)^{\text{th}}$  group of gate lines and the second gate lines of the  $(m+1)^{\text{th}}$  group of gate lines are orderly and synchronously turned on by the synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the first group to the  $(m+1)^{\text{th}}$  group of gate lines, the data voltage of the preceding frame is given to the thin film transistors connected with the  $(n+1)^{\text{th}}$  group to the  $(m+n-1)^{\text{th}}$  group of gate lines;

c. when the brightness keeping period begins, the first gate line of the first group of gate lines and the first gate line of the  $(m+2)^{\text{th}}$  group of gate lines are orderly turned on in a time of one synchronous control signal, the data voltage of the frame interval

and the predetermined voltage are respectively given to the thin film transistors connected with the gate lines, and the second gate line of the first group of gate lines and the second gate line of the  $(m+2)^{\text{th}}$  group of gate lines, the first gate line of the second group of gate lines and the first gate line of the  $(m+3)^{\text{th}}$  group of gate lines... and the second gate line of the  $(n-1)^{\text{th}}$  group of gate lines and the second (i.e. the last) gate line of the  $(m+n)^{\text{th}}$  group gate lines are orderly and synchronously turned on, the data voltage of the present frame interval is given to the thin film transistors connected with the second group to the  $(n-1)^{\text{th}}$  group of gate lines, the predetermined voltage is given to the thin film transistors connected with the  $(m+2)^{\text{th}}$  group to the last gate lines;

by using of the steps stated above, the response speed of the liquid crystal display can be increased.

35. (Original) The driving method for the liquid crystal display of matrix structure type as claimed in claim 34, wherein the driving method suits for the active matrix type liquid crystal display, the organic light emitting diode (OLED) display or the plasma display panel (PDP).

36. (Original) A liquid crystal display driving device of matrix structure type including:  
a group of thin film transistors with matrix array consisting of N rows and 2M columns of thin film transistors, wherein each pair of neighboring thin film transistors can drive one pixel, therefore, total N x M of pixels can be driven;

N groups of gate lines connected with the gate drivers and insulated with each other, wherein the first and the second gate line of the first group of gate lines are respectively connected with the gates of all the thin film transistors of the odd column and the even column of the first row, the first and the second gate lines of the second group of gate lines are respectively connected with the gates of all the thin film transistors of the odd column and the even column of the second row. . . and the first and the second gate lines of the  $N^{\text{th}}$

group of gate lines are respectively connected with the gates of all the thin film transistors of the odd column and the even column of the  $N^{\text{th}}$  row; and

a group of  $2M$  data lines connected with the source drivers and insulated with each other, wherein the first data line is connected with the sources of all the thin film transistors of the first column, the second data line is connected with the sources of all the thin film transistors of the second column. . . and the  $2M^{\text{th}}$  data line is connected with the sources of all the thin film transistors of the  $2M^{\text{th}}$  column.

37. The liquid crystal display driving device of matrix structure type as claimed in claim 36, wherein the first gate lines and the second gate lines of each group of gate lines are respectively given data by two groups of gate drivers, the two groups of gate drivers are respectively installed on the left side and the right side of the liquid crystal display.

38. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 36, wherein there is a space between the neighboring gate lines to prevent them from short circuit.

39. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 36, wherein the gate driver is a chip installed on glass.

40. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 36, wherein the gate drive is an integrated gate driver circuit installed on glass.

41. (Original) A driving method for the liquid crystal display driving device of matrix structure type including:

a. making use of the liquid crystal display driving device as claimed in claim 36, wherein there are  $2(m+n)$ , i.e.  $N=2(m+n)$ , gate lines in the liquid crystal display, the

period of the predetermined voltage of the over drive received by the thin film transistors connected with the first gate line of the first group of gate lines is set as a over exciting period, and the period of the data voltage of the present frame interval received by the thin film transistors connected with the second gate line of the first group of gate lines is set as a brightness keeping period;

b. when the over exciting period begins, the first gate line of the first group of gate lines and the second gate line of the  $n$ th group of gate lines are orderly turned on in a time of one synchronous control signal, the predetermined voltage of the over drive for the frame and the data voltage of the preceding frame are respectively given to the thin film transistors connected with the gate lines, and the first gate line of the second group of gate lines and the second gate line of the  $(n+1)$ <sup>th</sup> group of gate lines, the first gate line of the third group of gate lines and the second gate line of the  $(n+2)$ <sup>th</sup> group of gate lines... and the second gate line of the  $(m+n-1)$ <sup>th</sup> group of gate lines and the first gate line of the  $(m+1)$ <sup>th</sup> group of gate lines are orderly turned on in a time of the synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the first gate line of the second group to the  $(m+1)$ <sup>th</sup> group of gate lines, the data voltage of the preceding frame is given to the thin film transistors connected with the second gate line of the  $(n+1)$ <sup>th</sup> group to the  $(m+n-1)$ <sup>th</sup> group of gate lines;

c. when the brightness keeping period begins, the second gate line of the first group of gate lines and the first gate line of the  $(m+2)$ <sup>th</sup> group of gate lines are orderly turned on in a time of one synchronous control signal, the data voltage of the frame interval and the predetermined voltage are respectively given to the thin film transistors connected with the gate lines, and the first gate line of the  $(m+3)$ <sup>th</sup> group of gate lines and the second gate line of the second group of gate lines, the first gate line of the  $(m+4)$ <sup>th</sup> group of gate lines and the second gate line of the third group of gate lines. . . and the first gate line of the  $(m+n)$ <sup>th</sup> group of gate lines and the second gate line of the  $(n-1)$ <sup>th</sup> group of gate lines are orderly and synchronously turned on, the data voltage of the present frame interval is given

to the thin film transistors connected with the second gate line of the second group to the (n-1)<sup>th</sup> group of gate lines, the predetermined voltage is given to the thin film transistors connected with the first gate line of the (m+3)<sup>th</sup> group to the (m+n)<sup>th</sup> group of gate lines;

by using of the steps stated above, the response speed of the liquid crystal display can be increased .

42. (Original) The driving method for the liquid crystal display of matrix structure type as claimed in claim 41, wherein the driving method suits for the active matrix type liquid crystal display, the organic light emitting diode (OLED) display or plasma display panel (PDP).

43. (Original) A liquid crystal display driving device of matrix structure type including:

a group of thin film transistors with matrix array consisting of N rows and 2M columns of thin film transistors, wherein each pair of neighboring thin film transistors can drive one pixel, therefore total N x M of pixels can be driven;

a group of N gate lines connected with the gate drivers and insulated with each other, wherein the first and the second gate lines are respectively connected with the gates of all the thin film transistors of the odd column and the even column of the first row, the second and the third gate lines are respectively connected with the gates of all the thin film transistors of the odd columns and the even columns of the second row. . . and the N<sup>th</sup> and the (N+ 1)<sup>th</sup> gate lines are respectively connected with the gates of all the thin film transistors of the odd columns and the even columns of the N<sup>th</sup> row; and

M group of data lines connected with the source drivers and insulated with each other, wherein the first data line of the first group of date lines is connected with the sources of all the thin film transistors of the first column, the second data line of the first group of data lines is connected with the sources of all the thin film transistors of the second column. . . and the second data line of the M<sup>th</sup> group of data lines is connected with the

sources of all the thin film transistors of the odd rows and the even rows of the 2M<sup>th</sup> column.

44. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 43, wherein there further is one row of thin film transistors installed above the first row of thin film transistors, each thin film transistor can control one pixel, the gates of the row of thin film transistors are connected with the first gate line and their sources are connected with the second data line of each group of data lines.

45. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 43, wherein the first data lines and the second data lines of each group of data lines are respectively given data by two groups of source drivers, and the two groups of source drivers are respectively installed on the upper side and the lower side of the liquid crystal display.

46. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 44, wherein the first data line and the second data lines of each group of data lines are respectively given data by two groups of source drivers, and the two groups of source drivers are respectively installed on the upper side and the lower side of the liquid crystal display.

47. (Original) The liquid crystal display driving device of matrix Structure type as claimed in claim 43, wherein the first data lines of each group of data lines and the second data lines of each group of data lines are connected with the same source driver, each source driver is installed on the same side of the display panel, and there is an electronic switch installed on the source driver for switching the data transfer.

48. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 44, wherein the first data lines of each group of data lines and the second

data lines of each group of data lines are connected with the same source driver, each source driver is installed on the same side of the display panel, and there is an electronic switch installed on the source driver for switching the data transfer.

49. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 43, wherein there is a space between the neighboring gate lines to prevent them from short circuit.

50. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 44, wherein there is a space between the neighboring gate lines to prevent them from short circuit.

51. (Original) The liquid crystal display driving device of matrix Structure type as claimed in claim 43, wherein the gate driver is a chip installed on glass.

52. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 44, wherein the gate driver is a chip installed on glass.

53. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 43, wherein the gate driver is an integrated gate driver circuit installed on glass.

54. (Original) The liquid crystal display driving device of matrix structure type as claimed in claim 44, wherein the gate driver is an integrated gate driver circuit installed on glass.

55. (Currently Amended) A driving method for the liquid crystal display driving device of matrix structure type including:

a. making use of the liquid crystal display driving device as claimed in claim 43 or 44, wherein there are  $m+n$ , i.e.  $N=m+n$ , gate lines in the liquid crystal display, the period of predetermined voltage of the over drive received by the thin film transistors connected with the first gate line is set as a over exciting period, and the period of data voltage of the present frame interval received by the thin film transistors connected with the first gate line is set as a brightness keeping period;

b. when the over exciting period begins, the first and the  $(n+1)^{\text{th}}$  gate lines are orderly turned on in a time of one synchronous control signal, the predetermined voltage of over drive for the frame and the data voltage for the preceding frame are given to the thin film transistors connected with the gate lines, and the second and the  $(n+2)^{\text{th}}$  gate lines, the third and the  $(n+3)^{\text{th}}$  gate lines... and the  $(m+n-1)^{\text{th}}$  and the  $m^{\text{th}}$  gate lines are orderly and synchronously turned on in a time of the synchronous control signal, the predetermined voltage is given to the thin film transistors connected with the second to the  $m^{\text{th}}$  gate lines, the data voltage for the preceding frame is given to the thin transistors connected with the  $(n+2)^{\text{th}}$  to the  $(m+n-1)^{\text{th}}$  gate line;

c. when the brightness keeping period begins, the first and the  $(m+1)^{\text{th}}$  gate lines are orderly turned on in a time of one synchronous control signal the data voltage of the frame interval and the predetermined voltage are given to the thin film transistors connected with the gate lines, and the second and the  $(m+2)^{\text{th}}$  gate lines, the third and the  $(m+3)^{\text{th}}$  gate lines... and the  $(m+n)^{\text{th}}$  (i.e. the last) and the  $n^{\text{th}}$  gate lines are orderly and synchronously turned on, the predetermined voltage is given to the thin film transistors connected with the  $(m+2)^{\text{th}}$  to the  $(m+n)^{\text{th}}$  (i.e. the last) gate line, the data voltage of the present frame interval is given to the thin film transistors connected with the second to the  $n^{\text{th}}$  gate line;

by using of the steps stated above, the response speed of the liquid crystal display can be increased.

56. (Original) The driving method for the liquid crystal display of matrix structure type as claimed in claim 55, wherein the driving method suits for the active matrix type liquid

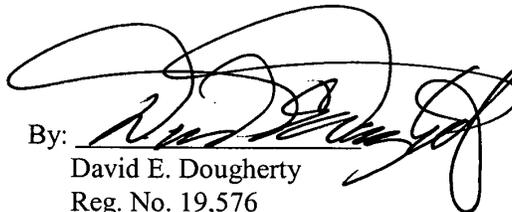
crystal display, the organic light emitting diode (OLED) display or plasma display panel (PDP).

**REMARKS**

By this Preliminary Amendment, Applicant has amended claim 55 in order to eliminate multiple dependencies.

Prompt, favorable action is requested.

Respectfully submitted,

By:   
David E. Dougherty  
Reg. No. 19,576

March 18, 2005  
Date

**PATENT APPLICATION FEE DETERMINATION RECORD**  
Effective October 1, 2003

Application or Docket Number

10/929473

**CLAIMS AS FILED - PART I**

	(Column 1)	(Column 2)
TOTAL CLAIMS	56	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	62 minus 20 =	42
INDEPENDENT CLAIMS	7 minus 3 =	4
MULTIPLE DEPENDENT CLAIM PRESENT <input checked="" type="checkbox"/>		

\* If the difference in column 1 is less than zero, enter "0" in column 2

**CLAIMS AS AMENDED - PART II**

2/7/03

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	62	62	-
Independent	7	7	-
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

**BEST AVAILABLE COPY**

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	56	62	-
Independent	7	7	-
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total			
Independent			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

\* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.  
 \*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."  
 \*\*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."  
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SMALL ENTITY TYPE  OR OTHER THAN SMALL ENTITY

RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
XS 9=	378	OR	XS18=	
X43=	172	OR	X86=	
+145=	145	OR	+290=	
TOTAL	1080	OR	TOTAL	

SMALL ENTITY OR OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

BEST AVAILABLE COPY



APR 26 2006

PTO/SB/122 (01-05)

Approved for use through 12/31/2008. OMB 0651-0035 U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

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<b>CHANGE OF CORRESPONDENCE ADDRESS</b> <i>Application</i>  Address to: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450	Application Number	10/929,473
	Filing Date	8-31-2004
	First Named Inventor	Yuh-Ken Shen
	Art Unit	2871
	Examiner Name	TBA
	Attorney Docket Number	3079/255

Please change the Correspondence Address for the above-identified patent application to:

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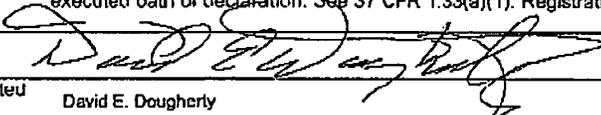
I am the:

Applicant/Inventor

Assignee of record of the entire interest. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/95)

Attorney or agent of record. Registration Number 19,576

Registered practitioner named in the application transmittal letter in an application without an executed oath or declaration. See 37 CFR 1.33(a)(1). Registration Number \_\_\_\_\_

Signature 

Typed or Printed Name David E. Dougherty

Date April 25, 2006 Telephone (703) 684-1111

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

Total of \_\_\_\_\_ forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 2 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT APPLICATION FEE DETERMINATION RECORD  
Effective December 8, 2004

10/929,473

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20= *	
INDEPENDENT CLAIMS	minus 3 = *	
MULTIPLE DEPENDENT CLAIM PRESENT <input type="checkbox"/>		

\* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE  OR OTHER THAN SMALL ENTITY

RATE	FEE		RATE	FEE
BASIC FEE	150.00	OR	BASIC FEE	300.00
X\$ 25=		OR	X\$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

10/10/06

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	* 29	Minus ** 29	= 0
Independent	* 2	Minus *** 3	= 0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

SMALL ENTITY OR OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X\$ 25=		OR	X\$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X\$ 25=		OR	X\$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X\$ 25=		OR	X\$50=	
X100=		OR	X200=	
+180=		OR	+360=	



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D

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/929,473	08/31/2004	Yuh-Ren Shen	3079/255	6164

22429 7590 09/20/2007  
LOWE HAUPTMAN HAM & BERNER, LLP  
1700 DIAGONAL ROAD  
SUITE 300  
ALEXANDRIA, VA 22314

EXAMINER

KOVALICK, VINCENT E

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
09/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/929,473	SHEN ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Vincent E. Kovalick	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1)  Responsive to communication(s) filed on 31 August 2004.
- 2a)  This action is **FINAL**.
- 2b)  This action is non-final.
- 3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4)  Claim(s) 1-56 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5)  Claim(s) \_\_\_\_\_ is/are allowed.
- 6)  Claim(s) \_\_\_\_\_ is/are rejected.
- 7)  Claim(s) \_\_\_\_\_ is/are objected to.
- 8)  Claim(s) 1-56 are subject to restriction and/or election requirement.

**Application Papers**

- 9)  The specification is objected to by the Examiner.
- 10)  The drawing(s) filed on 31 August 2004 is/are: a)  accepted or b)  objected to by the Examiner.
  - Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
  - Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a)  All   b)  Some \*   c)  None of:
    - 1.  Certified copies of the priority documents have been received.
    - 2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    - 3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1)  Notice of References Cited (PTO-892)
- 2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3)  Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5)  Notice of Informal Patent Application
- 6)  Other: \_\_\_\_\_

**DETAILED ACTION**

1. This Office Action is in response to Applicant's Patent Application, Serial No. 10/929,473, with a File Date of August 31, 2004.

*Election of Species*

2. This application contains claims directed to the following patentable distinct species:

o Figs. 4A – 4C	constitute	Species I
o Figs, 8A – 8C	constitute	Species II
o Figs. 12A –12C	constitute	Species III
o Figs, 15A –15B	constitute	Species IV
o Figs. 19A –19C	constitute	Species V
o Figs. 22A – 22C	constitute	Species VI

3. The species are independent or distinct because they relate to a variety of aspects corresponding to the makeup and functionality of LCD matrix structure types and driving methods.

4. Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, there are no generic claims.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable

thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

5. Should Applicant traverse on the ground that the species are not patentably distinct, Applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is that case. In either instance, if the Examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

***To Respond***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E. Kovalick whose telephone number is 571-272-7669. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Vincent E. Kovalick  
August 30, 2007



BIPIN SHALWALA  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600



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Bib Data Sheet

CONFIRMATION NO. 6164

<b>SERIAL NUMBER</b> 10/929,473	<b>FILING OR 371(c) DATE</b> 08/31/2004	<b>CLASS</b> 345	<b>GROUP ART UNIT</b> 2629	<b>ATTORNEY DOCKET NO.</b> 3079/255
<b>RULE</b>				

**APPLICANTS**  
 Yuh-Ren Shen, Tainan, TAIWAN;  
 Cheng-Jung Chen, Chunan Town, TAIWAN;  
 Chun-Chi Chen, Kaohsiung City, TAIWAN;

**\*\* CONTINUING DATA \*\*\*\*\***

**\*\* FOREIGN APPLICATIONS \*\*\*\*\***

**IF REQUIRED, FOREIGN FILING LICENSE GRANTED\*\* SMALL ENTITY \*\***  
**\*\* 11/01/2004**

Foreign Priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	<b>STATE OR COUNTRY</b> TAIWAN	<b>SHEETS DRAWING</b> 26	<b>TOTAL CLAIMS</b> 56	<b>INDEPENDENT CLAIMS</b> 7
35 USC 119 (a-d) conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> Met after Allowance				
Verified and Acknowledged Examiner's Signature: <i>[Signature]</i> Initials: <i>UK</i>				

**ADDRESS**  
 22429

**TITLE**  
 Liquid crystal display driving device of matrix structure type and its driving method

<b>FILING FEE RECEIVED</b> 1096	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	<input type="checkbox"/> All Fees
		<input type="checkbox"/> 1.16 Fees ( Filing )
		<input type="checkbox"/> 1.17 Fees ( Processing Ext. of time )
		<input type="checkbox"/> 1.18 Fees ( Issue )
		<input type="checkbox"/> Other _____
		<input type="checkbox"/> Credit

**Index of Claims**



Application/Control No.

10/929,473

Examiner

Vincent E. Kovalick

Applicant(s)/Patent under Reexamination

SHEN ET AL.

Art Unit

2629

√	Rejected
=	Allowed

-	(Through numeral) Cancelled
+	Restricted

N	Non-Elected
I	Interference

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Docket No.: 3079D-0255

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :  
Yu-Ren SHEN : Confirmation No.6164  
U.S. Patent Application No. 10/929,473 : Group Art Unit: 2629  
Filed: August 31, 2004 : Examiner: Vincent E. KOVALICK  
For: LIQUID CRYSTAL DISPLAY DRIVING DEVICE OF MATRIX STRUCTURE TYP  
AND ITS DRIVING METHOD

**RESPONSE TO RESTRICTION REQUIREMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

By Official Action mailed September 20, 2007 restriction to one of the following inventions is required under 35 USC 121.

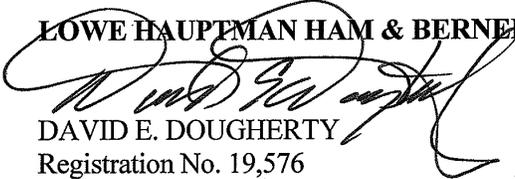
In response, Applicants hereby elect **claims 1-8/Species I; Figures 4A-4C** for examination in this case.

Early examination on the merits is courteously solicited.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

**LOWE HAUPTMAN HAM & BERNER, LLP**



DAVID E. DOUGHERTY  
Registration No. 19,576  
1700 Diagonal Road, Suite 300  
Alexandria, Virginia 22314  
(703) 684-1111 DED/eem  
Facsimile: (703) 518-5499  
**Date: October 15, 2007**

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	2330482
<b>Application Number:</b>	10929473
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	6164
<b>Title of Invention:</b>	Liquid crystal display driving device of matrix structure type and its driving method
<b>First Named Inventor/Applicant Name:</b>	Yuh-Ren Shen
<b>Customer Number:</b>	22429
<b>Filer:</b>	David E Dougherty/Beth Murphy
<b>Filer Authorized By:</b>	David E Dougherty
<b>Attorney Docket Number:</b>	3079/255
<b>Receipt Date:</b>	17-OCT-2007
<b>Filing Date:</b>	31-AUG-2004
<b>Time Stamp:</b>	12:04:26
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	no
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### File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	Response.pdf	39257 <small>425432736ed74900od92f344a26caf9276666f19</small>	no	1

### Warnings:

<b>Information:</b>	
<b>Total Files Size (in bytes):</b>	39257
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b>  If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b>  If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b>  If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>	

## Freeform Search

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 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

**Term:** L18 and @py<=2004

**Display:** 20 Documents in **Display Format:** TI Starting with Number 1

**Generate:**  Hit List  Hit Count  Side by Side  Image

Search
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### Search History

DATE: **Tuesday, November 27, 2007**    [Purge Queries](#)    [Printable Copy](#)    [Create Case](#)

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<u>L19</u>	L18 and @py<=2004	30	<u>L19</u>
<u>L18</u>	(space or distance) near2 between adj data adj lines and short adj circuit\$6	38	<u>L18</u>
<u>L17</u>	L16 and short adj circuit	9	<u>L17</u>
<u>L16</u>	space near2 between adj data adj line\$1	95	<u>L16</u>
<u>L15</u>	space near2 between adj data adj line\$1 same short adj circuit\$1	0	<u>L15</u>
<u>L14</u>	L13 and @py<=2004	13	<u>L14</u>
<u>L13</u>	data adj lines same prevent same short adj circuit\$1 same (space or distance)	23	<u>L13</u>
<u>L12</u>	space near2 between same data adj lines same prevent same short adj circuit\$1	4	<u>L12</u>
<u>L11</u>	l1 and space near2 between same data adj lines same prevent same short adj circuit\$1	3	<u>L11</u>
<u>L10</u>	l9 and gate adj driver\$1 near2 chip near2 glass	2	<u>L10</u>
<u>L9</u>	L8 and LCD same gate adj driver same chip near2 glass	14	<u>L9</u>

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<u>L8</u>	L7 and @py<=2004	109	<u>L8</u>
<u>L7</u>	l1 and gate adj driver same chip same glass	287	<u>L7</u>
<u>L6</u>	L5 and @py<=2004	90	<u>L6</u>
<u>L5</u>	l1 and data adj line\$1 same transistor\$1 same even same odd	174	<u>L5</u>
<u>L4</u>	l3 and data adj line\$1 same transistor\$1	46	<u>L4</u>
<u>L3</u>	L2 and @py<=2004	100	<u>L3</u>
<u>L2</u>	L1 and (dual or multiple) adj data adj lines	195	<u>L2</u>
<u>L1</u>	(LCD or liquid adj crystal adj (display or panel of screen))	521760	<u>L1</u>

END OF SEARCH HISTORY

# Freeform Search

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 IBM Technical Disclosure Bulletins

**Term:** 
 L3 and first adj data adj line same second adj  
 data adj line same switch\$6 near2 driver\$1

**Display:** 20 Documents in **Display Format:** TI Starting with Number 1

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DATE: **Wednesday, November 28, 2007**    [Purge Queries](#)    [Printable Copy](#)    [Create Case](#)

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<u>L14</u>	L3 and first adj data adj line same second adj data adj line same switch\$6 near2 driver\$1	6	<u>L14</u>
<u>L13</u>	L3 and first adj data adj line adj driver same second adj data adj line same driver same switch\$6 near2 driver\$1	0	<u>L13</u>
<u>L12</u>	L3 and first adj data adj line same second adj data adj line same driver same switch\$6	35	<u>L12</u>
<u>L11</u>	110 and switch\$6	22	<u>L11</u>
<u>L10</u>	17 and @py<=2004	32	<u>L10</u>
<u>L9</u>	16 and (common or mutual) adj driver	2	<u>L9</u>
<u>L8</u>	L7 and @py<=2004	32	<u>L8</u>
<u>L7</u>	L3 and first adj data adj line same second adj data adj line same driver	126	<u>L7</u>
<u>L6</u>	L3 and first adj data adj line same second adj data adj line	657	<u>L6</u>
<u>L5</u>	L13 and first adj data adj line same second adj data adj line	0	<u>L5</u>
<u>L4</u>	L3 and (first or second) adj data line\$1	1182	<u>L4</u>
<u>L3</u>	(LCD or liquid adj crystal adj (display or panel or screen))	550496	<u>L3</u>

<u>L2</u>	(LCD or liquid adj crystal adj (dislay or panel or screen))	342810	<u>L2</u>
<u>L1</u>	(space or distance) near2 between adj data adj line\$1 same short adj circuit\$6	13	<u>L1</u>

END OF SEARCH HISTORY

## Freeform Search

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 IBM Technical Disclosure Bulletins

**Term:** 
 L3 and first adj data adj line same second adj  
 data adj line same switch\$6 near2 driver\$1

**Display:** 20 Documents in **Display Format:** TI Starting with Number 1

**Generate:**  Hit List  Hit Count  Side by Side  Image

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<a href="#">L13</a>	L3 and first adj data adj line adj driver same second adj data adj line same driver same switch\$6 near2 driver\$1	0	<a href="#">L13</a>
<a href="#">L12</a>	L3 and first adj data adj line same second adj data adj line same driver same switch\$6	35	<a href="#">L12</a>
<a href="#">L11</a>	110 and switch\$6	22	<a href="#">L11</a>
<a href="#">L10</a>	17 and @py<=2004	32	<a href="#">L10</a>
<a href="#">L9</a>	16 and (common or mutual) adj driver	2	<a href="#">L9</a>
<a href="#">L8</a>	L7 and @py<=2004	32	<a href="#">L8</a>
<a href="#">L7</a>	L3 and first adj data adj line same second adj data adj line same driver	126	<a href="#">L7</a>
<a href="#">L6</a>	L3 and first adj data adj line same second adj data adj line	657	<a href="#">L6</a>
<a href="#">L5</a>	L13 and first adj data adj line same second adj data adj line	0	<a href="#">L5</a>
<a href="#">L4</a>	L3 and (first or second) adj data line\$1	1182	<a href="#">L4</a>
<a href="#">L3</a>	(LCD or liquid adj crystal adj (display or panel or screen))	550496	<a href="#">L3</a>

<u>L2</u>	(LCD or liquid adj crystal adj (dislay or panel or screen))	342810	<u>L2</u>
<u>L1</u>	(space or distance) near2 between adj data adj line\$1 same short adj circuit\$6	13	<u>L1</u>

END OF SEARCH HISTORY

## Refine Search

### Search Results -

Term	Documents
DRIVER	776127
DRIVERS	188438
SWITCHING	1398533
SWITCHINGS	2596
DATA	4373877
DATUM	41259
LINES	2950653
LINE	5965471
(14 AND (DRIVER ADJ SWITCHING ADJ DATA ADJ LINES)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	0
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**Database:**

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**Search:**

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### Search History

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			result set
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L16	114 and driver adj switching adj data adj lines	0	L16

<u>L15</u>	L14 and data adj lines same source adj driver	5	<u>L15</u>
<u>L14</u>	l6 and @py<=2004	85	<u>L14</u>
<u>L13</u>	L12 and @py<=2004	8	<u>L13</u>
<u>L12</u>	L11 and driver\$6	20	<u>L12</u>
<u>L11</u>	L1 and switching adj data adj line\$1	32	<u>L11</u>
<u>L10</u>	L1 and driver adj switch\$6 adj between two near4 data adj line\$1	0	<u>L10</u>
<u>L9</u>	L6 and switch\$6 adj between two near4 data adj line\$1	0	<u>L9</u>
<u>L8</u>	L6 and switch\$6 adj between two near data adj line\$1	0	<u>L8</u>
<u>L7</u>	L6 and switched adj between two near data adj line\$1	0	<u>L7</u>
<u>L6</u>	L4 and data adj line adj driver same switching	85	<u>L6</u>
<u>L5</u>	L4 and data adj line adj driver same switch\$6	172	<u>L5</u>
<u>L4</u>	L3 and @py<=2004	172	<u>L4</u>
<u>L3</u>	data adj line adj driver\$6 same switch\$6	302	<u>L3</u>
<u>L2</u>	L1 and first adj data adj line same second adj data adj line same switch\$6 near2 driver\$1	6	<u>L2</u>
<u>L1</u>	(LCD or liquid adj crystal adj (display\$1 or panel\$1 or screen\$1))	550499	<u>L1</u>

END OF SEARCH HISTORY



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/929,473	08/31/2004	Yuh-Ren Shen	3079/255	6164

22429 7590 12/05/2007  
LOWE HAUPTMAN HAM & BERNER, LLP  
1700 DIAGONAL ROAD  
SUITE 300  
ALEXANDRIA, VA 22314

EXAMINER

KOVALICK, VINCENT E

ART UNIT PAPER NUMBER

2629

MAIL DATE DELIVERY MODE

12/05/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/929,473	<b>Applicant(s)</b> SHEN ET AL.	
	<b>Examiner</b> Vincent E. Kovalick	<b>Art Unit</b> 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1)  Responsive to communication(s) filed on 17 October 2007.
- 2a)  This action is **FINAL**.                      2b)  This action is non-final.
- 3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4)  Claim(s) 1-8 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5)  Claim(s) \_\_\_\_\_ is/are allowed.
- 6)  Claim(s) 1, 2 and 4-6 is/are rejected.
- 7)  Claim(s) 3, 7 and 8 is/are objected to.
- 8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9)  The specification is objected to by the Examiner.
- 10)  The drawing(s) filed on 31 August 2004 is/are: a)  accepted or b)  objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All    b)  Some \*    c)  None of:
1.  Certified copies of the priority documents have been received.
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

1. This Office Action is in response to Applicant's Response to Restriction Requirement dated October 17, 2007 in response to USPTO Office Action dated September 20, 2007.

Applicant's election of claims 1-8/ Species I: Figures 4A-4C has been noted and entered in the record; said claims 1-8 are considered in this action.

***Minor Informalities***

1.1 Claim 7 is objected to because of the following informality:

Claim 7, Para. c, line 1; the first word "(Original)" needs to be deleted.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-2 are rejected under 35 USC 102 as being unpatentable over, Kim et al. (USP 5,805,128)

Relative to claim 1, Kim et al. **teaches** a liquid crystal display driving device of matrix structure type including: a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N x M of pixels can be driven; a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row..., and the Nth gate line is connected with the gates of all the thin film transistors of the Nth row; and M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second data lines of the first group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column..., and the first and the second data lines of the Mth group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the Mth column (col. 3, lines 26-37; col. 4, lines 28-51 and Fig. 5).

Regarding claim 2, Kim further **teaches** the said liquid crystal display driving device of matrix structure type, wherein the first and the second data lines of each group of data lines are given data by two groups of source drivers, respectively, and the two groups of source drivers are respectively arranged on the upper and the lower sides of the liquid crystal display (col. 3, lines 26-37; col. 4, lines 28-51 and Fig. 5).

**Claim Rejections - 35 USC § 103**

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. as applied to claim 1 in item 3 hereinabove, and further in view of Takeuchi et al. (USP 6,157,056).

Relative to claim 4, Kim et al. **does not teach** the said liquid crystal display driving device of matrix structure type wherein there is a space between the neighboring data lines to prevent them from short circuit.

Takeuchi et al. **teaches** a memory device having a plurality of memory cell transistors arranged to constitute memory cell arrays (col. 3, lines 26-6 and col. 6, lines 1-46); Takeuchi et al further the said liquid crystal display driving device of matrix structure type wherein there is a space between the neighboring data lines to prevent them from short circuit (col. 14, lines 38-43 and Fig. 35).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Kim et al. the feature as taught by Takeuchi et al. in order to provide sufficient space in the layout of the data lines to avoid causing a shot circuit.

6. Claim 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. as applied to claim 1 in item 3 hereinabove, and further in view of Chen et al. (Pub. No. 2004/0056331).

Regarding claim 5, Kim et al. **does not teach** the said liquid crystal display driving device of matrix structure type wherein the gate driver is a chip installed on glass.

Chen et al. **teaches** a display panel with bypassing lines (pg. 1, paras. 0007-0009); Chen et al. further **teaches** the said liquid crystal display driving device of matrix structure type wherein the gate driver is a chip installed on glass (pg. 1, para 0005 and Fig. 1).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to

the device as taught by Kim et al. the feature as taught by Chen et al. in order to provide gate drivers compatible with being installed on glass.

Relative to claim 6, Chen et al. further **teaches** the said liquid crystal display driving device of matrix structure type wherein the gate driver is an integrated gate driver circuit installed on glass (pg. 1, para. 0005 and Fig. 1).

***Allowable Subject Matter***

7. Claims 3 and 7-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 3, the major difference between the teachings of the prior art of record (USP 5,805,128, Kim et al.; USP 6,157,056, Takeuchi et al. and (Pub. No. 2004/0056331), Chen et al.) and that of the instant invention is that said prior art of record **does not teach** a liquid crystal display driving device of matrix structure type wherein the first data lines and the second data lines of each group of data lines are connected with the same source driver, each source driver is installed on the same side of the display panel and the data transfer is switched by an electronic switch.

Regarding claim 7, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a driving method for the liquid crystal display of matrix structure type including: a) making use of the liquid crystal display driving device wherein there are  $2(m+n)$ , i.e.  $N=2(m+n)$ , gate lines in the liquid crystal display, the period of the predetermined voltage of over drive received by the thin film transistor connected with the first gate line is set as a over exciting period, and the period of the data voltage of the present frame interval received by the thin film transistor connected with the first gate line is set as a brightness keeping period; b) when the over exciting period begins, the first gate line and the  $2n$ th gate line are simultaneously turned on, the predetermined voltage of the over drive for the frame is given to the thin film transistor connected with the

first gate line, the data voltage of the preceding frame is given to the thin film transistor connected with the 2nth gate line, and the second and the  $(2n+1)$ th gate lines, the third and the  $(2n+2)$ th gate lines..., and the  $(2m-1)$ th and the  $[2(n+m)-2]$ th gate lines are orderly and simultaneously turned on, the predetermined voltage is given to the thin film transistors connected with the second to the  $(2m-1)$ th gate lines, the data voltage of the preceding frame is given to the thin film transistors connected with the  $(2n+1)$ th to the  $[2(m+n)-2]$ th gate lines; c) when the brightness keeping period begins, the 2mth and the first gate lines are Simultaneously turned on, the predetermined voltage is given to the thin film transistors connected with the 2mth gate line, the data voltage of the preceding frame interval is given to the thin film transistors connected with the first gate line, and the  $(2m+1)$ th and the second gate lines, the  $(2m+2)$ th and the third gate lines..., and the  $[2(m+n)]$ th (the last) and the  $(2n-1)$ th gate lines are orderly and simultaneously turned on, the predetermined voltage is given to the thin film transistors connected with the  $(2m+J)$ th to the  $[2(m+n)]$ th (the last) gate lines, the data voltage of the present frame interval is given to the thin film transistors connected with the second and the  $(2n-1)$ th gate lines.

#### **Conclusion**

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No. 6,310,594 Libsch et al.

U. S Patent No. 6,057,904 Kim et al.

Application/Control Number:  
10/929,473  
Art Unit: 2629

Page 7

**To Respond**

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E. Kovalick whose telephone number is 571-272-7669. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
Vincent E. Kovalick  
November 28, 2007

  
BIPIN SHALWALA  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600

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TECHNOLOGY CENTER 2600

<b>Notice of References Cited</b>	Application/Control No. 10/929,473	Applicant(s)/Patent Under Reexamination SHEN ET AL.	
	Examiner Vincent E. Kovalick	Art Unit 2629	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A US-6,310,594	10-2001	Libsch et al.	345/90
*	B US-6,157,056	12-2000	Takeuchi et al.	257/315
*	C US-6,057,904	05-2000	Kim et al.	349/143
*	D US-5,805,128	09-1998	Kim et al.	345/96
*	E US-2004/0056331	03-2004	Chen et al.	257/629
	F US-			
	G US-			
	H US-			
	I US-			
	J US-			
	K US-			
	L US-			
	M US-			

**FOREIGN PATENT DOCUMENTS**

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N				
	O				
	P				
	Q				
	R				
	S				
	T				

**NON-PATENT DOCUMENTS**

*	Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
U				
V				
W				
X				

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
 Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

**Index of Claims**



Application/Control No.

10/929,473

Examiner

Vincent E. Kovalick

Applicant(s)/Patent under Reexamination

SHEN ET AL.

Art Unit

2629

√	Rejected
=	Allowed

-	(Through numeral) Cancelled
+	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claim		Date			
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
 United States Patent and Trademark Office  
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 Alexandria, Virginia 22313-1450  
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BIB DATA SHEET

CONFIRMATION NO. 6164

<b>SERIAL NUMBER</b> 10/929,473	<b>FILING or 371(c) DATE</b> 08/31/2004 <b>RULE</b>	<b>CLASS</b> 349	<b>GROUP ART UNIT</b> 2629	<b>ATTORNEY DOCKET NO.</b> 3079/255	
<b>APPLICANTS</b> Yuh-Ren Shen, Tainan, TAIWAN; Cheng-Jung Chen, Chunan Town, TAIWAN; Chun-Chi Chen, Kaohsiung City, TAIWAN; <b>** CONTINUING DATA *****</b> <b>** FOREIGN APPLICATIONS *****</b> <b>** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** ** SMALL ENTITY **</b> 11/01/2004					
Foreign Priority claimed <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No 35 USC 119(a-d) conditions met <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No <input type="checkbox"/> Met after Allowance Verified and Acknowledged <i>[Signature]</i> Examiner's Signature Initials		<b>STATE OR COUNTRY</b> TAIWAN	<b>SHEETS DRAWINGS</b> 26	<b>TOTAL CLAIMS</b> 568	<b>INDEPENDENT CLAIMS</b> 11
<b>ADDRESS</b> LOWE HAUPTMAN HAM & BERNER, LLP 1700 DIAGONAL ROAD SUITE 300 ALEXANDRIA, VA 22314 UNITED STATES					
<b>TITLE</b> Liquid crystal display driving device of matrix structure type and its driving method					
<b>FILING FEE RECEIVED</b> 1096	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		

**Search Notes**



<b>Application/Control No.</b>	<b>Applicant(s)/Patent under Reexamination</b>	
10/929,473	SHEN ET AL.	
<b>Examiner</b>	<b>Art Unit</b>	
Vincent E. Kovalick	2629	

SEARCHED			
Class	Subclass	Date	Examiner
345	50	11/28/2007	VEK
	58		
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349	143		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
West Auto Search	3/28/2007	VEK

<b>PATENT APPLICATION FEE DETERMINATION RECORD</b> Substitute for Form PTO-875					Application or Docket Number <b>10/929,473</b>		Filing Date <b>08/31/2004</b>		<input type="checkbox"/> To be Mailed		
<b>APPLICATION AS FILED – PART I</b>					SMALL ENTITY <input checked="" type="checkbox"/>		OR		OTHER THAN SMALL ENTITY		
(Column 1)		(Column 2)									
FOR	NUMBER FILED	NUMBER EXTRA			RATE (\$)	FEE (\$)	OR		RATE (\$)	FEE (\$)	
<input type="checkbox"/> BASIC FEE <small>(37 CFR 1.16(a), (b), or (c))</small>	N/A	N/A			N/A				N/A		
<input type="checkbox"/> SEARCH FEE <small>(37 CFR 1.16(k), (l), or (m))</small>	N/A	N/A			N/A				N/A		
<input type="checkbox"/> EXAMINATION FEE <small>(37 CFR 1.16(o), (p), or (q))</small>	N/A	N/A			N/A				N/A		
TOTAL CLAIMS <small>(37 CFR 1.16(i))</small>	minus 20 =	*			X \$ =				X \$ =		
INDEPENDENT CLAIMS <small>(37 CFR 1.16(h))</small>	minus 3 =	*			X \$ =				X \$ =		
<input type="checkbox"/> APPLICATION SIZE FEE <small>(37 CFR 1.16(s))</small>	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).										
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
* If the difference in column 1 is less than zero, enter "0" in column 2.											
<b>APPLICATION AS AMENDED – PART II</b>					SMALL ENTITY		OR		OTHER THAN SMALL ENTITY		
(Column 1)		(Column 2)		(Column 3)							
<b>AMENDMENT</b>	<b>03/17/2008</b>	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR		RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 7	Minus	** 29	= 0	X \$25 =	0			X \$ =	
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X \$105 =	0			X \$ =	
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))										
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE	<b>0</b>			TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)							
<b>AMENDMENT</b>		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR		RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =				X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =				X \$ =	
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))										
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE				TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.											

Legal Instrument Examiner:  
 /ADRIENE D. SELLMAN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**  
 If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Docket No.: 3079D-0255

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :  
:   
Yu-Ren SHEN *et al.* : Confirmation No. 6164  
:   
U.S. Patent Application No. 10/929,473 : Group Art Unit: 2629  
:   
Filed: August 31, 2004 : Examiner: Vincent E. Kovalick

For: LIQUID CRYSTAL DISPLAY DRIVING DEVICE OF MATRIX STRUCTURE TYP  
AND ITS DRIVING METHOD

**AMENDMENT UNDER 37 C.F.R. 1.111**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In response to the Office Action of December 5, 2007, please amend the above-identified application as follows:

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A liquid crystal display driving device of matrix structure type including:
  - a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that  $N \times M$  of pixels can be driven;
  - a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row... and the  $N^{\text{th}}$  gate line is connected with the gates of all the thin film transistors of the  $N^{\text{th}}$  row; and
  - M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second data lines of the first group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column... and the first and the second data lines of the  $M^{\text{th}}$  group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the  $M^{\text{th}}$  column, and the first data lines and the second data lines of each group of data lines are connected with the same source driver.
2. (Cancelled)
3. (Currently Amended) The liquid crystal display device of matrix structure type ~~as claimed~~

in claim 1, including:

a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that  $N \times M$  of pixels can be driven;

a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row... and the  $N^{\text{th}}$  gate line is connected with the gates of all the thin film transistors of the  $N^{\text{th}}$  row; and

M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second data lines of the first group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column... and the first and the second data lines of the  $M^{\text{th}}$  group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the  $M^{\text{th}}$  column, wherein the first data lines and the second data lines of each group of data lines are connected with the same source driver, each source driver is installed on the same side of the display panel and the data transfer is switched by an electronic switch.

4. (Currently Amended) The liquid crystal display driving device of matrix structure type as claimed in claim [[1]]3, wherein there is a space between the neighboring data lines to prevent them from short circuit.
5. (Currently Amended) The liquid crystal display driving device of matrix structure type as claimed in claim [[1]]3, wherein the gate driver is a chip installed on glass.
6. (Currently Amended) The liquid crystal display driving device of matrix structure type as claimed in claim [[1]]3, wherein the gate driver is an integrated gate driver circuit installed on glass.

7. (Currently Amended) A driving method for the liquid crystal display of matrix structure type including:
- a. making use of the liquid crystal display driving device as claimed in claim [[1]]3, wherein there are  $2(m+n)$ , i.e.  $N=2(m+n)$ , gate lines in the liquid crystal display, the period of the predetermined voltage of over drive received by the thin film transistor connected with the first gate line is set as a over exciting period, and the period of the data voltage of the present frame interval received by the thin film transistor connected with the first gate line is set as a brightness keeping period;
  - b. when the over exciting period begins, the first gate line and the  $2n^{\text{th}}$  gate line are simultaneously turned on, the predetermined voltage of the over drive for the frame is given to the thin film transistor connected with the first gate line, the data voltage of the preceding frame is given to the thin film transistor connected with the  $2n^{\text{th}}$  gate line, and the second and the  $(2n+1)^{\text{th}}$  gate lines, the third and the  $(2n+2)^{\text{th}}$  gate lines... and the  $(2m-1)^{\text{th}}$  and the  $[2(n+m)-2]^{\text{th}}$  gate lines are orderly and simultaneously turned on, the predetermined voltage is given to the thin film transistors connected with the second to the  $(2m-1)^{\text{th}}$  gate lines, the data voltage of the preceding frame is given to the thin film transistors connected with the  $(2n+1)^{\text{th}}$  to the  $[2(m+n)-2]^{\text{th}}$  gate lines;
  - c. when the brightness keeping period begins, the  $2m^{\text{th}}$  and the first gate lines are simultaneously turned on, the predetermined voltage is given to the thin film transistors connected with the  $2m^{\text{th}}$  gate line, the data voltage of the preceding frame interval is given to the thin film transistors connected with the first gate line, and the  $(2m+1)^{\text{th}}$  and the second gate lines, the  $(2m+2)^{\text{th}}$  and the third gate lines... and the  $[2(m+n)]^{\text{th}}$  (the last) and the  $(2n-1)^{\text{th}}$  gate lines are orderly and simultaneously turned on, the predetermined voltage is given to the thin film transistors connected with the  $(2m+1)^{\text{th}}$  to the  $[2(m+n)]^{\text{th}}$  (the last) gate lines, the data voltage of the present frame interval is given to the thin film transistors connected with the second and the  $(2n-1)^{\text{th}}$  gate lines;

by using of the steps stated above, the response speed of the liquid crystal display can be increased.

8. (Original) The driving method for liquid crystal display of matrix structure type as claimed in claim 7, wherein the driving method suits for the active matrix type liquid crystal display, the organic light emitting diode (OLED) display or plasma display panel (PDP).

Claims 9-56 (Cancelled)

REMARKS

Claims 9-56 have been cancelled without prejudice. Applicant reserves the right to file divisional applications to prosecute those claims. Applicant has also cancelled claim 2.

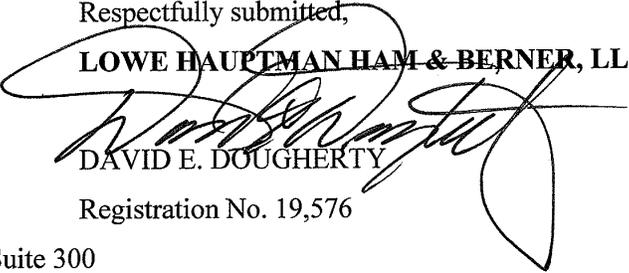
Applicant has rewritten claim 1 to include and the first data lines and the second data lines of each group of data lines are connected with the same source driver. This limitation was taken from original claim 3 and distinguishes amended claim 1 over the cited art. Further, claims 3-8 are now dependent on amended claim 3 as rewritten in independent form and are therefore patentability distinguished over the cited art and should be allowed.

Since all of the claims are now in proper form and clearly and patentably distinguished over the cited art, prompt favorable action is requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

**LOWE HAUPTMAN HAM & BERNER, LLP**

  
DAVID E. DOUGHERTY

Registration No. 19,576

1700 Diagonal Road, Suite 300

Alexandria, Virginia 22314

(703) 684-1111

(703) 518-5499 Facsimile

**Date: March 5, 2008**

**DED/eem**

Docket No.: 3079D-0255

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of :  
Yu-Ren SHEN : Confirmation No. 6164  
Application No. 10/929,473 : Group Art Unit: 2629  
Filed: August 31, 2004 : Examiner:  
Vincent E. KOVALICK :

For: LIQUID CRYSTAL DISPLAY DRIVING DEVICE OF MATRIX STRUCTURE TYP  
AND ITS DRIVING METHOD

**PETITION FOR EXTENSION OF TIME**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Applicant(s) hereby petition(s) the Commissioner of Patents and Trademarks to extend the time for response to the Official Action dated December 5, 2008 for 1 month from March 5, 2008 to April 5, 2008.

A credit card authorization form to cover the cost of the extension is attached. Any deficiency or overpayment should be charged or credited to Deposit Account No.: 07-1337.

Respectfully submitted,

**LOWE HAUPTMAN HAM & BERNER, LLP**

/David E. Dougherty/

DAVID E. DOUGHERTY  
Registration No. 19,576

1700 Diagonal Road, Suite 300  
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Facsimile: (703) 518-5499  
**DATE: March 18, 2008**

## Electronic Patent Application Fee Transmittal

<b>Application Number:</b>	10929473			
<b>Filing Date:</b>	31-Aug-2004			
<b>Title of Invention:</b>	Liquid crystal display driving device of matrix structure type and its driving method			
First Named Inventor/Applicant Name:	Yuh-Ren Shen			
<b>Filer:</b>	David E Dougherty/Beth Murphy			
<b>Attorney Docket Number:</b>	3079/255			
Filed as Small Entity				
<b>Utility Filing Fees</b>				
<b>Description</b>	<b>Fee Code</b>	<b>Quantity</b>	<b>Amount</b>	<b>Sub-Total in USD(\$)</b>
<b>Basic Filing:</b>				
<b>Pages:</b>				
<b>Claims:</b>				
<b>Miscellaneous-Filing:</b>				
<b>Petition:</b>				
<b>Patent-Appeals-and-Interference:</b>				
Post-Allowance-and-Post-Issuance:				
<b>Extension-of-Time:</b>				
Extension - 1 month with \$0 paid	2251	1	60	60

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Miscellaneous:</b>				
<b>Total in USD (\$)</b>				<b>60</b>

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	3014367
<b>Application Number:</b>	10929473
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	6164
<b>Title of Invention:</b>	Liquid crystal display driving device of matrix structure type and its driving method
<b>First Named Inventor/Applicant Name:</b>	Yuh-Ren Shen
<b>Customer Number:</b>	22429
<b>Filer:</b>	David E Dougherty/Beth Murphy
<b>Filer Authorized By:</b>	David E Dougherty
<b>Attorney Docket Number:</b>	3079/255
<b>Receipt Date:</b>	18-MAR-2008
<b>Filing Date:</b>	31-AUG-2004
<b>Time Stamp:</b>	11:53:11
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$60
RAM confirmation Number	6958
Deposit Account	
Authorized User	

### File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
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1		AmendmentToNonFinal.pdf	288969	yes	7
			54e46d31fefbad340eaf37eb92f276b13d7799fa		
<b>Multipart Description/PDF files in .zip description</b>					
		<b>Document Description</b>	<b>Start</b>	<b>End</b>	
		Amendment - After Non-Final Rejection	1	6	
		Extension of Time	7	7	
<b>Warnings:</b>					
<b>Information:</b>					
2	Fee Worksheet (PTO-06)	fee-info.pdf	8183	no	2
			d2f4f96de173a2e293856532bc4549fed53dbc18		
<b>Warnings:</b>					
<b>Information:</b>					
<b>Total Files Size (in bytes):</b>			297152		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b>  If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b>  If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b>  If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



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NOTICE OF ALLOWANCE AND FEE(S) DUE

22429 7590 05/16/2008

LOWE HAUPTMAN HAM & BERNER, LLP
1700 DIAGONAL ROAD
SUITE 300
ALEXANDRIA, VA 22314

EXAMINER

KOVALICK, VINCENT E

ART UNIT PAPER NUMBER

2629

DATE MAILED: 05/16/2008

Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
10/929,473 08/31/2004 Yuh-Ren Shen 3079/255 6164

TITLE OF INVENTION: LIQUID CRYSTAL DISPLAY DRIVING DEVICE OF MATRIX STRUCTURE TYPE AND ITS DRIVING METHOD

Table with 7 columns: APPLN. TYPE, SMALL ENTITY, ISSUE FEE DUE, PUBLICATION FEE DUE, PREV. PAID ISSUE FEE, TOTAL FEE(S) DUE, DATE DUE
nonprovisional YES \$720 \$300 \$0 \$1020 08/18/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

**PART B - FEE(S) TRANSMITTAL**

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE  
 Commissioner for Patents  
 P.O. Box 1450  
 Alexandria, Virginia 22313-1450  
 or Fax (571)-273-2885**

**INSTRUCTIONS:** This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

22429                      7590                      05/16/2008

**LOWE HAUPTMAN HAM & BERNER, LLP**  
 1700 DIAGONAL ROAD  
 SUITE 300  
 ALEXANDRIA, VA 22314

**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/929,473	08/31/2004	Yuh-Ren Shen	3079/255	6164

TITLE OF INVENTION: LIQUID CRYSTAL DISPLAY DRIVING DEVICE OF MATRIX STRUCTURE TYPE AND ITS DRIVING METHOD

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$720	\$300	\$0	\$1020	08/18/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
KOVALICK, VINCENT E	2629	345-204000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.563). <input type="checkbox"/> Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. <input type="checkbox"/> "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. <b>Use of a Customer Number is required.</b>	2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, _____ 1 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. _____ 2 _____ 3
--	--

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE \_\_\_\_\_ (B) RESIDENCE: (CITY and STATE OR COUNTRY) \_\_\_\_\_

Please check the appropriate assignee category or categories (will not be printed on the patent) :  Individual  Corporation or other private group entity  Government

4a. The following fee(s) are submitted: <input type="checkbox"/> Issue Fee <input type="checkbox"/> Publication Fee (No small entity discount permitted) <input type="checkbox"/> Advance Order - # of Copies _____	4b. Payment of Fee(s): ( <b>Please first reapply any previously paid issue fee shown above</b> ) <input type="checkbox"/> A check is enclosed. <input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached. <input type="checkbox"/> The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).
--	--

5. **Change in Entity Status** (from status indicated above)

a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.  b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature \_\_\_\_\_ Date \_\_\_\_\_  
 Typed or printed name \_\_\_\_\_ Registration No. \_\_\_\_\_

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO. Includes application numbers 10/929,473 and 22429, filing dates 08/31/2004 and 05/16/2008, inventor Yuh-Ren Shen, attorney docket number 3079/255, and confirmation number 6164. Also includes examiner KOVALICK, VINCENT E, art unit 2629, and date mailed: 05/16/2008.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 677 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 677 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

<b>Notice of Allowability</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/929,473	SHEN ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	VINCE E. KOVALICK	2629	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1.  This communication is responsive to Applicant's amendment dated 3/18/08.
2.  The allowed claim(s) is/are 1 and 3-8 (re-numbered 1-7).
3.  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a)  All    b)  Some\*    c)  None    of the:
    1.  Certified copies of the priority documents have been received.
    2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3.  Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4.  A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5.  CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
  - (a)  including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
    - 1)  hereto or 2)  to Paper No./Mail Date \_\_\_\_\_.
  - (b)  including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.

**Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6.  DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

- |  |  |
|--|--|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892)   | 5. <input type="checkbox"/> Notice of Informal Patent Application                      |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 6. <input type="checkbox"/> Interview Summary (PTO-413),<br>Paper No./Mail Date _____. |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08),<br>Paper No./Mail Date _____    | 7. <input type="checkbox"/> Examiner's Amendment/Comment                               |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit<br>of Biological Material | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance   |
|  | 9. <input type="checkbox"/> Other _____.   |

**DETAILED ACTION**

***Response to Amendment***

1. This Office Action is in response to Applicant's Amendment, dated March 18, 2008, in response to USPTO Office Action dated December 5, 2007.

The cancellation of claims 2 and 9-56 and the amendments to claims 1, and 3-7 are sufficient to place the application in a condition for allowance as set forth hereinbelow.

***Allowable Subject Matter***

2. Claims 1 and 3-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claims 1 and 3, the major difference between the teachings of the prior art of record (USP 5,805,128, Kim et al.; USP 6,157,056, Takeuchi et al. and (Pub. No. 2004/0056331), Chen et al.) and that of the instant invention is that said prior art of record **does not teach** a liquid crystal display driving device of matrix structure type including M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second data lines of the first group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column..., and the first and the second data lines of the M<sup>th</sup> group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M<sup>th</sup> column, and the first data lines and the second data lines of each group of data lines are connected with the same source driver, each source driver is installed on the same side of the display panel and the data transfer is switched by an electronic switch.

Art Unit: 2629

Regarding claim 7, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a driving method for the liquid crystal display of matrix structure type including: a) making use of the liquid crystal display driving device wherein there are  $2(m+n)$ , i.e.  $N=2(m+n)$ , gate lines in the liquid crystal display, the period of the predetermined voltage of over drive received by the thin film transistor connected with the first gate line is set as a over exciting period, and the period of the data voltage of the present frame interval received by the thin film transistor connected with the first gate line is set as a brightness keeping period; b) when the over exciting period begins, the first gate line and the  $2n$ th gate line are simultaneously turned on, the predetermined voltage of the over drive for the frame is given to the thin film transistor connected with the first gate line, the data voltage of the preceding frame is given to the thin film transistor connected with the  $2n$ th gate line, and the second and the  $(2n+1)$ th gate lines, the third and the  $(2n+2)$ th gate lines..., and the  $(2m-1)$ th and the  $[2(m+n)-2]$ th gate lines are orderly and simultaneously turned on, the predetermined voltage is given to the thin film transistors connected with the second to the  $(2m-1)$ th gate lines, the data voltage of the preceding frame is given to the thin film transistors connected with the  $(2n+1)$ th to the  $[2(m+n)-2]$ th gate lines; c) when the brightness keeping period begins, the  $2m$ th and the first gate lines are Simultaneously turned on, the predetermined voltage is given to the thin film transistors connected with the  $2m$ th gate line, the data voltage of the preceding frame interval is given to the thin film transistors connected with the first gate line, and the  $(2m+1)$ th and the second gate lines, the  $(2m+2)$ th and the third gate lines..., and the  $[2(m+n)]$ th (the last) and the  $(2n-1)$ th gate lines are orderly and simultaneously turned on, the predetermined voltage is given to the thin film transistors connected with the  $(2m+J)$ th to the  $[2(m+n)]$ th (the last) gate lines, the data voltage of the present frame interval is given to the thin film transistors connected with the second and the  $(2n-1)$ th gate lines.

### **Conclusion**

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No. 6,310,594 Libsch et al.

U. S Patent No. 6,057,904 Kim et al.

***To Respond***

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINCE E. KOVALICK whose telephone number is (571)272-7669. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vincent E Kovalick/  
Examiner, Art Unit 2629  
May 12, 2008

/Bipin Shalwala/

Supervisory Patent Examiner, Art Unit 2629

<b>Search Notes</b>  	<b>Application/Control No.</b> 10929473	<b>Applicant(s)/Patent Under Reexamination</b> SHEN ET AL.
	<b>Examiner</b> VINCE E KOVALICK	<b>Art Unit</b> 2629

SEARCHED			
Class	Subclass	Date	Examiner
345	50, 58, 90, 93, 95, 98, 103, 204and 214	11/28/2070	VEK
349	143	11/28/2007	VEK

SEARCH NOTES		
Search Notes	Date	Examiner
West	11/28/2007	VEK

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
same as above		11/28/2007	VEK


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**BIB DATA SHEET**
**CONFIRMATION NO. 6164**

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.	
10/929,473	08/31/2004	349	2629	3079/255	
<b>APPLICANTS</b> Yuh-Ren Shen, Tainan, TAIWAN; Cheng-Jung Chen, Chunan Town, TAIWAN; Chun-Chi Chen, Kaohsiung City, TAIWAN;					
<b>** CONTINUING DATA *****</b>					
<b>** FOREIGN APPLICATIONS *****</b>					
<b>** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** ** SMALL ENTITY **</b> 11/01/2004					
Foreign Priority claimed <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No 35 USC 119(a-d) conditions met <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No Verified and /VINCE E KOVALICK/ Acknowledged Examiner's Signature	<input checked="" type="checkbox"/> Met after Allowance VEK Initials	<b>STATE OR COUNTRY</b> TAIWAN	<b>SHEETS DRAWINGS</b> 26	<b>TOTAL CLAIMS</b> 56	<b>INDEPENDENT CLAIMS</b> 7
<b>ADDRESS</b> LOWE HAUPTMAN HAM & BERNER, LLP 1700 DIAGONAL ROAD SUITE 300 ALEXANDRIA, VA 22314 UNITED STATES					
<b>TITLE</b> Liquid crystal display driving device of matrix structure type and its driving method					
<b>FILING FEE RECEIVED</b> 1096	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		



<b>Index of Claims</b>  	<b>Application/Control No.</b> 10929473	<b>Applicant(s)/Patent Under Reexamination</b> SHEN ET AL.
	<b>Examiner</b> VINCE E KOVALICK	<b>Art Unit</b> 2629

✓	<b>Rejected</b>
=	<b>Allowed</b>

-	<b>Cancelled</b>
÷	<b>Restricted</b>

<b>N</b>	<b>Non-Elected</b>
<b>I</b>	<b>Interference</b>

<b>A</b>	<b>Appeal</b>
<b>O</b>	<b>Objected</b>

Claims renumbered in the same order as presented by applicant
  CPA
  T.D.
  R.1.47

CLAIM		DATE								
Final	Original	05/12/2008								
1	1	=								
	2									
2	3	=								
3	4	=								
4	5	=								
5	6	=								
6	7	=								
7	8	=								



## Electronic Patent Application Fee Transmittal

<b>Application Number:</b>	10929473			
<b>Filing Date:</b>	31-Aug-2004			
<b>Title of Invention:</b>	LIQUID CRYSTAL DISPLAY DRIVING DEVICE OF MATRIX STRUCTURE TYPE AND ITS DRIVING METHOD			
First Named Inventor/Applicant Name:	Yuh-Ren Shen			
<b>Filer:</b>	David E Dougherty/Beth Murphy			
<b>Attorney Docket Number:</b>	3079/255			
Filed as Small Entity				
<b>Utility Filing Fees</b>				
<b>Description</b>	<b>Fee Code</b>	<b>Quantity</b>	<b>Amount</b>	<b>Sub-Total in USD(\$)</b>
<b>Basic Filing:</b>				
<b>Pages:</b>				
<b>Claims:</b>				
<b>Miscellaneous-Filing:</b>				
<b>Petition:</b>				
<b>Patent-Appeals-and-Interference:</b>				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	2501	1	720	720
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Extension-of-Time:</b>				
<b>Miscellaneous:</b>				
<b>Total in USD (\$)</b>				<b>1020</b>

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	3696741
<b>Application Number:</b>	10929473
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	6164
<b>Title of Invention:</b>	LIQUID CRYSTAL DISPLAY DRIVING DEVICE OF MATRIX STRUCTURE TYPE AND ITS DRIVING METHOD
<b>First Named Inventor/Applicant Name:</b>	Yuh-Ren Shen
<b>Customer Number:</b>	22429
<b>Filer:</b>	David E Dougherty/Beth Murphy
<b>Filer Authorized By:</b>	David E Dougherty
<b>Attorney Docket Number:</b>	3079/255
<b>Receipt Date:</b>	29-JUL-2008
<b>Filing Date:</b>	31-AUG-2004
<b>Time Stamp:</b>	17:49:11
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 1020
RAM confirmation Number	3062
Deposit Account	
Authorized User	

### File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Issue Fee Payment (PTO-85B)	PTOL85B.pdf	95906 e2d863887ceb667bc7d172970630d65 d7bed0571	no	1
<b>Warnings:</b>					
<b>Information:</b>					
2	Fee Worksheet (PTO-06)	fee-info.pdf	8330 2622c31ae6160997ea16930c6256719 31fa048fa	no	2
<b>Warnings:</b>					
<b>Information:</b>					
<b>Total Files Size (in bytes):</b>				104236	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b>  If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b>  If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b>  If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



UNITED STATES PATENT AND TRADEMARK OFFICE

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www.uspto.gov

Table with 5 columns: APPLICATION NO., ISSUE DATE, PATENT NO., ATTORNEY DOCKET NO., CONFIRMATION NO.
10/929,473 09/02/2008 7420550 3079/255 6164

22429 7590 08/13/2008
LOWE HAUPTMAN HAM & BERNER, LLP
1700 DIAGONAL ROAD
SUITE 300
ALEXANDRIA, VA 22314

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 677 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Yuh-Ren Shen, Tainan, TAIWAN;
Cheng-Jung Chen, Chunan Town, TAIWAN;
Chun-Chi Chen, Kaohsiung City, TAIWAN;

**PATENT ASSIGNMENT COVER SHEET**

Electronic Version v1.1  
 Stylesheet Version v1.2

EPAS ID: PAT2735870

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
VASTVIEW TECHNOLOGY INC.	12/24/2013
RECEIVING PARTY DATA	
Name:	ADVANCED IP INNOVATIONS LIMITED
Street Address:	TMF CHAMBERS
Internal Address:	PO BOX 3296
City:	APIA
State/Country:	SAMOA
PROPERTY NUMBERS Total: 2	
Property Type	Number
Patent Number:	7202843
Patent Number:	7420550
CORRESPONDENCE DATA	
Fax Number:	
Email:	kjones@techknowledgelaw.com
<i>Correspondence will be sent via US Mail when the email attempt is unsuccessful.</i>	
Correspondent Name:	KEVIN JONES
Address Line 1:	1521 DIAMOND STREET
Address Line 4:	SAN FRANCISCO, CALIFORNIA 94131
NAME OF SUBMITTER:	KEVIN JONES
Signature:	/Kevin Jones/
Date:	02/21/2014
	This document serves as an Oath/Declaration (37 CFR 1.63).
Total Attachments: 3 source=Assignment 1#page1.tif source=Assignment 1#page2.tif source=Assignment 1#page3.tif	

## PATENT ASSIGNMENT

WHEREAS, VastView Technology Inc., a Taiwan corporation, having its principal place of business at 6F.-3, No.65, Gaotie 7th Rd., Zhubei City, Hsinchu County 302, Taiwan R.O.C (hereinafter "Assignor") is the sole and exclusive owner of the entire right, title and interest in and to certain United States patents identified in Schedule A attached hereto, and in and to the inventions disclosed therein; and

WHEREAS, Advanced IP Innovations Limited, a Somoa corporation, having its registered office at TMF Chambers, P.O. Box 3296, Apia, Somoa (hereinafter "Assignee") is desirous of acquiring all right, title and interest in and to said patents identified in Schedule A hereto, and to the inventions disclosed therein;

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, be it known that Assignor has sold, conveyed, assigned and transferred, and does hereby sell, convey, assign, transfer and set over unto Assignee, the entire right, title and interest in and to: (i) the patents listed in Schedule A attached hereto and all the inventions claimed in such patents; (ii) any and all inventions and improvements that are disclosed in the patents listed in Schedule A, together with all pending applications and all provisional applications, divisional applications, continuation applications, continued prosecution applications, continuation-in-part applications, substitute applications, renewal applications, reissue applications, reexaminations, extensions, and all other patent applications that have been or shall be filed in the United States and all foreign countries on any of said inventions or improvements, or claiming priority to or relying on the disclosure of any of the patents listed in Schedule A; (iii) all original patents, reissued patents, reexamination certificates, and extensions, that have been or shall be issued in the United States and all foreign countries on said inventions, improvements and/or patent applications; and (iv) all rights of priority resulting from the filing of said patents and/or patent applications ((i) – (iv) collectively, the "Patents").

Said sale, conveyance, assignment and transfer includes, without limitation, all rights to enforce, assert and sue for past, present and future infringement of the Patents, and all rights to recover and collect for past, present and future damages related to the Patents.

Assignor hereby authorizes and requests the competent authorities to grant and to issue any and all such Patents in the United States and throughout the world to the Assignee and the entire right, title and interest therein, as fully and entirely as the same would have been held and enjoyed by Assignor had this assignment not been made.

Assignor agrees, at any time, upon the request of the Assignee, to execute and to deliver to the Assignee any additional applications for patents for said inventions and discoveries, or any part or parts thereof, and any applications for patents of confirmation, registration and importation based on any of the Patents issuing on said inventions, discoveries, or applications and divisions, continuations, renewals, revivals, reissues, reexaminations and extensions thereof.

Assignor further agrees at any time to cooperate with Assignee, and to execute and to deliver upon request of the Assignee such additional documents, if any, as are necessary or desirable, in

the prosecution of the Patents, and to secure patent protection on said inventions, discoveries and applications throughout all countries of the world, and otherwise to do such acts as are necessary to give full effect to and to perfect the rights of the Assignee under this Assignment, including the execution, delivery and procurement of any and all further documents evidencing this assignment, transfer and sale as may be necessary or desirable.

Assignor hereby covenants that at the time of execution of this assignment, it was the sole and exclusive owner of the entire right, title and interest in and to the Patents, and that no assignment, sale, agreement or encumbrance has been or will be made or entered into which conflicts or would conflict with this assignment.

IN WITNESS WHEREOF, Assignor has caused this Patent Assignment to be signed on its behalf on this 24th day of December, 2013.

VastView Technology Inc.

By: 梁育正  
(Signature)

梁育正  
(Print or type name)

CEO  
(Print or type title)

Schedule A  
Patents

Patent No.	Patent Title	Country
US7202843	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD	US
TWI230291		TW
JP4199655		JP
CN100353409		CN
US7420550	Liquid crystal display driving device of matrix structure type and its driving method	US
TWI267819		TW

**PATENT ASSIGNMENT COVER SHEET**

Electronic Version v1.1  
 Stylesheet Version v1.2

EPAS ID: PAT2735872

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
ADVANCED IP INNOVATIONS LIMITED	02/11/2014
RECEIVING PARTY DATA	
Name:	SURPASS TECH INNOVATION LLC
Street Address:	3422 OLD CAPITOL TRAIL, SUITE 700
City:	WILMINGTON
State/Country:	DELAWARE
Postal Code:	19808-6192
PROPERTY NUMBERS Total: 2	
Property Type	Number
Patent Number:	7420550
Patent Number:	7202843
CORRESPONDENCE DATA	
Fax Number:	
Email:	kjones@techknowledgelaw.com
<i>Correspondence will be sent via US Mail when the email attempt is unsuccessful.</i>	
Correspondent Name:	KEVIN JONES
Address Line 1:	1521 DIAMOND STREET
Address Line 4:	SAN FRANCISCO, CALIFORNIA 94131
NAME OF SUBMITTER:	KEVIN JONES
Signature:	/Kevin Jones/
Date:	02/21/2014
This document serves as an Oath/Declaration (37 CFR 1.63).	
Total Attachments: 4 source=assignment 2#page1.tif source=assignment 2#page2.tif source=assignment 2#page3.tif source=assignment 2#page4.tif	

## PATENT ASSIGNMENT

WHEREAS, ADVANCED IP INNOVATIONS LIMITED, a Samoa corporation having its registered office at TMF Chambers, P.O. Box 3269, Apia, Samoa (hereinafter "Assignor") is the sole and exclusive owner of the entire right, title and interest in and to certain United States patents identified in Schedule A attached hereto, and in and to the inventions disclosed therein; and

WHEREAS, SURPASS TECH INNOVATION LLC, a Delaware limited liability company having its registered office at 3422 Old Capitol Trail, Suite 700, Wilmington, Delaware 19808-6192, U.S.A. (hereinafter "Assignee") is desirous of acquiring all right, title and interest in and to said patents identified in Schedule A hereto, and to the inventions disclosed therein;

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, be it known that Assignor has sold, conveyed, assigned and transferred, and does hereby sell, convey, assign, transfer and set over unto Assignee, the entire right, title and interest in and to: (i) the patents listed in Schedule A attached hereto and all the inventions claimed in such patents; (ii) any and all inventions and improvements that are disclosed in the patents listed in Schedule A, together with all pending applications and all provisional applications, divisional applications, continuation applications, continued prosecution applications, continuation-in-part applications, substitute applications, renewal applications, reissue applications, reexaminations, extensions, and all other patent applications that have been or shall be filed in the United States and all foreign countries on any of said inventions or improvements, or claiming priority to or relying on the disclosure of any of the patents listed in Schedule A; (iii) all original patents, reissued patents, reexamination certificates, and extensions, that have been or shall be issued in the United States and all foreign countries on said inventions, improvements and/or patent applications; and (iv) all rights of priority resulting from the filing of said patents and/or patent applications ((i) – (iv) collectively, the "Patents").

Said sale, conveyance, assignment and transfer includes, without limitation, all rights to enforce, assert and sue for past, present and future infringement of the Patents, and all rights to recover and collect for past, present and future damages related to the Patents.

Assignor hereby authorizes and requests the competent authorities to grant and to issue any and all such Patents in the United States and throughout the world to the Assignee and the entire right, title and interest therein, as fully and entirely as the same would have been held and enjoyed by Assignor had this assignment not been made.

Assignor agrees, at any time, upon the request of the Assignee, to execute and to deliver to the Assignee any additional applications for patents for said inventions and discoveries, or any part or parts thereof, and any applications for patents of confirmation, registration and importation based on any of the Patents issuing on said inventions, discoveries, or applications and divisions, continuations, renewals, revivals, reissues, reexaminations and extensions thereof.

Assignor further agrees at any time to cooperate with Assignee, and to execute and to deliver upon request of the Assignee such additional documents, if any, as are necessary or desirable, in the prosecution of the Patents, and to secure patent protection on said inventions, discoveries and applications throughout all countries of the world, and otherwise to do such acts as are necessary to give full effect to and to perfect the rights of the Assignee under this Assignment, including the execution, delivery and procurement of any and all further documents evidencing this assignment, transfer and sale as may be necessary or desirable.

Assignor hereby covenants that at the time of execution of this assignment, it was the sole and exclusive owner of the entire right, title and interest in and to the Patents, and that no assignment, sale, agreement or encumbrance has been or will be made or entered into which conflicts or would conflict with this assignment.

**IN WITNESS WHEREOF**, Assignor has caused this Patent Assignment to be signed on its behalf on February 11, 2014.

**ADVANCED IP INNOVATIONS LIMITED**

By: 沈 毓 仁 2014/02/11  
(Signature)

Shen, Yehren 沈 毓 仁  
(Print or type name)

Director  
(Print or type title)

Schedule A  
Patents

Patent No.	Patent Title	Country
U.S. Patent No. 7,420,550	Liquid Crystal Display Driving Device of Matrix Structure Type and Its Driving Method	U.S.
TWI267819		TW
U.S. Patent No. 7,202,843	Driving Circuit of A Liquid Crystal Display Panel and Related Driving Method	U.S.
TWI230291		TW
JP4199655		JP
CN100353409		CN

4.1.1

AO 120 (Rev. 08/10)

TO: <b>Mail Stop 8</b> <b>Director of the U.S. Patent and Trademark Office</b> P.O. Box 1450 Alexandria, VA 22313-1450	<b>REPORT ON THE                  FILING OR DETERMINATION OF AN                  ACTION REGARDING A PATENT OR                  TRADEMARK</b>
---	--

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the District of Delaware on the following

Trademarks or  Patents. (  the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED 3/14/2014	U.S. DISTRICT COURT for the District of Delaware
PLAINTIFF SURPASS TECH INNOVATION LLC		DEFENDANT SHARP CORPORATION, et al.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,202,843	4/10/2007	SURPASS TECH INNOVATION LLC
2 7,420,550	9/2/2008	SURPASS TECH INNOVATION LLC
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY <input type="checkbox"/> Amendment <input type="checkbox"/> Answer <input type="checkbox"/> Cross Bill <input type="checkbox"/> Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
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CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director  
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy