AO 120 (Rev. 08/10)

TO: **Mail Stop 8** **Director of the U.S. Patent and Trademark Office** **P.O. Box 1450** **Alexandria, VA 22313-1450**	**REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK**

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the District of Delaware on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED 3/14/2014	U.S. DISTRICT COURT for the District of Delaware
PLAINTIFF SURPASS TECH INNOVATION LLC		DEFENDANT LG DISPLAY CO., LTD, et al.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,202,843	4/10/2007	SURPASS TECH INNOVATION LLC
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	**DATE OF PATENT OR TRADEMARK**	**HOLDER OF PATENT OR TRADEMARK**
1		
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3		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO: **Mail Stop 8** **Director of the U.S. Patent and Trademark Office** **P.O. Box 1450** **Alexandria, VA 22313-1450**	**REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK**

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the District of Delaware on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED 3/14/2014	U.S. DISTRICT COURT for the District of Delaware
PLAINTIFF SURPASS TECH INNOVATION LLC		DEFENDANT SAMSUNG DISPLAY CO., LTD, et al.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,202,843	4/10/2007	SURPASS TECH INNOVATION LLC
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	**DATE OF PATENT OR TRADEMARK**	**HOLDER OF PATENT OR TRADEMARK**
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Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	**REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK**

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the District of Delaware on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED 3/14/2014	U.S. DISTRICT COURT for the District of Delaware
PLAINTIFF SURPASS TECH INNOVATION LLC		DEFENDANT SHARP CORPORATION, et al.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,202,843	4/10/2007	SURPASS TECH INNOVATION LLC
2 7,420,550	9/2/2008	SURPASS TECH INNOVATION LLC
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
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5		

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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT2735870

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
VASTVIEW TECHNOLOGY INC.	12/24/2013

RECEIVING PARTY DATA

Name:	ADVANCED IP INNOVATIONS LIMITED
Street Address:	TMF CHAMBERS
Internal Address:	PO BOX 3296
City:	APIA
State/Country:	SAMOA

PROPERTY NUMBERS Total: 2

Property Type	Number
Patent Number:	7202843
Patent Number:	7420550

CORRESPONDENCE DATA

Fax Number:
Email: kjones@techknowledgelaw.com
Correspondence will be sent via US Mail when the email attempt is unsuccessful.
Correspondent Name: KEVIN JONES
Address Line 1: 1521 DIAMOND STREET
Address Line 4: SAN FRANCISCO, CALIFORNIA 94131

NAME OF SUBMITTER:	KEVIN JONES
Signature:	/Kevin Jones/
Date:	02/21/2014
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 3
source=Assignment 1#page1.tif
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PATENT ASSIGNMENT

WHEREAS, VastView Technology Inc., a Taiwan corporation, having its principal place of business at 6F.-3, No.65, Gaotie 7th Rd., Zhubei City, Hsinchu County 302, Taiwan R.O.C (hereinafter "Assignor") is the sole and exclusive owner of the entire right, title and interest in and to certain United States patents identified in Schedule A attached hereto, and in and to the inventions disclosed therein; and

WHEREAS, Advanced IP Innovations Limited, a Somoa corporation, having its registered office at TMF Chambers, P.O. Box 3296, Apia, Somoa (hereinafter "Assignee") is desirous of acquiring all right, title and interest in and to said patents identified in Schedule A hereto, and to the inventions disclosed therein;

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, be it known that Assignor has sold, conveyed, assigned and transferred, and does hereby sell, convey, assign, transfer and set over unto Assignee, the entire right, title and interest in and to: (i) the patents listed in Schedule A attached hereto and all the inventions claimed in such patents; (ii) any and all inventions and improvements that are disclosed in the patents listed in Schedule A, together with all pending applications and all provisional applications, divisional applications, continuation applications, continued prosecution applications, continuation-in-part applications, substitute applications, renewal applications, reissue applications, reexaminations, extensions, and all other patent applications that have been or shall be filed in the United States and all foreign countries on any of said inventions or improvements, or claiming priority to or relying on the disclosure of any of the patents listed in Schedule A; (iii) all original patents, reissued patents, reexamination certificates, and extensions, that have been or shall be issued in the United States and all foreign countries on said inventions, improvements and/or patent applications; and (iv) all rights of priority resulting from the filing of said patents and/or patent applications ((i) – (iv) collectively, the "Patents").

Said sale, conveyance, assignment and transfer includes, without limitation, all rights to enforce, assert and sue for past, present and future infringement of the Patents, and all rights to recover and collect for past, present and future damages related to the Patents.

Assignor hereby authorizes and requests the competent authorities to grant and to issue any and all such Patents in the United States and throughout the world to the Assignee and the entire right, title and interest therein, as fully and entirely as the same would have been held and enjoyed by Assignor had this assignment not been made.

Assignor agrees, at any time, upon the request of the Assignee, to execute and to deliver to the Assignee any additional applications for patents for said inventions and discoveries, or any part or parts thereof, and any applications for patents of confirmation, registration and importation based on any of the Patents issuing on said inventions, discoveries, or applications and divisions, continuations, renewals, revivals, reissues, reexaminations and extensions thereof.

Assignor further agrees at any time to cooperate with Assignee, and to execute and to deliver upon request of the Assignee such additional documents, if any, as are necessary or desirable, in the prosecution of the Patents, and to secure patent protection on said inventions, discoveries and applications throughout all countries of the world, and otherwise to do such acts as are necessary to give full effect to and to perfect the rights of the Assignee under this Assignment, including the execution, delivery and procurement of any and all further documents evidencing this assignment, transfer and sale as may be necessary or desirable.

Assignor hereby covenants that at the time of execution of this assignment, it was the sole and exclusive owner of the entire right, title and interest in and to the Patents, and that no assignment, sale, agreement or encumbrance has been or will be made or entered into which conflicts or would conflict with this assignment.

IN WITNESS WHEREOF, Assignor has caused this Patent Assignment to be signed on its behalf on this 24th day of December, 2013.

VastView Technology Inc.

By: 梁育正
(Signature)

梁育正
(Print or type name)

CEO
(Print or type title)

Schedule A
Patents

Patent No.	Patent Title	Country
US7202843	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD	US
TWI230291		TW
JP4199655		JP
CN100353409		CN
US7420550	Liquid crystal display driving device of matrix structure type and its driving method	US
TWI267819		TW

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT2735872

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
ADVANCED IP INNOVATIONS LIMITED	02/11/2014

RECEIVING PARTY DATA

Name:	SURPASS TECH INNOVATION LLC
Street Address:	3422 OLD CAPITOL TRAIL, SUITE 700
City:	WILMINGTON
State/Country:	DELAWARE
Postal Code:	19808-6192

PROPERTY NUMBERS Total: 2

Property Type	Number
Patent Number:	7420550
Patent Number:	7202843

CORRESPONDENCE DATA

Fax Number:
Email: kjones@techknowledgelaw.com
Correspondence will be sent via US Mail when the email attempt is unsuccessful.
Correspondent Name: KEVIN JONES
Address Line 1: 1521 DIAMOND STREET
Address Line 4: SAN FRANCISCO, CALIFORNIA 94131

NAME OF SUBMITTER:	KEVIN JONES
Signature:	/Kevin Jones/
Date:	02/21/2014
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 4
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source=assignment 2#page2.tif
source=assignment 2#page3.tif
source=assignment 2#page4.tif

PATENT ASSIGNMENT

WHEREAS, ADVANCED IP INNOVATIONS LIMITED, a Samoa corporation having its registered office at TMF Chambers, P.O. Box 3269, Apia, Samoa (hereinafter "Assignor") is the sole and exclusive owner of the entire right, title and interest in and to certain United States patents identified in Schedule A attached hereto, and in and to the inventions disclosed therein; and

WHEREAS, SURPASS TECH INNOVATION LLC, a Delaware limited liability company having its registered office at 3422 Old Capitol Trail, Suite 700, Wilmington, Delaware 19808-6192, U.S.A. (hereinafter "Assignee") is desirous of acquiring all right, title and interest in and to said patents identified in Schedule A hereto, and to the inventions disclosed therein;

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, be it known that Assignor has sold, conveyed, assigned and transferred, and does hereby sell, convey, assign, transfer and set over unto Assignee, the entire right, title and interest in and to: (i) the patents listed in Schedule A attached hereto and all the inventions claimed in such patents; (ii) any and all inventions and improvements that are disclosed in the patents listed in Schedule A, together with all pending applications and all provisional applications, divisional applications, continuation applications, continued prosecution applications, continuation-in-part applications, substitute applications, renewal applications, reissue applications, reexaminations, extensions, and all other patent applications that have been or shall be filed in the United States and all foreign countries on any of said inventions or improvements, or claiming priority to or relying on the disclosure of any of the patents listed in Schedule A; (iii) all original patents, reissued patents, reexamination certificates, and extensions, that have been or shall be issued in the United States and all foreign countries on said inventions, improvements and/or patent applications; and (iv) all rights of priority resulting from the filing of said patents and/or patent applications ((i) – (iv) collectively, the "Patents").

Said sale, conveyance, assignment and transfer includes, without limitation, all rights to enforce, assert and sue for past, present and future infringement of the Patents, and all rights to recover and collect for past, present and future damages related to the Patents.

Assignor hereby authorizes and requests the competent authorities to grant and to issue any and all such Patents in the United States and throughout the world to the Assignee and the entire right, title and interest therein, as fully and entirely as the same would have been held and enjoyed by Assignor had this assignment not been made.

Assignor agrees, at any time, upon the request of the Assignee, to execute and to deliver to the Assignee any additional applications for patents for said inventions and discoveries, or any part or parts thereof, and any applications for patents of confirmation, registration and importation based on any of the Patents issuing on said inventions, discoveries, or applications and divisions, continuations, renewals, revivals, reissues, reexaminations and extensions thereof.

Assignor further agrees at any time to cooperate with Assignee, and to execute and to deliver upon request of the Assignee such additional documents, if any, as are necessary or desirable, in the prosecution of the Patents, and to secure patent protection on said inventions, discoveries and applications throughout all countries of the world, and otherwise to do such acts as are necessary to give full effect to and to perfect the rights of the Assignee under this Assignment, including the execution, delivery and procurement of any and all further documents evidencing this assignment, transfer and sale as may be necessary or desirable.

Assignor hereby covenants that at the time of execution of this assignment, it was the sole and exclusive owner of the entire right, title and interest in and to the Patents, and that no assignment, sale, agreement or encumbrance has been or will be made or entered into which conflicts or would conflict with this assignment.

IN WITNESS WHEREOF, Assignor has caused this Patent Assignment to be signed on its behalf on February 11, 2014.

ADVANCED IP INNOVATIONS LIMITED

By: 沈毓仁 2014/02/11
(Signature)

Shen, Yehren 沈毓仁
(Print or type name)

Director
(Print or type title)

Schedule A
Patents

Patent No.	Patent Title	Country
U.S. Patent No. 7,420,550	Liquid Crystal Display Driving Device of Matrix Structure Type and Its Driving Method	U.S.
TWI267819		TW
U.S. Patent No. 7,202,843	Driving Circuit of A Liquid Crystal Display Panel and Related Driving Method	U.S.
TWI230291		TW
JP4199655		JP
CN100353409		CN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,741	04/10/2007	7202843	VASP0001USA	1740

27765 7590 03/23/2007

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 602 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Yung-Hung Shen, Hsin-Chu City, TAIWAN;
Shih-Chung Wang, Kao-Hsiung City, TAIWAN;
Yuhren Shen, Tai-Nan City, TAIWAN;
Cheng-Jung Chen, Miao- Li Hsien, TAIWAN;

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,741	01/08/2004	Yung-Hung Shen	VASP0001USA	1740

27765 7590 01/17/2007
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
PATEL, NITIN	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
01/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.

EXAMINER

ART UNIT	PAPER

20061028

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

Examiner has initialed IDS (7/20/2004 and considered.

Nitin Patel
Examiner
Art Unit: 2629

PTO-90C (Rev.04-03)

PTO/SB/08A (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/707,741
Filing Date	01/08/2004
First Named Inventor	Yung-Hung Shen
Art Unit	2673
Examiner Name	
Attorney Docket Number	VASP0001USA

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
NP	1	US-2002/0044115A1	04/18/2002	Jinda, Akihito, et al.	—
NP	2	US-2003/0058264A1	03/27/2003	Takako, Adachi, et al.	—
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] -Number[4]- Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
NP	1	EP-1122711A2A3	08/08/2001	Lee, Baek-Woon, et al.	—	+
NP	2	EP-0660297A2A3	06/28/1995	Sawayama, et al.	—	+
NP	3	EP-0539185A1	04/28/1993	Mizukata, et al.	—	+

Examiner Signature	NP	Date Considered	1-3-07

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08B (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/707,741
Filing Date	01/08/2004
First Named Inventor	Yung-Hung Shen
Group Art Unit	2673
Examiner Name	
Attorney Docket Number	VASP0001USA

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
NW	1	Baek-Woon Lee, et al.; Reducing Gray-Level Response to One Frame: Dynamic Capacitance compensation; Samsung Electronics Corp.; ISSN00010966X, 2001	+

Examiner Signature	NW	Date Considered	1-3-07.

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

OIPE IAP6 DEC 2 1 2006 PATENT & TRADEMARK OFFICE

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

027765 7590 10/31/2006

NORTH AMERICA INTELLECTUAL PROPERTY
CORPORATION
P.O.BOX 506
MERRIFIELD, VA 22116

12/21/2006 ADSHAN2 00000001 503105 10707741

01 FC:2501 700.00 DA
02 FC:1504 300.00 DA

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Stephanie Lai (Depositor's name)
Stephanie Lai (Signature)
12/21/2006 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,741	01/08/2004	Yung-Hung Shen	VASP0001USA	1740

TITLE OF INVENTION: DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$300	$0	$1000	01/31/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
PATEL, NITIN	2629	345-087000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 Winston Hsu
2 ____
3 ____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Vastview Technology Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): 4F, No. 5, Technology Rd., Science-Based Industrial Park, Hsin-Chu, Taiwan, R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☑ Issue Fee
☑ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies ____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-3105 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Winston Hsu Date 12/21/2006

Typed or printed name Winston Hsu Registration No. 41,526

NAIP

North America
Intellectual Property corporation

P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
FAX: 806-498-6673
e-mail:winstonhsu@naipo.com

FAX TO: Mail Stop Issue Fee **Fax: (571) 273-2885**

FROM: Winston Hsu, PATENT AGENT, REG. NO.: 41,526

SERIAL NO.: 10/707,741

ATTORNEY DOCKET NO.: VASP0001USA

SUBJECT: ISSUE FEE PAYMENT

TOTAL PAGES: 2 PAGES (INCLUDING COVER PAGE)

Winston Hsu 12/21/2006

VASP0001USA0_E2_1

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NOTICE OF ALLOWANCE AND FEE(S) DUE

027765 7590 10/31/2006

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
PATEL, NITIN	
ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 10/31/2006

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,741	01/08/2004	Yung-Hung Shen	VASP0001USA	1740

TITLE OF INVENTION: DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$300	$0	$1000	01/31/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
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Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

027765 7590 10/31/2006

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,741	01/08/2004	Yung-Hung Shen	VASP0001USA	1740

TITLE OF INVENTION: DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$300	$0	$1000	01/31/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
PATEL, NITIN	2629	345-087000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
   - ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   - ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
   (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
   (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
   1 ____________
   2 ____________
   3 ____________

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies ____________

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number ________ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature ____________ Date ____________

Typed or printed name ____________ Registration No. ____________

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,741	01/08/2004	Yung-Hung Shen	VASP0001USA	1740

027765 7590 10/31/2006

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
PATEL, NITIN	
ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 10/31/2006

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 602 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 602 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

Notice of Allowability	Application No.	Applicant(s)	
	10/707,741	SHEN ET AL.	
	Examiner	**Art Unit**	
	Nitin Patel	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *1/8/2004*.

2. ☒ The allowed claim(s) is/are *1-9*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 7/20/2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Nitin Patel

LGD_000137

REASON FOR ALLOWANCE

1. Claims 1-9 are allowed.

2. The following is an examiner's statement of reason for allowance:

Ham (US 20040196229) shows apply the normal data to the liquid crystal panel at the initial half period of the frame after supplying of the modulated data to the liquid crystal panel during the later half period of the frame, thus a desired brightness level is achieved within the initial period of the frame.

Lee (US 20010038372) shows a driving method for LCD having a data gray signal modifier for receiving gray signal from a data gray signal source, and outputting modification gray signals by consideration of gray signals of present and previous frames; a data driver for changing the modification gray signals into corresponding data voltages and outputting image signals; a gate driver for sequentially supplying scanning signals and an LCD panel having a plurality of gate lines for transmitting the scanning signals; a plurality of data lines being insulted from the gate lines and crossing them for transmitting the image signals and a plurality of pixels formed by an area surrounded by gate lines and data lines and arranged as a matrix pattern.

The prior art fails to teach or suggest a method for driving a liquid crystal display (LCD) panel, the LCD panel comprising: a plurality of scan lines; a plurality of data lines; and a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device, and **the method comprising: receiving continuously a**

plurality of frame data; generating a plurality of data impulses for each pixel within every frame period according to the frame data; and applying the data impulses to the liquid crystal device of one of the pixels within one frame period via the data line connected to the pixel in order to control a transmission rate of the liquid crystal device of the pixel as claimed in claim 1.

The prior art fails to teach or suggest a driving circuit for driving an LCD panel, the LCD panel comprising: a plurality of scan lines; a plurality of data lines; and a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device, the driving circuit comprising: **a blur clear converter for receiving frame data every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel, the blur clear converter delaying current frame data to generate delayed frame data and generating a plurality of overdriven pixel data within every frame period for each pixel; a source driver for generating a plurality of data impulses to each pixel according to the plurality of overdriven pixel data generated by the blur clear converter and applying the data impulses to the liquid crystal device of the pixel via the scan line connected to the pixel within one frame period in order to control transmission rate of the liquid crystal device; and a gate driver for applying a scan line voltage to the switch device of the pixel so that the data impulses can be applied to the liquid crystal device of the pixel** as claimed in claim 7.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 571-272-7677. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin H. Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nitin Patel
Examiner
Art Unit 2629

OIPE JC139 JUL 2 0 2004 PATENT & TRADEMARK OFFICE

PTO/SB/08A (10-01)
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/707,741
Filing Date	01/08/2004
First Named Inventor	Yung-Hung Shen
Art Unit	2673
Examiner Name	
Attorney Docket Number	VASP0001USA

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
MP	1	US-2002/0044115A1	04/18/2002	Jinda, Akihito, et al.	—
MP	2	US-2003/0058264A1	03/27/2003	Takako, Adachi, et al.	—
		US-			
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] -Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
MP	1	EP-1122711A2A3	08/08/2001	Lee, Baek-Woon, et al.		+
MP	2	EP-0660297A2A3	06/28/1995	Sawayama, et al.		+
MP	3	EP-0539185A1	04/28/1993	Mizukata, et al.		+

Examiner Signature	MP.	Date Considered	10-16-06.

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

Notice of References Cited	Application/Control No. 10/707,741	Applicant(s)/Patent Under Reexamination SHEN ET AL.	
	Examiner Nitin Patel	Art Unit 2629	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2004/0119730	06-2004	Ham et al.	345/692
*	B	US-2004/0246224	12-2004	Tsai et al.	345/100
*	C	US-2004/0196229	10-2004	Ham, Yong Sung	345/087
*	D	US-2001/0038372	11-2001	Lee, Baek-Woon	345/89
*	E	US-2005/0073630	04-2005	Chen et al.	349/087
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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Bib Data Sheet

CONFIRMATION NO. 1740

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/707,741	01/08/2004 **RULE**	345	2629	VASP0001USA

APPLICANTS

Yung-Hung Shen, Hsin-Chu City, TAIWAN;
Shih-Chung Wang, Kao-Hsiung City, TAIWAN;
Yuhren Shen, Tai-Nan City, TAIWAN;
Cheng-Jung Chen, Miao- Li Hsien, TAIWAN;

** **CONTINUING DATA** ************************* None

** **FOREIGN APPLICATIONS** ******************** NLL
TAIWAN 092132122 11/17/2003

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** SMALL ENTITY **
** 03/11/2004

Foreign Priority claimed / 35 USC 119 (a-d) conditions met / Verified and Acknowledged	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed ☑ yes ☐ no 35 USC 119 (a-d) conditions met ☑ yes ☐ no ☐ Met after Allowance Verified and Acknowledged NLL Examiner's Signature NLL Initials	TAIWAN	10	9	2

ADDRESS
027765

TITLE

DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD

FILING FEE RECEIVED	FEES	
385	FEES: Authority has been given in Paper No. _________ to charge/credit DEPOSIT ACCOUNT No. _________ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other ______________ ☐ Credit

Issue Classification	Application/Control No. 10/707,741	Applicant(s)/Patent under Reexamination SHEN ET AL.
	Examiner Nitin Patel	Art Unit 2629

ISSUE CLASSIFICATION

ORIGINAL		INTERNATIONAL CLASSIFICATION								
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED			
345	87	G	09	G	3	/36				/
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CROSS REFERENCES				
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)			
345	89			

(Assistant Examiner) (Date)	Nitin Patel (Primary Examiner) (Date)	Total Claims Allowed: 9	
(Legal Instruments Examiner) (Date)		O.G. Print Claim(s): 1	O.G. Print Fig.: 5

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
4	1		31		61		91		121		151		181
5	2		32		62		92		122		152		182
6	3		33		63		93		123		153		183
7	4		34		64		94		124		154		184
8	5		35		65		95		125		155		185
9	6		36		66		96		126		156		186
1	7		37		67		97		127		157		187
2	8		38		68		98		128		158		188
3	9		39		69		99		129		159		189
	10		40		70		100		130		160		190
	11		41		71		101		131		161		191
	12		42		72		102		132		162		192
	13		43		73		103		133		163		193
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	18		48		78		108		138		168		198
	19		49		79		109		139		169		199
	20		50		80		110		140		170		200
	21		51		81		111		141		171		201
	22		52		82		112		142		172		202
	23		53		83		113		143		173		203
	24		54		84		114		144		174		204
	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Search Notes	Application/Control No. 10/707,741	Applicant(s)/Patent under Reexamination SHEN ET AL.	
	Examiner Nitin Patel	Art Unit 2629	

SEARCHED			
Class	Subclass	Date	Examiner
345	87	10/28/2006	NP
	88		
	89		
	90		
	91		
	93		
	98		
	99		
	100		
	204		
	589		
	596		
	600-605		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
Updated	**above**	**10/28/2006**	**NP**
class	subclass		
pgpub	database		

SEARCH NOTES (INCLUDING SEARCH STRATEGY)	DATE	EXMR
EAST SEARCH	10/28/2006	NP

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	89	(plurality near2 data) near4 frame near2 (period or timing or interval or duration)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/28 10:55
S1	0	frame near period with data near impluse	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/28 10:54
S2	72449	frame near (period or tim$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/18 12:35
S3	1694	S2 near3 (pixel or color or colour)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/18 12:36
S4	92	S3 same lcd	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/18 12:36
S5	158	data near3 frame near3 (period or tim$5) same lcd	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/18 13:20
S6	105811	data near3 frame	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/23 14:19
S7	6532	S6 near4 (period or timing or interval or duration)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/23 14:19
S8	109	S7 same lcd	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/23 14:19

EAST Search History

S9	15041	frame near3 data near4 (timing or time or duration or interval)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/25 11:15
S10	145	S9 same lcd	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/25 11:25
S11	4920	convert$5 near4 (frame near3 data)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/25 11:25
S12	517	S11 with (time or interval or duration or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/25 11:26
S13	21	S12 same lcd	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/25 11:27
S14	5	overdrive$5 near pixel near data	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/25 11:28
S15	2474	converter same frame near data	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/25 11:29
S16	90	S15 same lcd	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/25 11:29

Day : Saturday
Date: 10/28/2006

PALM INTRANET

Time: 12:38:42

Inventor Name Search Result

Your Search was:

Last Name = SHEN
First Name = YUNG-HUNG

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10707741	Not Issued	30	01/08/2004	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD	SHEN, YUNG-HUNG
10709506	Not Issued	30	05/11/2004	DRIVING METHOD FOR A LIQUID CRYSTAL DISPLAY	SHEN, YUNG-HUNG

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** SHEN **First Name** YUNG-HUNG Search

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Day : Saturday
Date: 10/28/2006
Time: 12:38:51

PALM INTRANET

Inventor Name Search Result

Your Search was:

Last Name = WANG
First Name = SHIH-CHUNG

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10707741	Not Issued	30	01/08/2004	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD	WANG, SHIH-CHUNG
10904250	Not Issued	30	11/01/2004	METHOD FOR CONTROLLING OPEPRATIONS OF A LIQUID CRYSTAL DISPLAY TO AVOID FLICKERING FRAMES	WANG, SHIH-CHUNG
11456866	Not Issued	25	07/12/2006	APPARATUS AND METHOD FOR TEMPORAL NOISE REDUCTION AND MOTION ENHANCEMENT	WANG, SHIH-CHUNG

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** WANG **First Name** SHIH-CHUNG Search

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Day : Saturday
Date: 10/28/2006

PALM INTRANET

Time: 12:38:57

Inventor Name Search Result

Your Search was:

Last Name = SHEN
First Name = YUHREN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09826097	6680755	150	04/05/2001	ADJUSTABLE BIASED GAMMA-CORRECTION CIRCUIT WITH CENTRAL-SYMMETRY VOLTAGE	SHEN, YUHREN
09842817	6778161	150	04/27/2001	CENTRAL SYMMETRIC GAMMA VOLTAGE CORRECTION CIRCUIT	SHEN, YUHREN
09940289	6750834	150	08/27/2001	MODIFICATION OF THE V-T CURVE OF AN LCD BY CHANGING THE WAVEFORM OF COMMON VOLTAGE	SHEN, YUHREN
10707362	Not Issued	61	12/09/2003	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF	SHEN, YUHREN
10707384	Not Issued	93	12/09/2003	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY AND RELATING DRIVING METHOD	SHEN, YUHREN
10707741	Not Issued	30	01/08/2004	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD	SHEN, YUHREN
10799046	Not Issued	93	03/11/2004	METHOD FOR DRIVING LCD DEVICE	SHEN, YUHREN

Inventor Search Completed: No Records to Display.

Search Another: Inventor Last Name: SHEN First Name: YUHREN [Search]

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Day : Saturday
Date: 10/28/2006

PALM INTRANET

Time: 12:39:02

Inventor Name Search Result

Your Search was:

Last Name = CHEN
First Name = CHENG-JUNG

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09026439	5901587	250	02/19/1998	PADLOCK WITH SAFETY LOCKING MECHANISM	CHEN, CHENG-JUNG
10646844	Not Issued	83	08/25/2003	High-quality-image liquid crystal display device and the driving method thereof	CHEN, CHENG-JUNG
10707362	Not Issued	61	12/09/2003	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF	CHEN, CHENG-JUNG
10707384	Not Issued	93	12/09/2003	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY AND RELATING DRIVING METHOD	CHEN, CHENG-JUNG
10707741	Not Issued	30	01/08/2004	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD	CHEN, CHENG-JUNG
10709506	Not Issued	30	05/11/2004	DRIVING METHOD FOR A LIQUID CRYSTAL DISPLAY	CHEN, CHENG-JUNG
10772930	Not Issued	30	02/04/2004	Device and method of dynamic driving for liquid crystal display	CHEN, CHENG-JUNG
10810621	Not Issued	30	03/29/2004	Method for luminance compensation of liquid crystal display and its device	CHEN, CHENG-JUNG
10841033	Not Issued	25	08/30/2004	Method and device for driving liquid crystal display	CHEN, CHENG-JUNG
10850172	Not Issued	30	05/19/2004	Method and device used for simulating CRT impulse type image display	CHEN, CHENG-JUNG
10862516	Not Issued	30	06/05/2004	Method and device used for eliminating image overlap blurring phenomenon between frames in process of simulating	CHEN, CHENG-JUNG

				CRT impulse type image display	
10866026	Not Issued	30	06/14/2004	Method of fast gray-scale converting of LCD	CHEN, CHENG-JUNG
10866028	Not Issued	30	06/14/2004	Method of increasing image gray-scale response speed	CHEN, CHENG-JUNG
10889265	Not Issued	30	07/10/2004	Driving method for LCD panel	CHEN, CHENG-JUNG
10929473	Not Issued	30	08/31/2004	Liquid crystal display driving device of matrix structure type and its driving method	CHEN, CHENG-JUNG
10965808	Not Issued	30	10/18/2004	Color display system	CHEN, CHENG-JUNG
10965863	Not Issued	30	03/07/2005	Method of signal processing	CHEN, CHENG-JUNG
10965946	Not Issued	30	10/14/2004	Liquid crystal screen display method	CHEN, CHENG-JUNG
10989264	Not Issued	30	11/17/2004	Driving system of a display panel	CHEN, CHENG-JUNG
29083561	D407294	150	02/13/1998	COMBINATION LOCK	CHEN, CHENG-JUNG

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** CHEN **First Name** CHENG-JUNG Search

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TRANSMITTAL FORM *(to be used for all correspondence after initial filing)*		
	Application Number	10/707,741
	Filing Date	01/08/2004
	First Named Inventor	Yung-Hung Shen
	Art Unit	2673
	Examiner Name	
Total Number of Pages in This Submission: 113	Attorney Docket Number	VASP0001USA

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [x] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) ____________
- [ ] After Allowance communication to Technology Center (TC)
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) (please Identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Winston Hsu, Reg. No.: 41,526
Signature	Winston Hsu
Date	JUN 19 2004

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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☑ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 0.00

Complete if Known	
Application Number	10/707,741
Filing Date	01/08/2004
First Named Inventor	Yung-Hung Shen
Examiner Name	
Art Unit	2673
Attorney Docket No.	VASP0001USA

METHOD OF PAYMENT *(check all that apply)*

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☑ Deposit Account:

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Deposit Account Name	North America Intellectual Property Corp.

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1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X		=	
Independent Claims		- 3** =		X		=	
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) ________________

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 0.00

SUBMITTED BY				(Complete *(if applicable)*)	
Name *(Print/Type)*	Winston Hsu	Registration No. *(Attorney/Agent)*	41,526	Telephone	886289237350
Signature	Winston Hsu			Date	JUN 19 2004

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 1

Complete if Known	
Application Number	10/707,741
Filing Date	01/08/2004
First Named Inventor	Yung-Hung Shen
Art Unit	2673
Examiner Name	
Attorney Docket Number	VASP0001USA

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US-2002/0044115A1	04/18/2002	Jinda, Akihito, et al.	
	2	US-2003/0058264A1	03/27/2003	Takako, Adachi, et al.	
		US-			
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] -Number[4]- Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	1	EP-1122711A2A3	08/08/2001	Lee, Baek-Woon, et al.		+
	2	EP-0660297A2A3	06/28/1995	Sawayama, et al.		+
	3	EP-0539185A1	04/28/1993	Mizukata, et al.		+

Examiner Signature		Date Considered	

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Complete if Known	
Application Number	10/707,741
Filing Date	01/08/2004
First Named Inventor	Yung-Hung Shen
Group Art Unit	2673
Examiner Name	
Attorney Docket Number	VASP0001USA

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	Baek-Woon Lee, et al.; Reducing Gray-Level Response to One Frame: Dynamic Capacitance compensation; Samsung Electronics Corp.; ISSN00010966X, 2001	+

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

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(19) Europäisches Patentamt
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Office européen des brevets

(11) EP 1 122 711 A2

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
08.08.2001 Bulletin 2001/32

(51) Int Cl.[7]: **G09G 3/36**

(21) Application number: **01102227.4**

(22) Date of filing: **31.01.2001**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **03.02.2000 KR 2000005442**
27.07.2000 KR 2000043509
06.12.2000 KR 2000073672

(71) Applicant: **Samsung Electronics Co., Ltd.**
Suwon-city, Kyungki-do (KR)

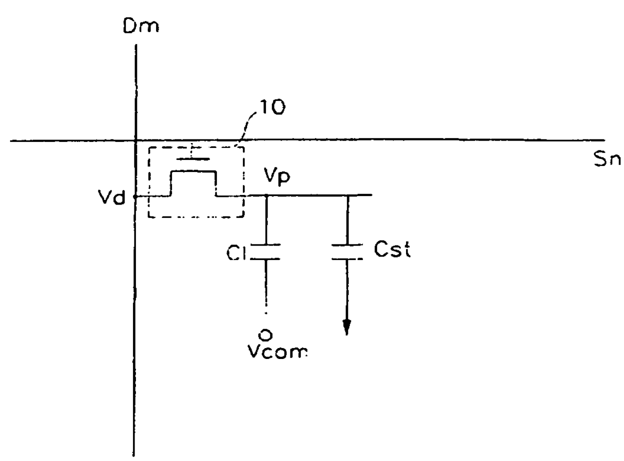
(72) Inventor: **Lee, Baek-Woon**
Yongin-city, Kyungki-do (KR)

(74) Representative: **Modiano, Guido, Dr.-Ing. et al**
Modiano, Josif, Pisanty & Staub,
Baaderstrasse 3
80469 München (DE)

(54) **Liquid crystal display and driving method thereof**

(57) Disclosed is an LCD and driving method thereof. The present invention comprises a data gray signal modifier for receiving gray signals from a data gray signal source, and outputting modification gray signals by consideration of gray signals of present and previous frames; a data driver for changing the modification gray signals into corresponding data voltages and outputting image signals; a gate driver for sequentially supplying scanning signals; and an LCD panel comprising a plurality of gate lines for transmitting the scanning signals; a plurality of data lines, being insulated from the gate lines and crossing them, for transmitting the image signals; and a plurality of pixels, formed by an area surrounded by the gate lines and data lines and arranged as a matrix pattern, having switching elements connected to the gate lines and data lines.

Fig. 1



EP 1 122 711 A2

Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND OF THE INVENTION

(a) Field of the Invention

[0001] The present invention relates to a Liquid Crystal Display (LCD) and driving method thereof. More specifically, the present invention relates to an LCD and driving method for providing compensated data voltage in order to improve a response speed of the liquid crystal.

(b) Description of the Related Art

[0002] As personal computers (PC) and televisions have recently become lighter in weight and slimmer in thickness, display devices have also been required to become lighter and slimmer. Accordingly, flat panel type displa000000000ys such as the LCD instead of cathode ray tubes (CRT) have been developed.

[0003] In the LCD, an electric field is supplied to liquid crystal material having anisotropic permittivity and is injected between two substrates, and the quantity of light projected on the substrates is controlled by the intensity of the electric field, thereby obtaining desired image signals. Such an LCD is one of the most commonly used portable flat panel display devices, and in particular, the thin film transistor liquid crystal display (TFT-LCD) employing the TFT as a switching element is widely utilized.

[0004] As the TFT-LCDs have been increasingly used as display devices of computers and televisions, the need for implementing moving pictures has increased. However, since the conventional TFT-LCDs have a delayed response speed, it is difficult to implement moving pictures using the conventional TFT-LCD. To solve the problem of the delayed response speed, another type of TFT-LCD that uses the optically compensated band (OCB) mode or ferro-electric liquid crystal (FLC) has been developed.

[0005] However, the structure of the conventional TFT-LCD panel must be modified to use the OCB mode or the FLC.

SUMMARY OF THE INVENTION

[0006] It is an object of the present invention to enhance the response speed of the liquid crystal by modifying the liquid crystal driving method without modifying the structure of the TFT-LCD.

[0007] In one aspect of the present invention, an LCD comprises: a data gray signal modifier for receiving gray signals from a data gray signal source, and outputting modification gray signals by consideration of gray signals of present and previous frames; a data driver for changing the modification gray signals into corresponding data voltages and outputting image signals; a gate driver for sequentially supplying scanning signals; and an LCD panel comprising a plurality of gate lines for transmitting the scanning signals; a plurality of data lines, being insulated from the gate lines and crossing them, for transmitting the image signals; and a plurality of pixels, formed by an area surrounded by the gate lines and data lines and arranged as a matrix pattern, having switching elements connected to the gate lines and data lines.

[0008] The data gray signal modifier comprises: a frame storage device for receiving the gray signals from the data gray signal source, storing the gray signals during a single frame, and outputting the same; a controller for controlling writing and reading the gray signals of the frame storage device; and a data gray signal converter for considering the gray signals of a present frame transmitted by the data gray signal source and the gray signals of a previous frame transmitted by the frame storage device, and outputting the modification gray signals.

[0009] The LCD further comprises: a combiner for receiving the gray signals from the data gray signal source, combining the gray signals to be synchronized with the clock signal frequency with which the controller is synchronized, and outputting the combined gray signals to the frame storage device and the data gray signal converter; and a divider for dividing the gray signals output by the data gray signal converter so as to be synchronized with the frequency with which the gray signals transmitted by the data gray signal source are synchronized.

[0010] In another aspect of the present invention, in an LCD driving method comprising a plurality of gate lines; a plurality of data lines being insulated from the gate lines and crossing them; and a plurality of pixels, formed by an area surrounded by the gate lines and data lines and arranged as a matrix pattern, having switching elements connected to the gate lines and data lines, an LCD driving method comprises: (a) sequentially supplying scanning signals to the gate lines; (b) receiving image signals from a image signal source, and generating modification image signals by considering image signals of present and previous frames; and (c) supplying data voltages corresponding to the generated modification image signals to the data lines.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate an embodiment of the invention, and, together with the description, serve to explain the principles of the invention:

FIG. 1 shows an equivalence circuit of an LCD pixel;
FIG. 2 shows data voltages and pixel voltages supplied by a prior driving method;
FIG. 3 shows a transmission of the LCD according to a prior driving method;
FIG. 4 shows a modeled relation between the voltage and permittivity of the LCD;
FIG. 5 shows a method for supplying the data voltage according to a first preferred embodiment of the present invention;
FIG. 6 shows a permittivity of the LCD in case of supplying the data voltage according to the first preferred embodiment of the present invention;
FIG. 7 shows a permittivity of the LCD in case of supplying the data voltage according to a second preferred embodiment of the present invention;
FIG. 8 shows an LCD according to the preferred embodiment of the present invention;
FIG. 9 shows a data gray signal modifier according to the preferred embodiment of the present invention;
FIG. 10 shows a conversion table according to the first preferred embodiment of the present invention;
FIG. 11 shows a data gray signal modifier according to a second embodiment of the present invention;
FIG. 12 conceptually shows an operation of the data gray signal modifier according to the first preferred embodiment of the present invention shown in FIG. 11;
FIG. 13 conceptually shows an operation of the data gray signal modifier according to the second preferred embodiment of the present invention shown in FIG. 11;
FIG. 14 shows a data gray signal modifier according to a third embodiment of the present invention;
FIGs. 15(a) to 15(c) show a conversion process of the modified gray data computed according to the third preferred embodiment of the present invention; and
FIG. 16 shows a waveform diagram for comparing the conventional voltage supply method with that according to the preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0012] In the following detailed description, only the preferred embodiment of the invention has been shown and described, simply by way of illustration of the best mode contemplated by the inventor(s) of carrying out the invention. As will be realized, the invention is capable of modification in various obvious respects, all without departing from the invention. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not restrictive.

[0013] The LCD comprises a plurality of gate lines which transmit scanning signals, a plurality of data lines which cross the gate lines and transmit image data, and a plurality of pixels which are formed by regions defined by the gate lines and data lines, and are interconnected through the gate lines, data lines, and switching elements.

[0014] Each pixel of the LCD can be modeled as a capacitor having the liquid crystal as a dielectric substance, that is, a liquid crystal capacitor, and FIG. 1 shows an equivalence circuit of the pixel of the LCD.

[0015] As shown, the LCD pixel comprises a TFT 10 having a source electrode connected to a data line D_m and a gate electrode connected to a gate line S_n, a liquid crystal capacitor C_1 connected between a drain electrode of the TFT 10 and a common voltage V_{com}, and a storage capacitor C_{st} connected to the drain electrode of the TFT 10.

[0016] When a gate ON signal is supplied to the gate line Sn to turn on the TFT 10, the data voltage V_d supplied to the data line is supplied to each pixel electrode (not illustrated) via the TFT 10. Then, an electric field corresponding to a difference between the pixel voltage Vp supplied to the pixel electrode and the common voltage V_{com} is supplied to the liquid crystal (shown as the liquid crystal capacitor in FIG. 1) so that the light permeates the TFT with a transmission corresponding to a strength of the electric field. At this time, the pixel voltage V_p is maintained during one frame period. The storage capacitor C_{st} is used in an auxiliary manner so as to maintain the pixel voltage V_p supplied to the pixel electrode.

[0017] Since the liquid crystal has anisotropic permittivity, the permittivity depends on the directions of the liquid crystal. That is, when a direction of the liquid crystal is changed as the voltage is supplied to the liquid crystal, the permittivity is also changed, and accordingly, the capacitance of the liquid crystal capacitor (which will be referred to as the liquid crystal capacitance) is also changed. After the liquid crystal capacitor is charged while the TFT is turned ON, the TFT is then turned OFF. If the liquid crystal capacitance is changed, the pixel voltage V_p at the liquid crystal is also changed, since Q=CV.

[0018] For an example of normally white mode twisted nematics (TN) LCD, when zero voltage is supplied to the pixel, the liquid crystal capacitance C(0V) becomes $\varepsilon_\perp A/d$, where $\varepsilon_\perp$ represents the permittivity when the liquid crystal molecules are arranged in the direction parallel with the LCD substrate, that is, when the liquid crystal molecules are arranged in the direction perpendicular with that of the light, 'A' represents the area of the LCD substrate, and 'd' represents the distance between the substrates. If the voltage for implementing a full black is set to be 5V, when the 5V voltage is supplied to the liquid crystal, the liquid crystal is arranged in the direction perpendicular to the substrate, and therefore, the liquid crystal capacitance C(5V) becomes $\varepsilon_{//}$ *A/d*. Since $\varepsilon_{//} - \varepsilon_{\perp} > 0$ in the case of the liquid crystal used in the TN mode, the more the pixel voltage supplied to the liquid crystal becomes greater, the more the liquid crystal capacitance becomes greater.

[0019] The amount the TFT must charge so as to make the n-th frame full black is C(5V) x 5V. However, if it is assumed that the (n-1)th frame is full white (V_{n-1}=0V), the liquid crystal capacitance becomes C(0V) since the liquid crystal has not yet responded during the TFT's turn ON period. Hence, even when the n-th frame supplies 5V data voltage Vd to the pixel, the actual amount of the charge provided to the pixel becomes C(0V) x 5V, and since C(0V) < C(5V), the pixel voltage below 5V (e.g., 3.5V) is actually supplied to the liquid crystal, and the full black is not implemented. Further, when the (n+1)th frame supplies 5V data voltage V_d so as to implement the full black, the amount of the charge provided to the liquid crystal becomes C(3.5V) x 5V, and accordingly, the voltage V_p supplied to the liquid crystal ranges between 3.5V and 5V. After repeating the above-noted process, the pixel voltage V_p reaches a desired voltage after a few frames.

[0020] The above-noted description will now be described with respect to gray levels. When a signal (a pixel voltage) supplied to a pixel is changed from a lower gray to a higher gray (or from a higher gray to a lower gray), the gray of the present frame reaches the desired gray after a few frames since the gray of the present frame is affected by the gray of a previous frame. In a similar manner, the permittivity of the pixel of the present frame reaches a desired value after a few frames since the permittivity of the pixel of the present frame is affected by that of the pixels of the previous frame.

[0021] If the (n-1)th frame is full black, that is, the pixel voltage V_p is 5V, and the n-th frame supplies 5V data voltage so as to implement the full black, the amount of the charge corresponding to C(5V) x 5V is charged to the pixel since the liquid crystal capacitance is C(5V), and accordingly, the pixel voltage V_p of the liquid crystal becomes 5V.

[0022] Therefore, the pixel voltage V_p actually supplied to the liquid crystal is determined by the data voltage supplied to the present frame as well as the pixel voltage V_p of the previous frame.

[0023] FIG. 2 shows the data voltages and pixel voltages supplied by a prior driving method.

[0024] As shown, the data voltage V_d corresponding to a target pixel voltage V_w is conventionally supplied for each frame without regarding the pixel voltage V_p of the previous frame. Hence, the actual pixel voltage V_p supplied to the liquid crystal becomes lower or higher than the target pixel voltage by the liquid crystal capacitance corresponding to the pixel voltage of the previous frame, as described above. Hence, the pixel voltage V_p reaches the target pixel voltage after a few frames.

[0025] FIG. 3 shows a transmission of the LCD according to a prior driving method.

[0026] As shown, since the actual pixel voltage becomes lower than the target pixel voltage, the permittivity reaches the target permittivity after a few frames even when the response time of the liquid crystal is within one frame.

[0027] In the preferred embodiment of the present invention, a picture signal S_n of the present frame is compared with a picture signal S_{n-1} of a previous frame so as to generate a modification signal S_n' and the modified picture signal S_n' is supplied to each pixel. Here, the picture signal S_n represents the data voltage in the case of analog driving methods. However, since binary gray codes are used to control the data voltage in digital driving methods, the actual modification of the voltage supplied to the pixel is performed by the modification of the gray signal.

[0028] First, if the picture signal (the gray signal or data voltage) of the present frame is identical with the picture signal of the previous frame, the modification is not performed.

[0029] Second, if the gray signal (or the data voltage) of the present frame is higher than that of the previous frame, a modified gray signal (data voltage) higher than the present gray signal (data voltage) is output, and if the gray signal (or the data voltage) of the present frame is lower than that of the previous frame, a modified gray signal (data voltage) lower than the present gray signal (data voltage) is output. At this time, the modification degree is proportional to the difference between the present gray signal (data voltage) and the gray signal (data voltage) of the previous frame.

[0030] A method for modifying the data voltage according to a preferred embodiment will now be described.

[0031] FIG. 4 shows a modeled relation between the voltage and permittivity of the LCD.

[0032] As shown, the horizontal axis represents the pixel voltage, and the perpendicular axis represents a ratio between the permittivity $\varepsilon(v)$ at a predetermined pixel voltage v and the permittivity $\varepsilon_{\perp}$ at the time the liquid crystal is arranged parallel to the substrate, that is, when the liquid crystal is perpendicular to the permeating direction of the light.

[0033] The maximum value of $\varepsilon(v)/\varepsilon_{\perp}$, that is, $\varepsilon_{//}/\varepsilon_{\perp}$ is assumed to be 3, V_{th} to be 1V, and V_{max} to be 4V. Here, the V_{th} and V_{max} respectively represent the pixel voltages of the full white and full black (or vice versa).

[0034] When the capacitance of the storage capacitor (which will be referred to as the storage capacitance) is set to be identical with an average value $<C_{st}>$ of the liquid crystal capacitance, and the area of the LCD substrate and distance between the substrates are respectively set to be 'A' and 'd', the storage capacitance C_{st} can be expressed as Equation 1.

Equation 1 $C_{st} = \langle C_l \rangle = (1/3)\cdot(\varepsilon_{//} + 2\varepsilon_{\perp})\cdot(A/d) = (5/3)\cdot(\varepsilon_{\perp}\cdot A/d) = (5/3)\cdot C0$

where $C0 = \varepsilon_{\perp}\cdot A/d$.

[0035] Referring to FIG. 4, $\varepsilon(v)/\varepsilon_{\perp}$ can be expressed as Equation 2.

Equation 2 $\varepsilon(v)/\varepsilon_{\perp} = (1/3)\cdot(2V+1)$

[0036] Since total capacitance C(V) of the LCD is the sum of the liquid crystal and the storage capacitance, the capacitance C(V) can be expressed in Equation 3 from Equations 1 and 2.

Equation 3

$$C(V) = C_l + C_{st} = \varepsilon(v)\cdot(A/d) + (5/3)\cdot C0 = (1/3)\cdot(2V+1)\cdot C0 + (5/3)\cdot C0$$
$$= (2/3)\cdot(V+3)\cdot C0$$

[0037] Since the charge Q supplied to the pixel is preserved, the following Equation 4 is established.

Equation 4 $Q = C(V_{n-1})\cdot V_n = C(V_f)\cdot V_f$

where V_n represents the data voltage (or, an absolute value of the data voltage of an inverting driving method) to be supplied to the present frame, $C(V_{n-1})$ represents the capacitance corresponding to the pixel voltage of the previous frame (that is, (n-1)th frame), and $C(V_f)$ represents the capacitance corresponding to the actual voltage V_f of the pixel of the present frame (that is, n-th frame).

[0038] Equation 5 can be derived from Equations 3 and 4.

Equation 5 $C(V_{n-1})\cdot V_n = C(V_f)\cdot V_f = (2/3)\cdot(V_{n-1} + 3)\cdot V_n = (2/3)\cdot(V_f + 3)\cdot V_f$

[0039] Hence, the actual pixel voltage Vf can be expressed as Equation 6.

Equation 6 $V_f = (-3 + \sqrt{9 + 4V_n(V_{n-1}+3)})/2$

[0040] As clearly expressed in Equation 6, the actual pixel voltage V_f is determined by the data voltage V_n supplied to the present frame and the pixel voltage V_{n-1} supplied to the previous frame.

[0041] If the data voltage supplied in order for the pixel voltage to reach the target voltage V_n at the n-th frame is set to be V_n', the data voltage V_n' can be expressed as Equation 7 from Equation 5.

Equation 7 $(V_{n-1} + 3)\cdot V_n' = (V_n + 3)\cdot V_n$

[0042] Hence, the data voltage V_n' can be expressed as Equation 8.

Equation 8 $$V_n' = \frac{V_{n+3}}{V_{n-1} + 3}\cdot V_n = V_n + \frac{V_n - V_{n-1}}{V_{n-1} + 3}\cdot V_n$$

[0043] As noted-above, when supplying the data voltage V_n' obtained by the Equation 8 by the consideration of the target pixel voltage V_n of the present frame and the pixel voltage V_{n-1} of the previous frame, the pixel voltage can directly reach the target pixel voltage V_n.

[0044] Equation 8 is derived from FIG. 4 and a few assumptions, and the data voltage V_n' applied to the general LCD can be expressed as Equation 9.

Equation 9 $$|V'_n| = |V_n| + f(|V_n|-|V_{n-1}|)$$

where the function f is determined by the characteristics of the LCD. The function *f* has the following characteristics.

[0045] That is, $f = 0$ when $|V_n|=|V_{n-1}|$, $f > 0$ when $|V_n|>|V_{n-1}|$, and $f < 0$ when $|V_n| < |V_{n-1}|$.

[0046] A method for supplying the data voltage according to a first preferred embodiment of the present invention will now be described.

[0047] FIG. 5 shows the method for supplying the data voltage.

[0048] As shown in the first preferred embodiment, the data voltage V_n' modified by consideration of the target pixel voltage of the present frame and the pixel voltage (data voltage) of the previous frame is supplied, and the pixel voltage Vp reaches the target voltage. That is, in the case the target voltage of the present frame is different from the pixel voltage of the previous frame, the voltage higher (or lower) than the target voltage of the present frame is supplied as the modified data voltage so as to reach the target voltage level at the first frame, and after this, the target voltage is supplied as the data voltage at the following frames. Therefore, the response speed of the liquid crystal can be increased.

[0049] At this time, the modified data voltage (charges) is determined by consideration of the liquid crystal capacitance determined by the pixel voltage of the previous frame. That is, the charge Q is supplied by considering the pixel voltage level of the previous frame so as to directly reach the target voltage level at the first frame.

[0050] FIG. 6 shows a permittivity of the LCD in the case of supplying the data voltage according to the first preferred embodiment of the present invention. As shown, since the modified data voltage is supplied according to the first preferred embodiment, the permittivity directly reaches the target permittivity.

[0051] In a second preferred embodiment, a modified voltage V_n' a little higher than the target voltage is supplied to the pixel voltage. As shown in FIG. 7, the permittivity becomes lower than the target permittivity before a half of the response time of the liquid crystal, but after this, the permittivity becomes overcompensated compared to the target value so that the average permittivity becomes equal to the target permittivity.

[0052] An LCD will now be described according to a preferred embodiment of the present invention.

[0053] FIG. 8 shows an LCD according to the preferred embodiment of the present invention. The LCD according to the preferred embodiment uses a digital driving method.

[0054] As shown, the LCD comprises an LCD panel 100, a gate driver 200, a data driver 300 and a data gray signal modifier 400.

[0055] A plurality of gate lines S1, S2, ..., Sn for transmitting gate ON signals, and a plurality of data lines D1, D2, ..., Dn for transmitting the modified data voltages are formed on the LCD panel 100. An area surrounded by the gate lines and data lines forms a pixel, and the pixel comprises TFTs 110 having a gate electrode connected to the gate line and having a source electrode connected to the data line, a pixel capacitor C1 connected to a drain electrode of the TFT 110, and a storage capacitor C_{st}.

[0056] The gate driver 200 sequentially supplies the gate ON voltage to the gate lines so as to turn on the TFT having a gate electrode connected to the gate line to which the gate ON voltage is supplied.

[0057] The data gray signal modifier 400 receives n-bit data gray signals G_n from a data gray signal source (e.g., a graphic signal controller), and outputs the m-bit modified data gray signals G_n' by consideration of the m-bit data gray signals of the present and previous frames. At this time, the data gray signal modifier 400 can be a stand-alone unit or can be integrated into a graphic card or an LCD module.

[0058] The data driver 300 converts the modified gray signals G_n' received from the data gray signal modifier 400 into corresponding gray voltages (data voltages) so as to supply the same to the data lines.

[0059] FIG. 9 shows a detailed block diagram of the data gray signal modifier 400 of FIG. 8.

[0060] As shown, the data gray signal modifier 400 comprises a combiner 410, a frame memory 420, a controller 430, a data gray signal converter 440 and a divider 450. The combiner 410 receives gray signals from the data gray signal source, and converts the frequency of the data stream into a speed that can be processed by the data gray signal modifier 400. For example, if 24-bit data synchronized with the 65MHz frequency are transmitted from the data gray signal source and the processing speed of the components of the data gray signal modifier 400 is limited within 50MHz, the combiner 410 combines the 24-bit gray signals into 48-bit gray signals G_m two by two and then transmits the same to the frame memory 420.

[0061] The combined gray signals G_m output the previous gray signals G_{m-1} stored in a predetermined address to the data gray signal converter 440 according to a control process by the controller 430 and concurrently stores the gray signals G_m transmitted by the combiner 410 in the above-noted address. The data gray signal converter 440 receives the present frame gray signals G_m output by the combiner and the previous frame gray signals G_{m-1} output by the frame memory 420, and generates modified gray signals G_m' by processing the gray signals of the present and previous frames.

[0062] The divider 450 divides 48-bit modified data gray signals G_m' output by the data gray signal converter 440 and outputs 24-bit modified gray signals G_n'.

[0063] In the preferred embodiment of the present invention, since the clock frequency synchronized to the data gray signal is different from that for accessing the frame memory 420, the combiner 410 and the divider 450 are needed, but in the case the clock frequency synchronized to the data gray signal is identical with that for accessing the frame memory 420, the combiner 410 and the divider 450 are not needed.

[0064] Any digital circuits that satisfy the above-defined equation 9 can be manufactured as the data gray signal converter 440.

[0065] Also, in the case a lookup table is made and stored in a read only memory (ROM), the gray signals can be modified by accessing the lookup table.

[0066] Since the modified gray voltage V_n' is not only proportional to the difference between the data voltage V_{n-1} of the previous frame and the V_n of the previous frame but also depends on their respective absolute values, the configuration of the lookup table makes the circuit more easy compared to the computation process.

[0067] In order to modify the data voltage according to the preferred embodiment of the present invention, a dynamic range wider than the actually used gray scale range must be used. In the analog circuits, this problem can be solved using high voltage integrated circuits, but in the digital circuit, the number of the grays is restricted. For example, in the 6-bit gray case, a portion of the 64 gray levels has to be assigned not for the actual gray representation but for the modified voltage. That is, a portion of the gray level should be assigned for modification of the voltage, and hence the number of the grays to be represented is reduced.

[0068] In order to prevent the reduction of the number of the grays, a truncation concept can be introduced. For example, it is assumed that the voltage from 0 to 8V is necessary when the liquid crystal is activated at voltage from 1 to 4V and a modification voltage is considered. At this time, when dividing the voltage having the range from 0 to 8V into 64 levels in order to perform a full modification, the number of the grays which can be actually represented becomes about 30 at most. Therefore, in the case the range of the voltage becomes 1 to 4V and the modified voltage V_n' becomes greater than 4V, the number of the grays can be reduced if truncating all the modification voltages to 4V.

[0069] FIG. 10 shows a configuration of the lookup table to which the concept of the truncation is introduced according to the preferred embodiment of the present invention.

[0070] In the preferred embodiments of the present invention, the LCD driven by a digital method is described, and also the present invention can be applied to the LCD driven by an analog method.

[0071] In this case, a data gray signal modifier which functions corresponding to the data gray signal modifier as described in FIG. 8 is needed, and this data gray signal modifier can be implemented using an analog circuit that satisfies the equation 9.

[0072] As described above, the pixel voltage reaches the target voltage level as the data voltage is modified and the modified data voltage is provided to the pixels. Therefore, the configuration of the TFT LCD panel is not needed to be changed and the response speed of the liquid crystal can be improved.

[0073] FIG. 11 shows a detailed block diagram of the data gray signal modifier 400 according to a second preferred embodiment of the present invention.

[0074] As shown, the data gray signal modifier 400 comprises a frame memory 460, a controller 470 and a data gray signal converter 480, and receives n-bit gray signals of the respective red (R), green (G) and blue (B) from the data gray signal source. Therefore, the total number of bits of the gray signals transmitted to the data gray signal converter 480 becomes (3 x n) bits. Here, a skilled person can make either the (3 x n)-bit gray signals be concurrently supplied to the data gray signal modifier 480 from the data gray signal source, or make the respective n-bit R, G and B gray signals be sequentially supplied to the same.

[0075] Referring to FIG. 11, the frame memory 460 fixes the bit of the gray signal to be modified. The frame memory 460 receives m bits of the n-bit R, G and B gray signals from the data gray signal source, stores the same in predetermined addresses corresponding to the R, G and B, and outputs the same to the data gray signal converter 480 after a single frame delay. That is, the frame memory 460 receives the m-bit gray signals G_n of the present frame and outputs m-bit gray signals G_{n-1} of the previous frame.

[0076] The data gray signal converter 480 receives (n-m) bits of the present frame G_n which are passed through without modification, m bits of the present frame received for modification, and m bits of the previous frame G_{n-1} delayed by the frame memory 460, and then generates the modified gray signals G_n' by considering the m bits of the present and previous frames.

[0077] The above-noted description will now be further provided, with reference to FIG. 12.

[0078] FIG. 12 conceptually shows an operation of the data gray signal modifier according to the first preferred embodiment of the present invention. It is assumed that the R, G and B gray signals transmitted to the data gray signal modifier 400 from the data gray signal source are respectively 8-bit signals.

[0079] Two bits (bits of the present frame) starting from the LSB among 8-bit gray signals transmitted to the data gray signal modifier 400 are not modified, and they are input to the data gray signal converter 480. The remaining 6 bits of the present frame are input to the data gray signal converter 480 for modification and concurrently stored in predetermined addresses of the frame memory 460.

[0080] Here, since the frame memory 460 stores the bit of the present frame during a single frame period and then outputs the same, 6-bit gray signals of the previous frame are output to the data gray signal converter 480.

[0081] The data gray signal converter 480 receives 6-bit gray signals of the present frame and 6-bit R gray signals of the previous frame, generates modified gray signals considering the 6-bit R gray signals of the previous and present frames, adds the generated 6-bit gray signals and the 2-bit LSB gray signals of the present frame, and outputs finally modified 8-bit gray signals G_n'.

[0082] In the same manner as with the R gray signals, the data gray signal converter 480 outputs modified 8-bit G and B gray signals considering the 6-bit gray signals of the present and previous frames. The 8-bit modified gray signals are converted into corresponding voltages by a data driver and supplied to the data lines.

[0083] Here, the 6-bit R, G and B gray signals are stored in the established addresses of the frame memory 460. A skilled person can use a single frame memory 460 to assign the addresses for covering the R, G and B, or use three frame memories for the respective R, G and B to function as a single frame.

[0084] Through the description referred to in FIG. 12, when 8-bit gray signals are input from the data gray signal source, the prior frame memory stores 8-bit R, G and B gray signals in the case of SXGA (1,280 x 1,024), and therefore at least 30 Mb memories are necessary, but the frame memory 460 according to the preferred embodiment of the present invention only stores 6-bit gray signals, thereby reducing memory capacity needed.

[0085] Here, the more the number of the bits of the gray signals stored in the frame memory 460 becomes lower, the more the capacity needs of the frame memory 460 become lower, compared to the prior art.

[0086] An operation of the data gray signal modifier according to the second preferred embodiment will now be described.

[0087] FIG. 13 conceptually shows an operation of the data gray signal modifier according to the second preferred embodiment of the present invention. For easy understanding, the data gray signal modifier is designed using one frame memory and one data gray signal converter. However, the number of the frame memories and the data gray signal converters can be changed according to grades of the LCD panels, the bit number of the gray signals, and designer's intention. For example, three memories for configuring the frame memory and the data gray signal converter can be used to process R, G and B.

[0088] A skilled person can configure the frame memory by using first and second memories for processing reading and writing processes corresponding to the respective R, G and B gray signals so as to enhance data processing speed.

[0089] That is, when the gray signals are sequentially input to the frame memory, odd-numbered gray signals are stored in the first memory, and even-numbered gray signals are stored in the second memory, and when the odd-numbered gray signals are stored in the first memory, the second memory reads the first memory, and when the even-numbered gray signals are stored in the second memory, the first memory reads the second memory so that the data can be written/read to from the frame memory within a shorter time.

[0090] Referring to FIG. 13, the configuration of the data gray signal modifier 400 is identical with that of the first preferred embodiment. However, the data gray signal modifier 400 according to the second preferred embodiment is different from that of the first preferred embodiment in that the data gray signal modifier 400 according to the second preferred embodiment reduces the bit number of the output gray signals compared to the bit number of the input gray signals. An operation of the data gray signal modifier 400 will now be described.

[0091] When the 8-bit R, G and B gray signals are provided by the data gray signal source, the lower 3 bits of the 8-bit R gray signals are not modified and are passed though the dotted line in the figure, and the remaining 5 bits of the present frame are input to the data gray signal converter 480 and the frame memory 460.

[0092] The 5-bit R gray signals of the present frame input to the frame memory 460 are stored in predetermined addresses and then output at the next frame, and 5-bit R gray signals of the previous frame are output to the data gray signal converter 480. The data gray signal converter 480 then receives the 5-bit R gray signals of the present and previous frames G_n and G_{n-1}, generates the modified gray signals G_n' proportional to the differences between the gray signals of the present and previous frames, and outputs the same. At this time, the modified R gray signals G_n' are 8-bit signals obtained by an addition of the modified 5 bits and the unmodified 3 bits.

[0093] Two bits of the 8-bit G gray signals are passed via the dotted line, and remaining 6-bit gray signals G_n are input to the data gray signal converter 480 and the frame memory 460. Here, the frame memory 460 stores the 6-bit G gray signals of the present frame in a predetermined address, and outputs the 6-bit G gray signals of the previous frame G_{n-1}. Therefore, the data gray signal converter 480 outputs the modified gray signals G_n' using the 6-bit G gray signals of the present and previous frames. At this time, the modified G gray signals G_n' are obtained by an addition of the modified 6 bits and unmodified 2 bits.

[0094] Finally, 3 bits of the 8-bit B gray signals are passed via the dotted line, and remaining 5-bit gray signals G_n are input to the data gray signal converter 480 and the frame memory 460. Here, the frame memory 460 stores the 5-bit G gray signals of the present frame in a predetermined address and outputs the 5-bit G gray signals of the previous frame G_{n-1}. Hence, the data gray signal converter 480 outputs modified gray signals G_n' by using the 5-bit G gray signals of the present and previous frames. At this time, the modified G gray signals G_n' are 8 bits obtained by an addition of the modified 5 bits and unmodified 3 bits.

[0095] As described above, it is preferable that the passed bits among the 8-bit R, G and B gray signals start from the LSB, and a skilled person can change the number of the passed bits. Hence, the skilled person can change the capacity and number of the frame memories and modify the date gray signal converter. A digital circuit that satisfies Equation 9 can be manufactured as the data gray signal converter 480 according to the preferred embodiment, or a look-up table is made and then stored into a read only memory (ROM), and accessed to modify the gray signals. Since the modified data voltage V_n' is not only proportional to the difference between the data voltage V_{n-1} of the previous frame and that of the present frame, but is also dependent on absolute values of the data voltages, the look-up table makes the configuration of the circuit simpler than computation.

[0096] Referring to FIGs. 12 and 13, an example of a case in which an LCD panel is the SXGA (1,280 x 1,024) type and 8-bit gray signals are supplied will now be described.

[0097] Conventionally, in this case, the frame memory requires at least 30 Mb, and the data gray signal converter requires 512Kb x 6 when processing two R, G and B pixels per clock signal of the control signals output by the controller 470, and it requires 512Kb x 3 when processing one R, G and B pixel per clock signal.

[0098] In detail, in the case of processing two pixels per clock signal, the data gray signal modifier 400 receives 48-bit signals. Since the bus size of the memory is configured as x4, x8, x16 and x32, the 48-bit bus is configured using three 16-bit wide memories.

[0099] However, since the bits from the LSB to the i (i=1, 2, ..., n-1) among the n bits are modified and the remaining parts are not modified in the preferred embodiment of the present invention, the capacity of the frame memory and the data gray signal converter can be reduced. For example, when n=8 and i=2, since six MSBs are needed to be modified and the remaining two bits are not needed to be modified, the frame memory only needs the capacity of 1,280 x 1,024 x 6 bits = 22.5Mb, and since the data gray signal converter can use six bits instead of an 8-bit gray table memory (512Kb), the size is greatly reduced to 24Kb in the case of one pixel per clock signal, and reduced to 6 x 24Kb in the case of two pixels per clock signal.

[0100] In the preferred embodiment, a number of modification bits are omitted in the modification of the gray signals since human eyes are not as sensitive to moving pictures as to still pictures, and therefore it is desirable to omit a number of modification bits within ranges wherein the human eyes cannot discern the variation of the gray signals of the moving pictures.

[0101] Since peoples' eyes have different sensitivity with respect to R, G and B, it is desirable to differently omit the number of modification bits with respect to the gray signals of the corresponding color. That is, since human eyes are most sensitive to green and least sensitive to blue, it is desirable that the number of modification bits 'i' be in the order of G ≤R≤B.

[0102] According to the present invention, the data voltage is modified and the modified data voltage is supplied to the pixels so that the pixel voltage reaches the target voltage level. Hence, the response speed of the liquid crystal can be improved without changing the configuration of the TFT-LCD panel.

[0103] Further, since only 'm' bits among n-bit gray signals are used, the number and capacity of the memory needed for modification of the data voltage can be reduced, thereby increasing yield of the panels and reducing the cost.

[0104] As described above, an image signal modification circuit for improving the response speed of the liquid crystal is shown in FIGs. 9 and 11.

[0105] Particularly, in order to reduce the cost of the image signal modification circuit, the gray signals except a portion of the LSB are modified, and this algorithm is simple and easy to apply.

[0106] However, in the case of modifying four bits of the 8-bit gray, two problems caused by quantization can be generated as follows.

[0107] It is assumed that the response speed becomes maximized when 168 (10101000) gray level (G_n') is defined as the DCC modification value in the case 208 (11010000) gray level (G_{n-1}) is switched to 192 (11000000) gray level (G_n). A modification of the full 8 bits generates no problem, but a modification of MSB 4 bits so as to reduce the cost, the value 168 can not be provided to the gray lookup table. Therefore, the value of 176 (10110000) or 160 (10100000) is input to the lookup table instead. That is, modification errors are generated as much as the omitted LSB bits. This can generate a greater problem in the following interval.

Table 1

Gn'		Gn-1																
		1	16	32	48	64	80	96	112	128	144	160	176	192	208	224	240	255
Gn	32	33	33	32	30	28	26	24	22	20	16	12	9	9	9	0	0	0

[0108] In this interval, the modification is gradually performed. In the case of configuring this interval using only 4 bits, it becomes as follows.

Table 2

Gn'		Gn-1																
		0	16	32	48	64	80	96	112	128	144	160	176	192	208	224	240	255
Gn	32	32	32	32	32	32	32	32	16	16	16	16	16	0	0	0	0	0

[0109] The second problem is as follows. In the like manner of the previous example, if it is assumed that 1 176 gray level is provided as a modification value when the 208 gray level is switched to the 192 gray level, the 176 or 175 gray level must be provided to obtain a maximum liquid crystal response speed when the 207 gray level is switched to the 192 gray level.

[0110] However, in the case of modifying only 4 bits, since the MSB 4 bits of 207 (11001111) is identical with that of 192 (11000000), the modification is not performed and the 192 is output.

[0111] Particularly, in the case of moving pictures, the grays of 209 and 207 gray levels are distributed on a uniform screen of about 208 gray level, and although the difference between the 208 and 207 gray levels is 1, degrees of compensation become greater, and accordingly, some displayed stains may look exaggerated.

[0112] The above-noted two problems are referred to as the quantization errors, and when the number of the LSBs which are not modified but omitted is increased, the quantization errors become severe.

[0113] An LCD for reducing the quantization errors will now be described.

[0114] FIG. 14 shows a data gray signal modifier according to a third embodiment of the present invention. Repeated portions compared to FIG. 9 will be assigned with identical reference numerals and no further description will be provided.

[0115] Referring to FIG. 14, the data gray signal converter 460 of the data gray signal modifier comprises a lookup table 462 and a calculator 464.

[0116] As MSB 4-bit gray data $G_m[0:3]$ of the present frame and MSB 4-bit gray data $G_{m-1}[0:3]$ of the previous frame are provided by the combiner 410, the values f, a and b stored in the lookup table are extracted and provided to the calculator 464.

[0117] The calculator 464 receives the LSB 4-bit gray data $G_m[4:7]$ of the present frame from the combiner 410, the LSB 4-bit gray data $G_{m-1}[4:7]$ of the previous frame from the frame memory 420, the variables f, a and b for modification of the moving pictures from the lookup table, and performs a predetermined computation and outputs first modified gray data $G_m'[0:7]$ to the divider 450.

[0118] The first modified 36-bit gray data provided to the divider 450 are divided, and the modified 24-bit gray data G_n' are output to the data driver 300.

[0119] In the preferred embodiments of the present invention as shown in FIG. 8, the LCD driven by a digital method is described, and also the present invention can be applied to the LCD driven by an analog method.

[0120] According to a second preferred embodiment of the present invention, effects of reduction of the quantization errors will now be described in detail.

[0121] First, if the total gray levels are set to be x bits, the MSB y bits of the x bits are modified using the gray lookup table and the remaining z bits, that is (x-y) bits are modified by computation.

[0122] An example will now be described when x=8 and y=4.

[0123] For ease of explanation, the following will be defined. [A]n is a multiple of the maximum 2^n not greater than A. For example, $[207]_4=[206]_4=[205]4= \ldots =[193]_4=[192]_4=192$.

[0124] That is, $[A]_n$ is a value representing that zeros are provided to all the LSB n bits of A, $_m[A]$ is a value representing that zeros are provided to all the MSB m bits of A, and $_m[A]_n$ is a value representing that zeros are provided to all the LSB n bits and MSB m bits of A. When a mapping according to the gray lookup table for modification is set to be $f(G_n, G_{n-1})$, the modification of the present invention is as follows.

Equation 10 $$G_n^{'}=f([G_n]_4,[G_{n-1}]_4)+a([G_n]_4,[G_{n-1}]_4)\cdot \frac{_4[G_n]}{16} - b([G_n]_4,[G_{n-1}]_4)\cdot \frac{_4[G_n]}{16}$$

where $[G_n]_4$ represents that zeros are provided to all the LSB 4 bits of Gn, $[G_{n-1}]_4$ represents that zeros are provided to all the LSB 4 bits of G_{n-1}, $4[G_n]$ represents that zeros are provided to all the MSB 4 bits of G_n, and a and b are positive integers.

[0125] According to the equation 10, the quantization errors can be reduced by using the gray lookup table.

[0126] The f, a and b are given as follows.

$$f([G_n]_4,[G_{n-1}]_4)=G_n^{'}([G_n]_4,[G_{n-1}]_4)$$

$$a([G_n]_4,[G_{n-1}]_4) = G_n^{'}([G_n]_4+16,[G_{n-1}]_4) = G_n^{'}([G_n]_4,[G_{n-1}]_4)$$

$$b([G_n]_4,[G_{n-1}]_4)=G_n^{'}([G_n]_4, [G_{n-1}]_4)-G_n^{'}([G_n]_4, [G_{n-1}]_4 + 16)$$

[0127] It is assumed that a gray lookup table for modification is obtained as shown in FIG. 3.

Table 3

Gn'		Gn-1	
		64	80
Gn	128	140	136
	144	160	158

[0128] For example if it is set that $[G_n]_4$=128 and $[G_{n-1}]$4=64, then it becomes that f([Gn]4,$[G_{n-1}]_4$)=140, a([Gn]4, $[G_{n-1}]_4$)=160-140=20 and b([Gn]4,$[G_{n-1}]$4)=140- 136=4. However, these values are not absolute and the values are determined so that the values in the 16 x 16 interval may be approximated with minimized errors.

[0129] For example when approximating the case of G_n=144 and G_{n-1} = 80 by using the equation 10, since Gn'=140+20x16/16-4x16/16 156. the value is different from the actually measured value 158. This error can be ignored, but if the error becomes greater. the error of the values in the 16 x 16 interval can be minimized by precisely adjusting the values of f, a and b

[0130] An exceptional case is a block of $[G_n]_4=[G_{n-1}]_4$. In this case, since a state that $G_n'=G_n$ must be maintained, a state that f=$[G_n]_4$ is fixed and the values of a and b are adjusted according to the state. If $G_n=G_{n-1}$ in the equation 10, when it becomes that a-b=16 then the state that $G_n'=G_n$ is satisfied.

[0131] An example will be described in order to describe the modified gray data computed using the equation 10.

[0132] For example, when a previous gray data G_{n-1} is a 72 gray level and a present gray data G_n is a 136 gray level, since the gray lookup table of the table 3 does not have the above-noted gray data, these values must be obtained by a predetermined computation as shown in FIG. 15(a).

[0133] That is, since f([Gn]4.$[G_{n-1}]_4$)=f($[136]_4$,$[72]_4$), it is satisfied that f(128,64)=140, a($[Gn]_4$,$[G_{n-1}]_4$)=160-140=20 and b($[Gn]_4$,$[G_{n-1}]_4$)=140-136=4.

[0134] Hence, when substituting the values for the equation 10, it becomes that G_n'=140+20x(136-128)/16-4x(72-64) /16=148.

[0135] Also, in order to reduce the number of the bits stored in the lookup table, subsequent equation 11 can be used.

Equation 11 $$G_n'=f'+[G_n]_4+a\cdot([G_n]_4,[G_{n-1}]_4)\cdot\frac{{}_4[G_n]}{16}-b\cdot([G_n]_4,[G_{n-1}]_4)\cdot\frac{{}_4[G_n]}{16}$$

where it is defined that f'=f($[G_n]_4$,$[G_{n-1}]_4$)-$[G_n]_4$, and $[G_n]_4$ represents that zeros are provided to all the LSB 4 bits of G_n, and $[G_{n-1}]_4$ represents that zeros are provided to all the LSB 4 bits of G_{n-1}, and ${}_4[G_n]$ represents that zeros are provided to all the MSB 4 bits of G_n. and the values a and b are positive integers.

[0136] An example will be described in order to describe the modified gray data computed using the equation 11.

[0137] For example, when a previous gray data G_{n-1} is a 72 gray level and a present gray data G_n is a 136 gray level, since the gray lookup table of the table 3 does not have the above-noted gray data, these values must be obtained by a predetermined computation as shown in FIG. 15(c).

[0138] That is, f'=f([Gn]4,$[G_{n-1}]_4$)-$[G_n]_4$=f($[136]_4$,$[72]_4$)-128=f(128,64)-128=140- 128=12, a"($[G_n]_4$, $[G_{n-1}]_4$)=a'$(G_n)_4$, $[G_{n-1}]_4$)+2^4=4+16=20 and b($[G_n]_4$,$[G_{n-1}]_4$)=4.

[0139] Hence, when substituting the values for the equation 11, it becomes that G_n'=128+12+20x(136-128)/16-4x (72-64)/16=148.

[0140] Also, in order to reduce the number of the bits stored in the lookup table, subsequent equation 12 can be used.

Equation 12 $$G_n'=f'([G_n]_4,[G_{n-1}]_z)+G_n+a'\cdot([G_n]_4,[G_{n-1}]_4)\cdot\frac{{}_4[G_n]}{16}-b\cdot([G_n]_4,[G_{n-1}]_4)\cdot\frac{{}_4[G_n]}{16}$$

where it is defined that f'=f-G_n, and $[G_n]_4$ represents that zeros are provided to all the LSB 4 bits of G_n, and $[G_{n-1}]_4$ represents that zeros are provided to all the LSB 4 bits of G_{n-1}, and ${}_4[G_n]$ represents that zeros are provided to all the MSB 4 bits of G_n, and the value a'is an integer, and the value b is a positive integer.

[0141] That is, it becomes that a'($[G_n]_4$,$[G_{n-1}]_4$)=a($[G_n]_4$,$[G_{n-1}]_4$)-2^4.

[0142] An example will be described in order to describe the modified gray data computed using the equation 12.

[0143] For example, when a previous gray data G_{n-1} is a 72 gray level and a present gray data G_n is a 136 gray level, since the gray lookup table of the table 3 does not have the above-noted gray data, these values must be obtained by a predetermined computation as shown in FIG. 15(b).

[0144] That is, since $f([G_n]_4,[G_{n-1}]_4)=f([136]4,[72]_4)=f(128,64)=140$, it is satisfied that $f'=f([G_n]_4,[G_{n-1}]_4)-G_n=140-128=12$, $G_n=136$, $a'([Gn]_4,[G_{n-1}]_4)=a'-16=4$ and $b([G_n]_4,[G_{n-1}]_4)=4$.

[0145] Hence, when substituting the values for the equation 12, it becomes that $G_n'=132+12+4x(136-128)/16-4x(72-64)/16=148$.

[0146] In this case, since the value of a' becomes smaller, the number of the bits assigned to (-16)a' can be reduced, but a' can be negative number in some intervals, and accordingly, an additional sign bit must be assigned.

[0147] As described above, the size of the lookup table for the modified gray data becomes smaller in order of equations 10, 11 and 12, and the logic complication increases on the contrary.

[0148] In the above, modification of 8 bits is described.

[0149] However, all the 8-bit data may not be stored when the capacity of the frame memory or the number of input/output pins should be reduced.

[0150] For example, since dimensions of a DRAM include x4, x8, x16 and x32, the dimension of x32 should be used so as to store 24-bit color information of the respective R, G and B, but it costs a lot. Instead of the dimension of x32, a dimension of x16 can be used, and 5-bit R, 6-bit G and 5-bit G can only be stored. The modification in this case is executed as follows

[0151] That is, in the case of 6 bits, the modification gray values are output as follows.

Equation 13 $$G_n' = f([G_n]_4,[G_{n-1}]_4)+a\cdot[G_n]_4,[G_{n-1}]_4)\cdot\frac{{}_4[G_n]}{16}-b\cdot([G_n]_4,[G_{n-1}]_4)\cdot\frac{{}_4[G_n]\gg 2}{4}$$

where it is defined that $[G_n]_4$ represents that zeros are provided to all the LSB 4 bits of G_n, and $[G_{n-1}]_4$ represents that zeros are provided to all the LSB 4 bits of G_{n-1}, and ${}_4[G_n]$ represents that zeros are provided to all the MSB 4 bits of G_n, and the values a and b are positive integers, and ${}_4[G_n]\gg 2$ functions such that binary data of the computed ${}_4[G_n]_2$ are shifted in the right direction by 2 bits, and as a result, it functions as division by 22.

[0152] Also, in the case of 5 bits, the modification gray values are output as follows.

Equation 14 $$G_n' = f([G_n]_4,[G_{n-1}]_4)+a\cdot([G_n]_4,[G_{n-1}]_4)\cdot\frac{{}_4[G_n]}{16}-b\cdot([G_n]_4,[G_{n-1}]_4)\cdot\frac{{}_4[G_n]\gg 3}{2}$$

where it is defined that $[G_n]_4$ represents that zeros are provided to all the LSB 4 bits of G_n, and $[G_{n-1}]_4$ represents that zeros are provided to all the LSB 4 bits of G_{n-1}, and ${}_4[G_n]$ represents that zeros are provided to all the MSB 4 bits of G_n, and the values a and b are positive integers, and ${}_4[G_n]\gg 3$ functions such that binary data of the computed ${}_4[G_n]_2$ are shifted in the right direction by 3 bits, and as a result, it functions as division by 2^3.

[0153] Also in the case a high speed computation is difficult as the pixel frequency becomes higher according to the resolution, even the gray data G_n of the present frame can be modified omitting some LSBs. In the case of modifying respective 6 bits of G_n and G_{n-1}, the conversion is as follows.

Equation 15 $$G_n' = f([G_n]_4,[G_{n-1}]_4)+a\cdot([G_n]_4,[G_{n-1}]_4)\cdot\frac{{}_4[G_n]\gg 2}{4}-b\cdot([G_n]_4,[G_{n-1}]_4)\cdot\frac{{}_4[G_n]\gg 2}{4}$$

[0154] As described above, a gray lookup table of p bits is used, and in the case of modifying only q-bit Gn and r-bit Gn-1, it is as follows (q, r > p.)

Equation 16 $$G_n' = f([G_n]_{8-p}, [G_{n-1}]_{8-p}) + a\cdot([G_n]_{8-p}, [G_{n-1}]_{8-p})\cdot\frac{{}_p[G_n]_{8-q}\gg(8-q)}{2^{(q-p)}}$$
$$-b\cdot([G_n]_{8-p}, [G_{n-1}]_{8-p})\cdot\frac{{}_p[G_n]_{8-r}\gg(8-r)}{2^{(r-p)}}$$

[0155] An operation of an LCD having a function of a moving picture modification will now be described.

[0156] As described above, in order to remove a lagging effect of moving pictures, image signals G_n of a frame are modified compared to the image signals G_{n-1} of a previous frame and using the equations 17 to 20.

Equation 17 $$G_n' = G_n, \text{ if } G_n = G_{n-1}$$

Equation 18 $$G_n' > G_n, \text{ if } G_n > G_{n-1}$$

Equation 19 $$G_n' < G_n, \text{ if } G_n < G_{n-1}$$

Equation 20 $$G_n' - G_n \propto G_n - G_{n-1}$$

[0157] That is, when the image signals provided by the present frame are identical with that of the previous frame, no modification is executed as shown in Equation 17, and when the present gray signal (or gray voltage) becomes higher than the previous one, the modification circuit raises the present gray (or gray voltage) and outputs the same as shown in FIG. 18, and when the present gray signal (or gray voltage) becomes lower than the previous one, the modification circuit lowers the present gray (or gray voltage) and outputs the same as shown in FIG. 19. At this time, states of the modification are proportional to the difference between the present gray (or gray voltage) and the previous one as shown in the equation 20.

[0158] Via the above-described modification process, the response speed of the LCD panel becomes faster based on the following reasons.

[0159] First, desired voltage is supplied. That is, if a person wishes to supply 5V to liquid crystal cells, the actual 5V is supplied to the cells. When the liquid crystal reacts to the electric field and the direction of the director of the liquid crystal is changed, the capacitance is also changed, and accordingly, the voltage different from the previous one is supplied to the liquid crystal.

[0160] That is, even when the response speed of the liquid crystal is within one frame (16.7ms, @60Hz), the conventional AMLCD driving method does not provide accurate voltages according to the above-noted mechanism and but the voltage between the previous and present voltages, and accordingly, the actual response speed of the LCD panel is delayed more than the one frame.

[0161] The desired voltage is generated according to the signal modification and therefore correct response is performed. At this time, transmission errors during the response time of the liquid crystal can be compensated by performing an overcompensation.

[0162] Second, the response speed of the liquid crystal material generally becomes faster as the voltage is greatly varied. For example, in the case of rising, the response speed is faster when the voltage is switched-from 1V to 3V than when the voltage is switched from 1V to 2V, and in the case of falling, the response speed is faster when the voltage is switched from 3V to 1V than when the voltage is switched from 3V to 2V. This tendency is preserved in most cases even though there are some differences depending on the liquid crystal or the driving modes of the LCD. For example, in the case of the twisted nematic mode, the response speed of the rising becomes 15 times faster and that of the falling becomes 1.5 times faster as the voltage difference becomes greater.

[0163] Third, in the case the response speed of the liquid crystal is greater than one frame (16.7ms), the response time can be lowered to one frame by using a forced traction method. It is assumed that there is a liquid crystal that has a response time of 30ms when the voltage is changed from 1V to 2V. In other words, in order to obtain the transmission corresponding to 2V, 30ms of time is needed when 2V voltage is supplied.

[0164] When it is assumed that a time for the identical liquid crystal to reach 3V from 1V is also 30ms (in most cases, the time is shorter than this case), the transmission reaches its target transmission corresponding to 2V before 30ms. That is, when supplying 3V in order to obtain desired transmission corresponding to 2V, the transmission reaches its target transmission corresponding to 2V in a time shorter than 30ms.

[0165] When continuously supplying 3V, the liquid crystal reaches 3V, and accordingly, the access voltage is cut off when the voltage reaches 2V, and when 2V is supplied, the liquid crystal reaches 2V in a time shorter than 30ms. A time to cut off the voltage, that is, to switch the voltage is when the frame is switched. Therefore, if the voltage of the liquid crystal reaches 2V after a single frame (16.7ms), for example, 3V voltage is supplied and it becomes to 2V at a subsequent frame, the response time becomes 16.7ms. In this case, the transmission errors during the response time (e.g., 16.7ms) of the liquid crystal can be set off using the compensation method.

[0166] According to the above-noted embodiment of the present invention, as described above, the pixel voltage can reach the target voltage level by modifying the data voltage and supplying the modified data voltage to the pixels. Hence, the response speed of the liquid crystal can be improved without modification of the configuration of the TFT LCD panel.

[0167] Also, in the case of driving the LCD and particularly in the case of implementation of the moving pictures, the size of the gray lookup table of the image signal modification circuit for enhancing the response speed of the liquid crystal can be reduced and the quantization errors can be removed.

[0168] While this invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

[0169] Where technical features mentioned in any claim are followed by reference signs, those reference signs have been included for the sole purpose of increasing the intelligibility of the claims and accordingly, such reference signs do not have any limiting effect on the scope of each element identified by way of example by such reference signs.

Claims

1. , A liquid crystal display (LCD) comprising:

   a data gray signal modifier for receiving gray signals from a data gray signal source, and outputting modification gray signals by consideration of gray signals of present and previous frames;
   a data driver for changing the modification gray signals into corresponding data voltages and outputting image signals;
   a gate driver for sequentially supplying scanning signals; and
   an LCD panel comprising a plurality of gate lines for transmitting the scanning signals; a plurality of data lines, being insulated from the gate lines and crossing them, for transmitting the image signals; and a plurality of pixels, formed by an area surrounded by the gate lines and data lines and arranged as a matrix pattern, having switching elements connected to the gate lines and data lines.

2. The LCD of claim 1, wherein the data gray signal modifier comprises:

   a frame storage device for receiving the gray signals from the data gray signal source, storing the gray signals during a single frame, and outputting the same;
   a controller for controlling writing and reading the gray signals of the frame storage device; and
   a data gray signal converter for considering the gray signals of a present frame transmitted by the data gray signal source and the gray signals of a previous frame transmitted by the frame storage device, and outputting the modification gray signals.

3. The LCD of claim 2, wherein a clock signal frequency synchronized with the gray signal provided by the data gray signal source is identical with that synchronized with the controller.

4. The LCD of claim 2, wherein a clock signal frequency synchronized with the gray signal provided by the data gray signal source is different from that synchronized with the controller.

5. The LCD of claim 4, wherein the LCD further comprises:

   a combiner for receiving the gray signals from the data gray signal source, combining the gray signals to be synchronized with the clock signal frequency with which the controller is synchronized, and outputting the combined gray signals to the frame storage device and the data gray signal converter; and
   a divider for dividing the gray signals output by the data gray signal converter so as to be synchronized with the frequency with which the gray signals transmitted by the data gray signal source are synchronized.

6. The LCD of claim 2, wherein the data gray signal modifier modifies the gray signals so as to output a modification data voltage V_n' that satisfies the following equation

$$|V_n'| = |V_n| + f(|V_n| - |V_{n-1}|)$$

   where the data voltage of the present frame is set to be V_n and that of the previous frame to be V_{n-1}.

7. The LCD of claim 6, wherein the data gray signal converter uses a digital circuit to output modified gray signals that satisfy the above-noted equation.

8. The LCD of claim 2, wherein the data gray signal converter comprises a storage device for storing a lookup table for writing modification gray signals corresponding to the gray signals of the present and previous frames.

9. The LCD of claim 8, wherein when the modification gray signal is greater than a first voltage, the lookup table sets the modification gray signal as the first voltage, and when the modification gray signal is less than a second voltage, the lookup table sets the same as the second voltage.

10. The LCD of claim 1, wherein the data gray signal modifier receives n-bit gray signals with respect to red R, green G and blue B signals from the data gray signal source, and outputs modification gray signals by considering the m-bit gray signals of the present and previous frames among n-bit gray signals.

11. The LCD of claim 10, wherein the data gray signal modifier comprises:

a frame storage device for receiving the m-bit gray signals from the data gray signal source, storing the gray signals during a single frame, and outputting the same;
a controller for controlling writing and reading the gray signals of the frame storage device; and
a data gray signal converter for considering the m-bit gray signals of a present frame transmitted by the data gray signal source and the gray signals of a previous frame transmitted by the frame storage device, and generating and outputting the modification gray signals.

12. The LCD of claim 11, wherein the number 'm' represents remaining bits obtained by a subtraction of bits from the least significant bit (LSB) to 'I' (i=0, 1, ..., n-1) among the 'n' bits of the gray signals.

13. The LCD of claim 11, wherein the number 'm' is varied according to R, G and B.

14. The LCD of claim 13, wherein the number 'm' is the biggest with respect to B.

15. The LCD of claim 13, wherein the number 'm' is the smallest with respect to G.

16. The LCD of claim 11, wherein the data gray signal converter receives unmodified (n-m) bits among the n-bit gray signals received from the data gray signal source, adds the received (n-m) bits to the gray signals generated by considering the gray signals of the present and previous frames, and generates n-bit modification gray signals.

17. The LCD of claim 11, wherein the frame storage device comprises:

a first frame storage device that writes outputs of the m-bit odd-numbered gray signals of the data gray signal source and reads outputs of the m-bit even-numbered gray signals; and
a second frame storage device that reads the outputs of the m-bit odd-numbered gray signals of the data gray signal source and writes the outputs of the m-bit even-numbered gray signals.

18. The LCD of claim 11, wherein the data gray signal converter modifies the gray signals so as to output a modification data voltage V_n' that satisfies the following equation

$$|V_n'| = |V_n| + f(|V_n| - |V_{n-1}|)$$

where the data voltage of the present frame is set to be V_n and that of the previous frame to be V_{n-1}.

19. The LCD of claim 18, wherein the data gray signal converter uses a digital circuit to output modified gray signals that satisfy the above-noted equation.

20. The LCD of claim 11, wherein the data gray signal converter comprises a storage device for storing a lookup table for writing modification gray signals corresponding to the gray signals of the present and previous frames.

21. The LCD of claim 20, wherein when the modification gray signal is greater than a first voltage, the lookup table sets the modification gray signal as the first voltage, and when the modification gray signal is less than a second voltage, the lookup table sets the same as the second voltage.

22. The LCD of claim 1, wherein the data gray signal modifier receives x-bit gray data with respect to R, G and B from the data gray signal source and performs a first modification on a predetermined MSB bits of the respective x-bit gray data of the present and previous frames by using the lookup table, performs a second modification on respective remaining bits of the gray data of the present and previous frames via a predetermined computation, and outputs modification gray data via the first and second modifications.

23. The LCD of claim 22, wherein the data gray signal modifier comprises:

    a frame storage device for receiving the x-bit gray data from the data gray signal source, storing the gray data during a single frame, and outputting the same;
    a controller for controlling writing and reading the gray data of the frame storage device; and
    a data gray signal converter for considering the x-bit gray data of a present frame transmitted by the data gray signal source and the gray data of a previous frame transmitted by the frame storage device, generating modification gray data and outputting the same to the data driver.

24. , The LCD of claim 23, wherein the data gray signal converter comprises:

    a lookup table for respectively receiving MSB y-bit data of the x-bit data of the previous and present image data, and outputting variables (f, a, b) for a modification of moving pictures; and
    a calculator for respectively receiving LSB z-bit data of the x-bit data of the previous and present image data, receiving the variables (f, a, b) and outputting the modified gray data.

25. The LCD of claim 24, wherein the modified gray data G_n are obtained using the subsequent equation:

$$G_n' = f([G_n]_z, [G_{n-1}]_z) + a([G_n]_z, [G_{n-1}]_z) \cdot \frac{{}_y[G_n]}{2^z} - b([G_n]_z, [G_{n-1}]_z) \cdot \frac{{}_y[G_n]}{2^z}$$

where z=x-y, $[G_n]_z$ represents that zeros are provided to all the LSB z bits of Gn, $[G_{n-1}]_z$ represents that zeros are provided to all the LSB z bits of G_{n-1}, ${}_y[G_n]$ represents that zeros are provided to all the MSB y bits of G_n, and a and b are positive integers.

26. The LCD of claim 24, wherein the modified gray data G_n are obtained using the subsequent equation:

$$G_n' = f' + [G_n]_z + a \cdot ([G_n]_z, [G_{n-1}]_z) \cdot \frac{{}_y[G_n]}{2^z} - b \cdot ([G_n]_z, [G_{n-1}]_z) \cdot \frac{{}_y[G_n]}{2^z}$$

where it is defined that z=x-y, $f'=f([G_n]_z,[G_{n-1}]_z)-[G_n]_z$, and $[G_n]_z$ represents that zeros are provided to all the LSB z bits of G_n, and $[G_{n-1}]_z$ represents that zeros are provided to all the LSB z bits of G_{n-1}, and ${}_y[G_n]$ represents that zeros are provided to all the MSB y bits of G_n, and the values a and b are positive integers.

27. The LCD of claim 24, wherein the modified gray data G_n are obtained using the subsequent equation:

$$G'_n = f'([G_n]_z,[G_{n-1}]_z)+G_n+a' \cdot ([G_n]_z,[G_{n-1}]_z) \cdot \frac{{}_y[G_n]}{2^z} - b \cdot ([G_n]_z,[G_{n-1}]_z) \cdot \frac{{}_y[G_n]}{2^z}$$

where it is defined that z=x-y, $f'=f-G_n$, and $[G_n]_z$ represents that zeros are provided to all the LSB z bits of G_n, and $[G_{n-1}]_z$ represents that zeros are provided to all the LSB z bits of G_{n-1}, and ${}_y[G_n]$ represents that zeros are provided to all the MSB y bits of G_n, and the value a is an integer, and the value b is a positive integer.

28. The LCD of claim 25, wherein if a-b=16 in the case $[G_n]_z=[G_{n-1}]_z$, the condition that $G_n = G_{n-1}$ is satisfied.

29. The LCD of claim 27, wherein if a-b=0 in the case $[G_n]_z=[G_{n-1}]_z$, the condition that $G_n = G_{n-1}$ is satisfied.

30. In a liquid crystal display (LCD) driving method comprising a plurality of gate lines; a plurality of data lines being insulated from the gate lines and crossing them; and a plurality of pixels, formed by an area surrounded by the

gate lines and data lines and arranged as a matrix pattem, having switching elements connected to the gate lines and data lines, an LCD driving method comprising:

(a) sequentially supplying scanning signals to the gate lines;
(b) receiving image signals from a image signal source, and generating modification image signals by considering image signals of present and previous frames; and
(c) supplying data voltages corresponding to the generated modification image signals to the data lines.

31. The LCD driving method of claim 30, wherein the image signals are identified as analog voltages.

32. The LCD driving method of claim 30, wherein the image signals are identified as digital gray signals.

33. The LCD driving method of claim 32, wherein the (b) comprises:

delaying the image signals transmitted from the image signal source by as much as a single frame;
generating modification image signals by considering the image signals of the present frame received from the image signal source and the delayed image signals of the previous frame.

34. The LCD driving method of claim 30, wherein the modification image signals satisfy the following equation

$$|V_n'| = |V_n| + f(|V_n| - |V_{n-1}|)$$

where the data voltage of the present frame is set to be V_n and that of the previous frame to be V_{n-1}.

35. The LCD driving method of claim 33, wherein in the (b), a lookup table for writing modification image signals corresponding to the image signals of the previous and present frames is searched and the modification image signals are generated.

36. The LCD driving method of claim 35, wherein when the modification image signals are greater than a first voltage, the lookup table sets the modification image signals as the first voltage, and when the modification image signals are less than a second voltage, the lookup table sets the modification image signals as the second voltage.

37. In a liquid crystal display (LCD) driving method comprising a plurality of gate lines; a plurality of data lines being insulated from the gate lines and crossing them; and a plurality of pixels, formed by an area surrounded by the gate lines and data lines and arranged as a matrix pattern, having switching elements connected to the gate lines and data lines, an LCD driving method comprising:

(a) sequentially supplying scanning signals to the gate lines;
(b) receiving n-bit gray signals from a data gray signal source, and generating modification gray signals by considering respective m-bit gray signals of present and previous frames among the n-bit gray signals; and
(c) supplying data voltages corresponding to the generated modification gray signals to the data lines.

38. The LCD driving method of claim 37, wherein the (b) comprises:

(b-1) delaying the m-bit gray signals among the n-bit gray signals transmitted from the data gray signal source by as much as a single frame;
(b-2) generating first m-bit modification gray signals by considering the m-bit gray signals of the present frame received from the data gray signal source and the m-bit delayed gray signals of the previous frame; and
(b-3) adding the unmodified and passed (n-m) bits to the first m-bit modification gray signals, and generating second n-bit modification gray signals.

39. The LCD driving method of claim 38, wherein the number 'm' represents remaining bits obtained by a subtraction of bits from the least significant bit (LSB) to 'i' (i=0, 1, ..., n-1) among the n-bit gray signals.

40. The method of claim 39, wherein the number 'm' is varied according to red (R), green (G) and blue (B).

41. The method of claim 40, wherein the number 'm' is the biggest with respect to the B.

42. The method of claim 40, wherein the number 'm' is the smallest with respect to the G.

43. The method of claim 37, wherein the modification gray signal satisfies the following equation

$$|V_n| = |V_n| + f(|V_n| - |V_{n-1}|)$$

where the data voltage of the present frame is set to be V_n and that of the previous frame to be V_{n-1}.

44. The method of claim 38, wherein in the (b-2), a look-up table that writes modification gray signals corresponding to the respective m-bit gray signals of previous and present frames is searched and first modification gray signals are then generated.

45. The method of claim 44, wherein when the modification gray voltage is greater than a first voltage, the lookup table sets the modification data voltage as the first voltage, and when the modification data voltage is lesser than the second voltage, the lookup table sets the modification data voltage as the second voltage.

46. In a liquid crystal display (LCD) driving method comprising a plurality of gate lines; a plurality of data lines being insulated from the gate lines and crossing them; and a plurality of pixels, formed by an area surrounded by the gate lines and data lines and arranged as a matrix pattern, having switching elements connected to the gate lines and data lines, an LCD driving method comprising:

(a) sequentially supplying scanning signals to the gate lines;
(b) receiving x-bit image gray data from an outer image signal source;
(c) delaying the image gray data by a single frame;
(d) extracting variables for a modification of the moving pictures from the lookup table by using MSB y bits of a single-frame delayed digital gray data and MSB y bits of the digital gray data received at the present frame;
(e) computing LSB (x-y) bits of the single-frame delayed digital gray data, LSB (x-y) bits of the digital gray data received at the present frame, and the variables extracted from the (d); and
(f) supplying the data voltage corresponding to the modified gray data to the data line.

47. The LCD driving method of claim 46, wherein the modified gray data G_n is obtained according to the subsequent equation:

$$G_n' = f([G_n]_z,[G_{n-1}]_z)+a([G_n]_z,[G_{n-1}]_z)\cdot\frac{{}_y[G_n]}{2^z}-b([G_n]_z,[G_{n-1}]_z)\cdot\frac{{}_y[G_n]}{2^z}$$

where z=x-y, $[G_n]_z$ represents that zeros are provided to all the LSB z bits of Gn, $[G_{n-1}]_z$ represents that zeros are provided to all the LSB z bits of G_{n-1}, ${}_y[G_n]$ represents that zeros are provided to all the MSB y bits of G_n, and a and b are positive integers.

48. The LCD driving method of claim 46, wherein the modified gray data G_n are obtained using the subsequent equation:

$$G_n' = f'+[G_n]_z+a\cdot([G_n]_z,[G_{n-1}]_z\cdot\frac{{}_y[G_n]}{2^z}-b\cdot([G_n]_z,[G_{n-1}]_z)\cdot\frac{{}_y[G_n]}{2^z}$$

where it is defined that z=x-y, $f'=f([G_n]_z, [G_{n-1}]_z)-[G_n]_z$, and $[G_n]_z$ represents that zeros are provided to all the LSB z bits of G_n, and $[G_{n-1}]_z$ represents that zeros are provided to all the LSB z bits of G_{n-1}, and ${}_y[G_n]$ represents that zeros are provided to all the MSB y bits of G_n, and the values a and b are positive integers.

49. The LCD driving method of claim 46, wherein the modified gray data G_n are obtained using the subsequent equation:

$$G_n' = f'([G_n]_z, [G_{n-1}]_z + G_n + a'\cdot([G_n]_z, [G_{n-1}]_z)\cdot\frac{{}_y[G_n]}{2^z} - b\cdot([G_n]_z, [G_{n-1}]_z)\cdot\frac{{}_y[G_n]}{2^z}$$

where it is defined that z=x-y, f'=f-G_n, and $[G_n]_z$ represents that zeros are provided to all the LSB z bits of G_n, and $[G_{n-1}]_z$ represents that zeros are provided to all the LSB z bits of G_{n-1}, and ${}_y[G_n]$ represents that zeros are provided to all the MSB y bits of G_n, and the value a is an integer, and the value b is a positive integer.

50. The LCD driving method of claim 47, wherein if a-b=16 in the case $[G_n]_z=[G_{n-1}]_z$, the condition that $G_n = G_{n-1}$ is satisfied.

51. The LCD driving method of claim 49, wherein if a-b=0 in the case $[G_n]_z=[G_{n-1}]_z$, the condition that $G_n = G_{n-1}$ is satisfied.

52. In a liquid crystal display (LCD) driving apparatus comprising a plurality of gate lines; a plurality of data lines being insulated from the gate lines and crossing them; and a plurality of pixels, formed by an area surrounded by the gate lines and data lines and arranged as a matrix pattern, having switching elements connected to the gate lines and data lines, an LCD driving apparatus comprising:

a data gray signal modifier for receiving x-bit gray signals from a data gray signal source, performing a first modification on predetermined MSBs of respective x-bit gray data of the present and previous frames by using a lookup table, performing a second modification on respective remaining bits of gray data of the present and previous frames via a predetermined computation, and outputting modification gray signals via the first and second modifications;
a data driver for changing the modification gray signals output from the data gray signal modifier into data voltages corresponding to the modification gray data and outputting image signals to the data lines; and
a gate driver for sequentially supplying scanning signals to the gate lines.

53. The LCD driving apparatus of claim 52, wherein the data gray signal modifier comprises:

a frame storage device for receiving the x-bit gray data from the data gray signal source, storing the gray data during a single frame, and outputting the same;
a controller for controlling writing and reading the gray data of the frame storage device; and
a data gray signal converter for considering the x-bit gray data of a present frame transmitted by the data gray signal source and the x-bit gray data of a previous frame transmitted by the frame storage device, generating the modification gray data and outputting the same to the data driver,

54. The LCD driving apparatus of claim 53, wherein the data gray signal converter comprises:

a lookup table for respectively receiving MSB y-bit data of the x-bit image data of the previous and present frames, and outputting variables (f, a, b) for a modification of moving pictures; and
a calculator for respectively receiving LSB z-bit data of the x-bit data of the previous and present image data, receiving the variables (f, a, b) and outputting the modified gray data.

55. The LCD driving apparatus of claim 54, wherein the modified gray data G_n are obtained using the subsequent equation:

$$G_n' = f([G_n]_z, [G_{n-1}]_z) + a([G_n]_z, [G_{n-1}]_z)\cdot\frac{{}_y[G_n]}{2^z} - b([G_n]_z, [G_{n-1}]_z)\cdot\frac{{}_y[G_n]}{2^z}$$

where z=x-y, $[G_n]_z$ represents that zeros are provided to all the LSB z bits of Gn, $[G_{n-1}]_z$ represents that zeros are provided to all the LSB z bits of G_{n-1}, ${}_y[G_n]$ represents that zeros are provided to all the MSB y bits of G_n, and a and b are positive integers.

56. The LCD driving apparatus of claim 54, wherein the modified gray data G_n are obtained using the subsequent equation:

$$G_n' = f' + [G_n]_z + a\cdot([G_n]_z, [G_{n-1}]_z)\cdot\frac{{}_y[G_n]}{2^z} - b\cdot([G_n]_z, [G_{n-1}]_z)\cdot\frac{{}_y[G_n]}{2^z}$$

where it is defined that z=x-y, $f'=f([G_n]_z,[G_{n-1}]_z)-[G_n]_z$, and $[G_n]_z$ represents that zeros are provided to all the LSB z bits of G_n, and $[G_{n-1}]_z$ represents that zeros are provided to all the LSB z bits of G_{n-1}, and ${}_y[G_n]$ represents that zeros are provided to all the MSB y bits of G_n, and the values a and b are positive integers.

57. The LCD driving apparatus of claim 54, wherein the modified gray data G_n are obtained using the subsequent equation:

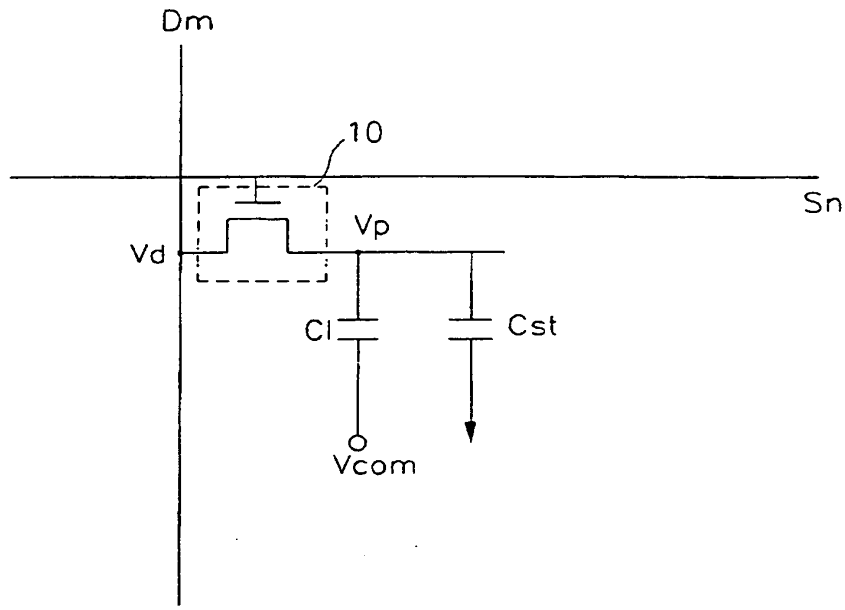
$$G_n' = f([G_n]_z, [G_{n-1}]_z) + G_n + a'\cdot([G_n]_z, [G_{n-1}]_z)\cdot\frac{{}_y[G_n]}{2^z} - b\cdot([G_n]_z, [G_{n-1}]_z)\cdot\frac{{}_y[G_n]}{2^z}$$

where it is defined that z=x-y, $f'=f-G_n$, and $[G_n]_z$ represents that zeros are provided to all the LSB z bits of G_n, and $[G_{n-1}]_z$ represents that zeros are provided to all the LSB z bits of G_{n-1}, and ${}_y[G_n]$ represents that zeros are provided to all the MSB y bits of G_n, and the value a is an integer, and the value b is a positive integer.

58. The LCD of claim 55, wherein if a-b=16 in the case $[G_n]_z=[G_{n-1}]_z$, the condition that $G_n = G_{n-1}$ is satisfied.

59. The LCD of claim 57, wherein if a-b=0 in the case $[G_n]_z=[G_{n-1}]_z$, the condition that $G_n = G_{n-1}$ is satisfied.

Fig. 1



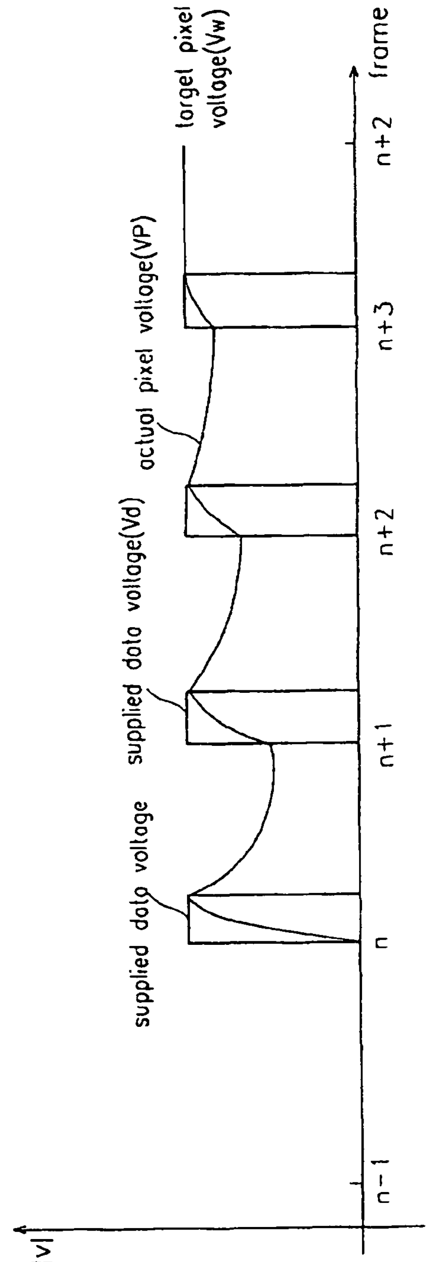

supplied data voltage
supplied data voltage(Vd)
actual pixel voltage(VP)
target pixel voltage(Vw)
|V|
frame
n-1
n
n+1
n+2
n+3
n+2

Fig.2

Fig.3

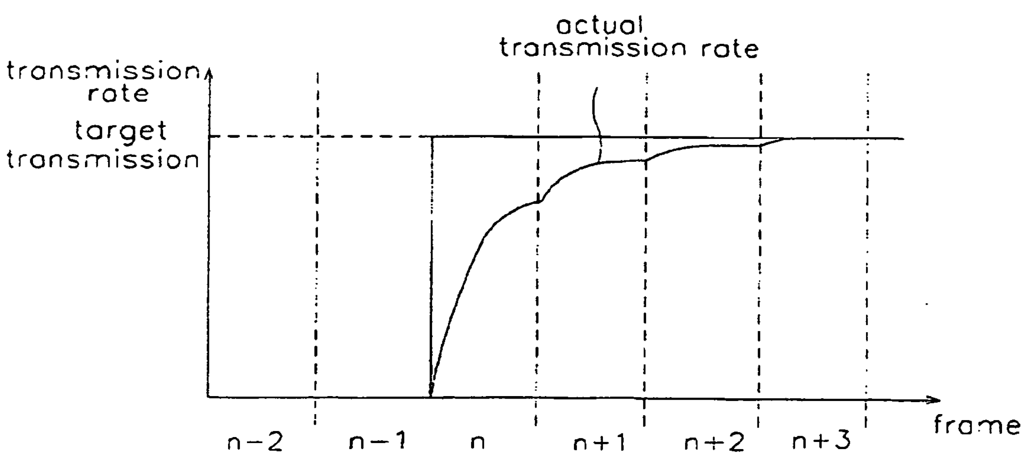

actual
transmission rate
transmission
rate
target
transmission
frame
n-2
n-1
n
n+1
n+2
n+3

Fig.4

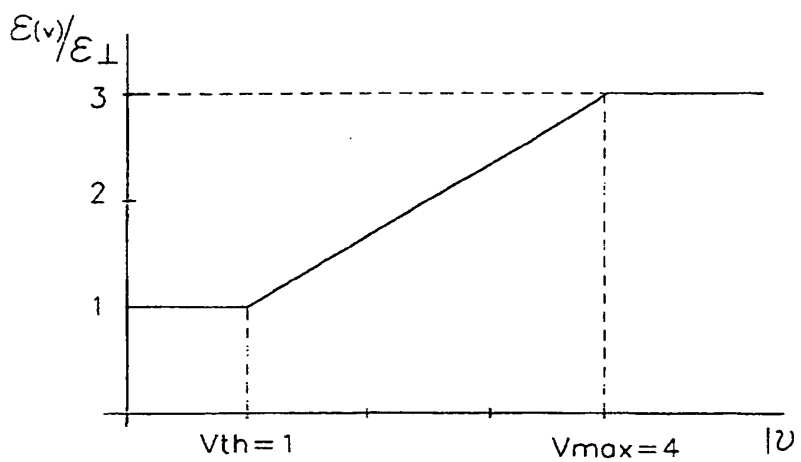


Fig.5

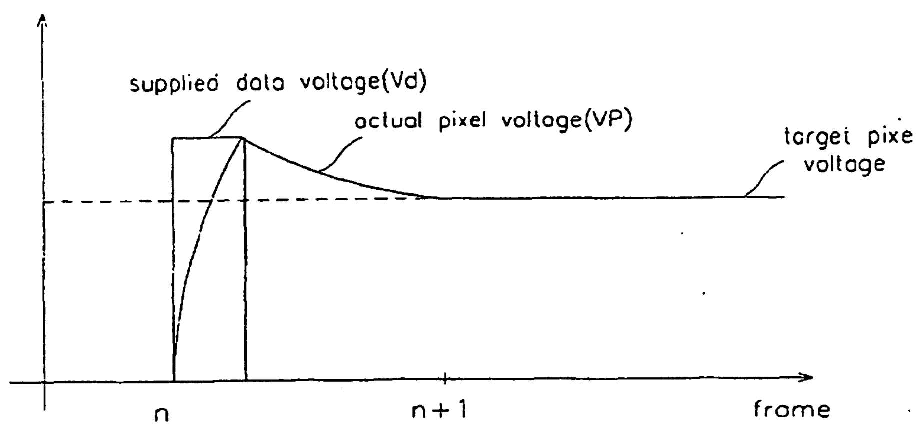

supplied data voltage(Vd)
actual pixel voltage(VP)
target pixel voltage
n
n+1
frame

Fig.6

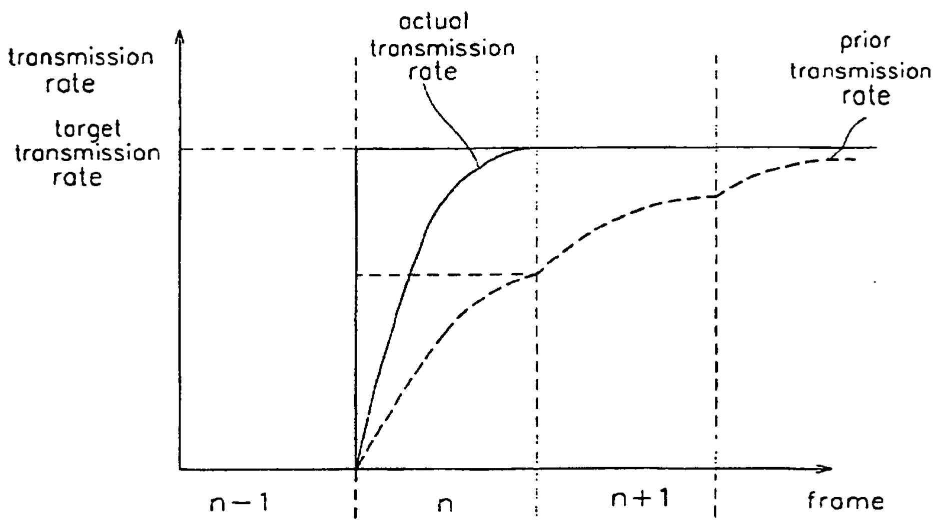

transmission rate
target transmission rate
actual transmission rate
prior transmission rate
n−1
n
n+1
frame

Fig.7

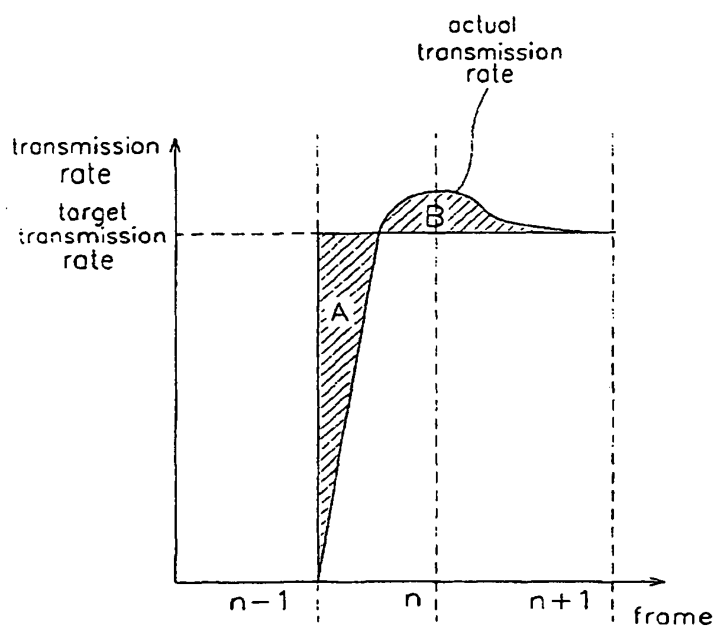

actual
transmission
rate
transmission
rate
target
transmission
rate
B
A
n−1
n
n+1
frame

Fig.8

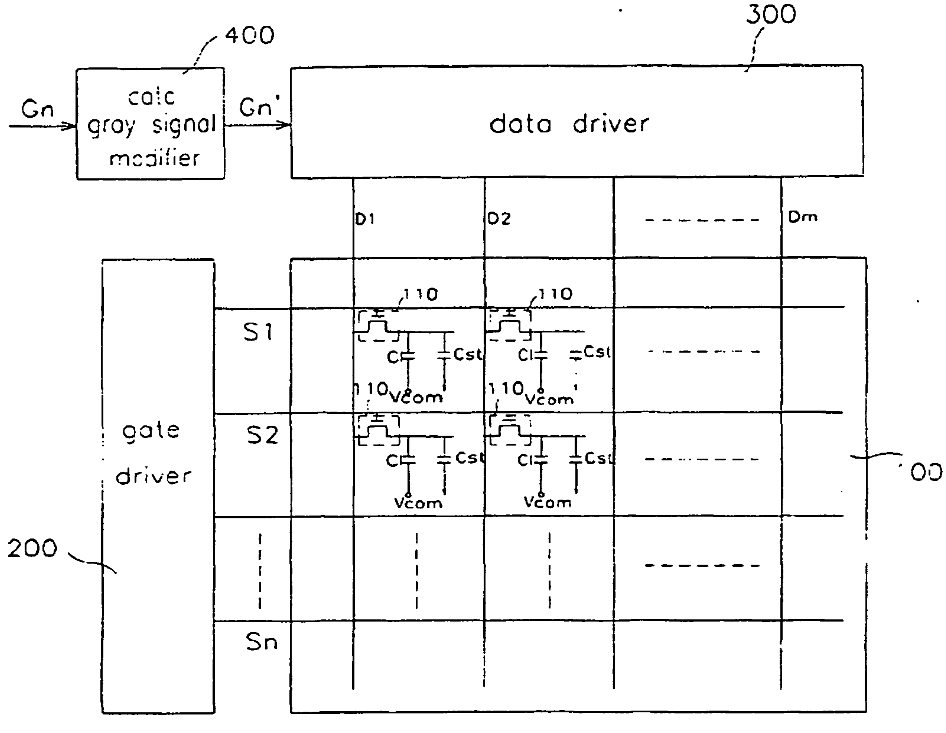

400
300
Gn
calc
gray signal
modifier
Gn'
data driver
D1
D2
Dm
110
S1
C1
Cst
Vcom
S2
gate
driver
200
Sn

Fig.9

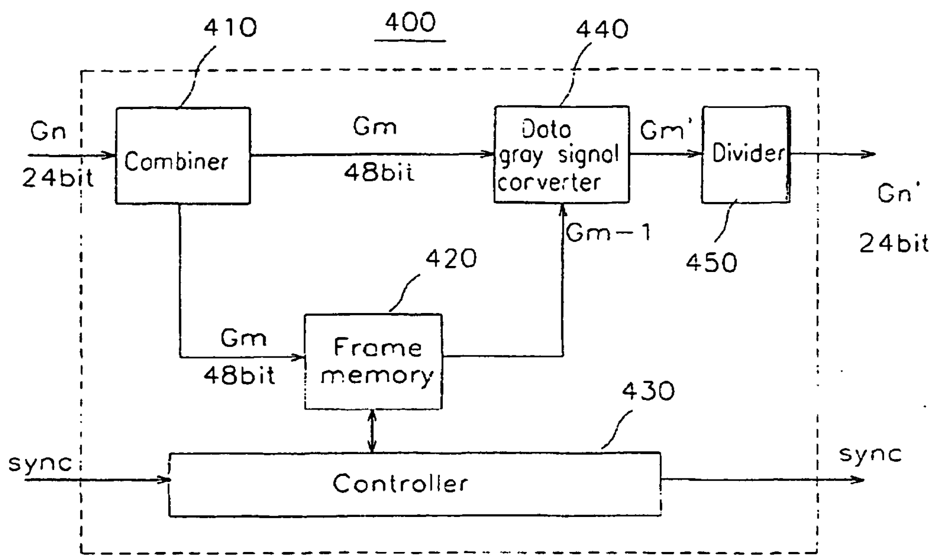

410
400
440
Gn
24bit
Combiner
Gm
48bit
Data gray signal converter
Gm'
Divider
Gn'
24bit
Gm-1
450
420
Gm
48bit
Frame memory
430
sync
Controller
sync

Fig. 10

Gn'		Gn							
		0	1	2	2	...	253	254	255
Gn-1	0	0	1	3	5	...	255	255	255
	1	0	1	3	4	...	255	255	255
	2	0	1	2	3	...	255	255	255
	3	0	0	2	3	...	255	255	255
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	253	0	0	0	0	...	253	254	255
	254	0	0	0	0	...	253	254	255
	255	0	0	0	0	...	252	253	255

Fig. 11

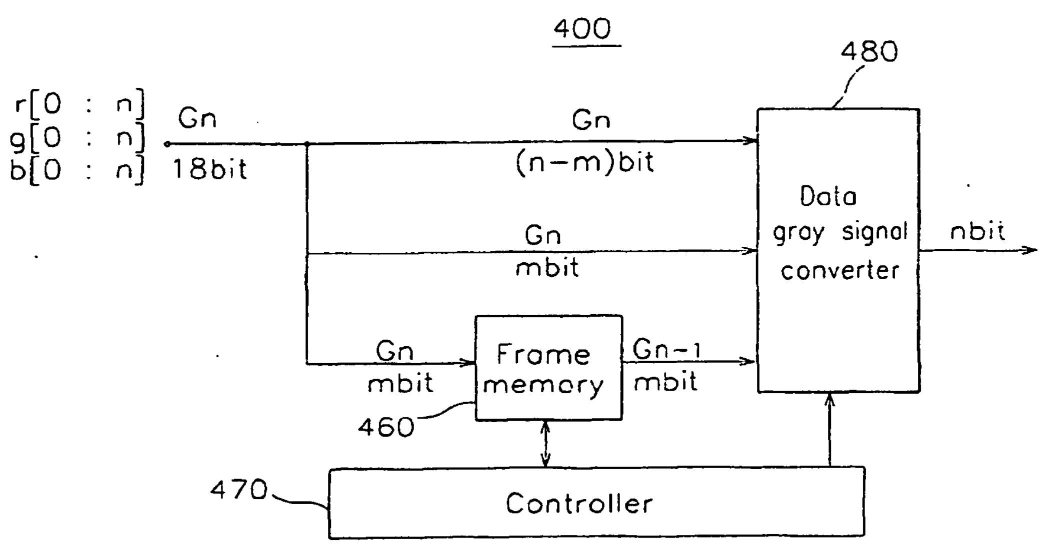

400
480
r[0 : n]
g[0 : n]
b[0 : n]
Gn
18bit
Gn
(n−m)bit
Data
gray signal
converter
Gn
mbit
nbit
Gn
mbit
Frame
memory
Gn-1
mbit
460
470
Controller

Fig.12

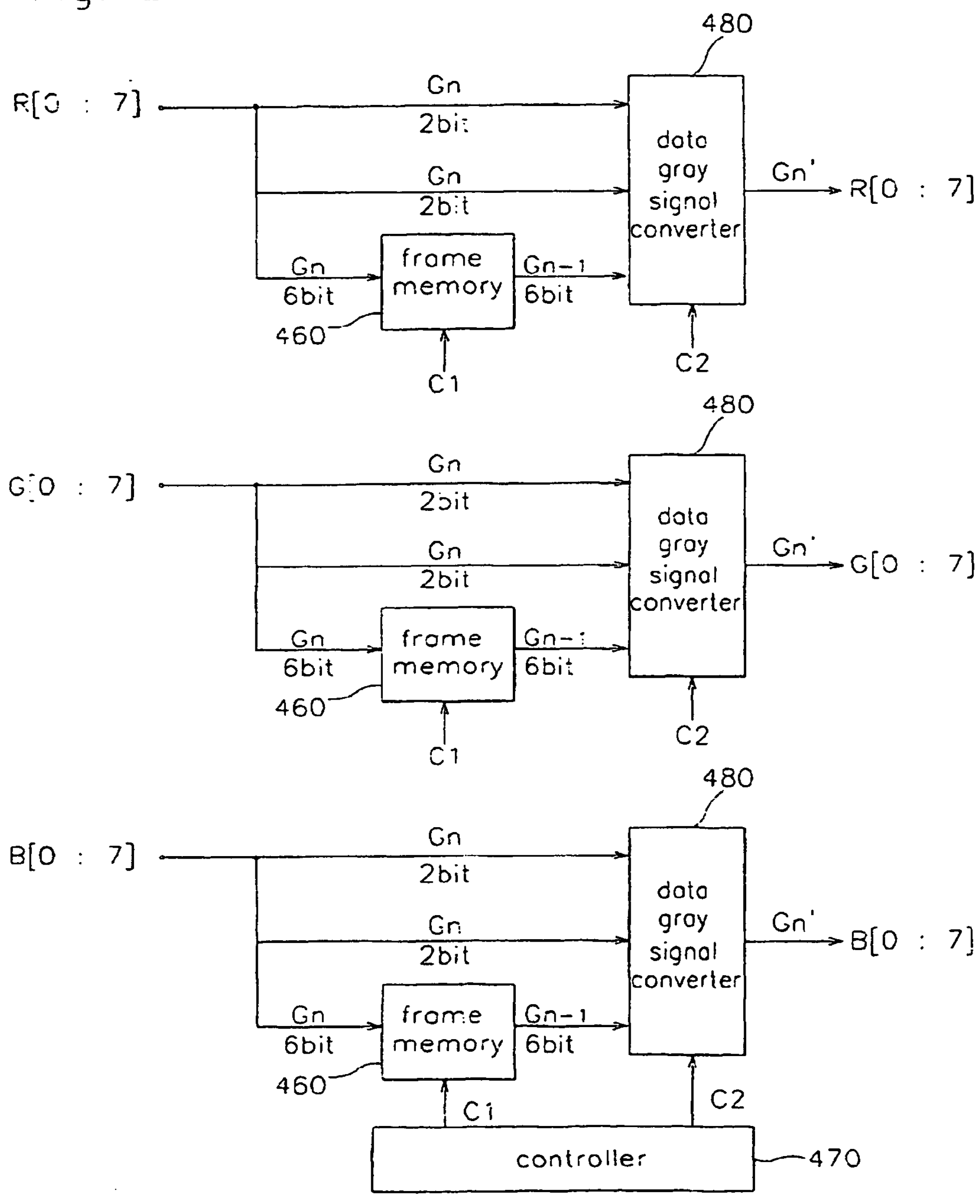

480
R[0 : 7]
Gn
2bit
Gn
2bit
data gray signal converter
Gn'
R[0 : 7]
Gn
6bit
frame memory
Gn-1
6bit
460
C1
C2
480
G[0 : 7]
Gn
2bit
Gn
2bit
data gray signal converter
Gn'
G[0 : 7]
Gn
6bit
frame memory
Gn-1
6bit
460
C1
C2
480
B[0 : 7]
Gn
2bit
Gn
2bit
data gray signal converter
Gn'
B[0 : 7]
Gn
6bit
frame memory
Gn-1
6bit
460
C1
C2
controller
470

Fig.13

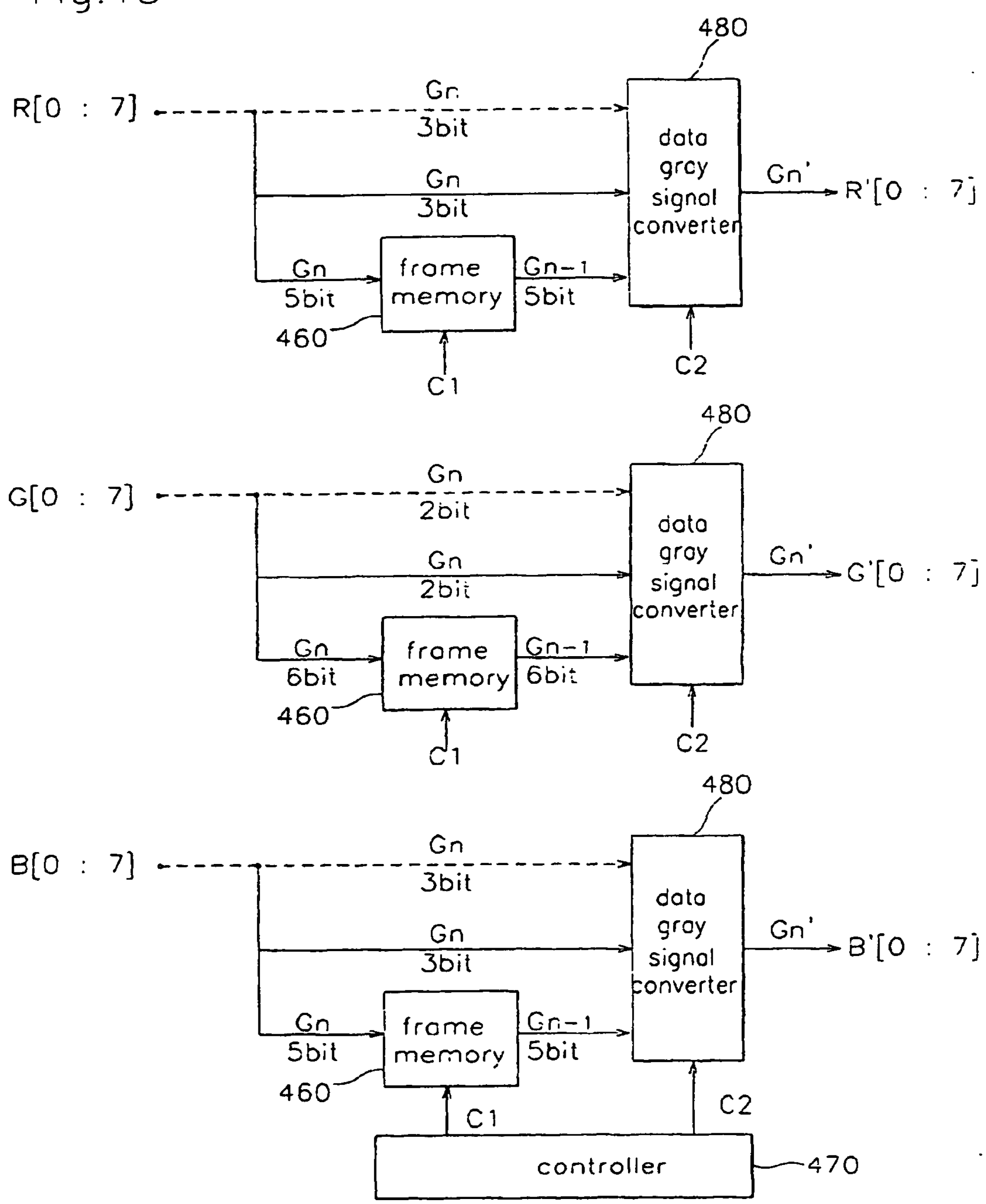

480
R[0 : 7]
Gn
3bit
Gn
3bit
data
gray
signal
converter
Gn'
R'[0 : 7]
Gn
5bit
frame
memory
Gn-1
5bit
460
C1
C2
480
G[0 : 7]
Gn
2bit
Gn
2bit
data
gray
signal
converter
Gn'
G'[0 : 7]
Gn
6bit
frame
memory
Gn-1
6bit
460
C1
C2
480
B[0 : 7]
Gn
3bit
Gn
3bit
data
gray
signal
converter
Gn'
B'[0 : 7]
Gn
5bit
frame
memory
Gn-1
5bit
460
C1
C2
controller
470

Fig.14

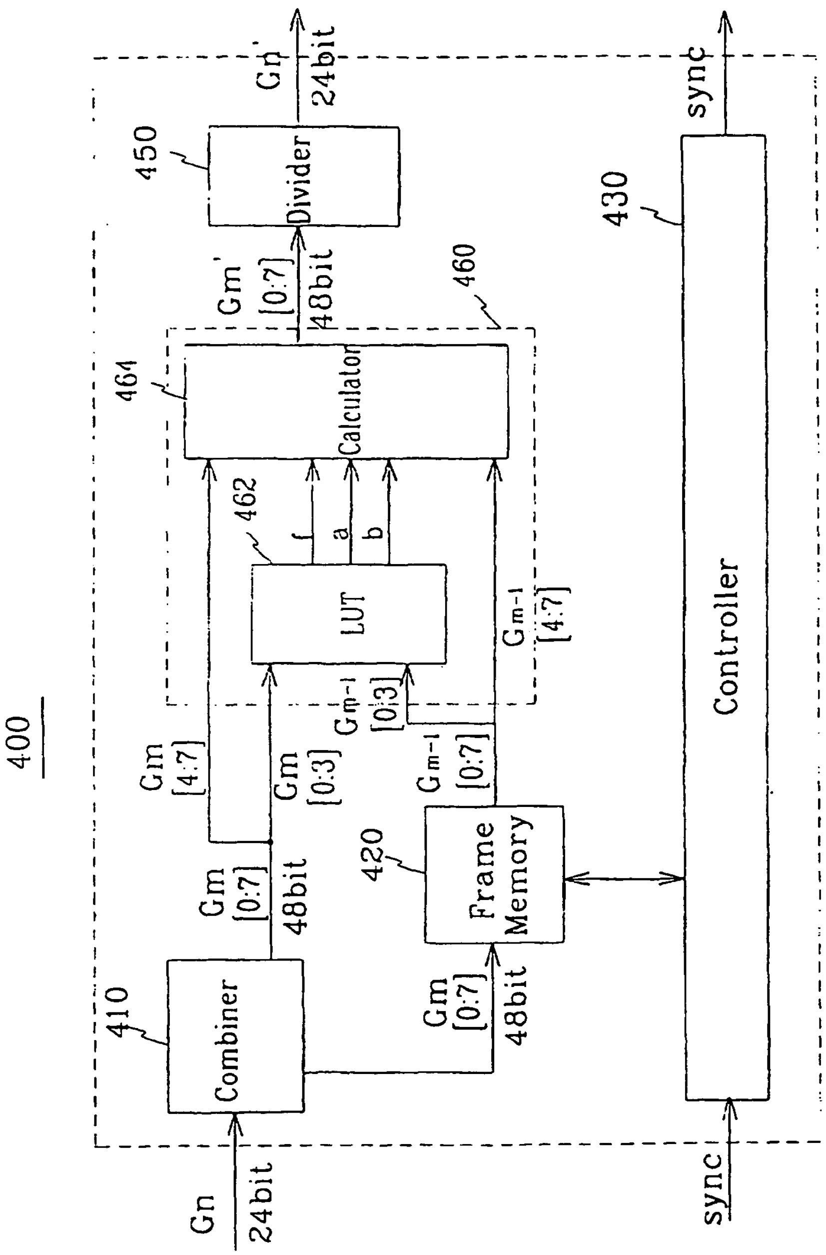

400
Gn
24bit
Combiner
410
Gm
[0:7]
48bit
Gm
[4:7]
Gm
[0:3]
Frame
Memory
420
Gm-1
[0:7]
Gm-1
[0:3]
LUT
462
f
a
b
Gm-1
[4:7]
Calculator
461
460
Gm'
[0:7]
48bit
Divider
450
Gn'
24bit
Controller
430
sync
sync

Fig. 15a

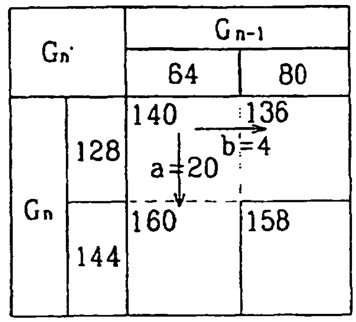


Fig. 15b

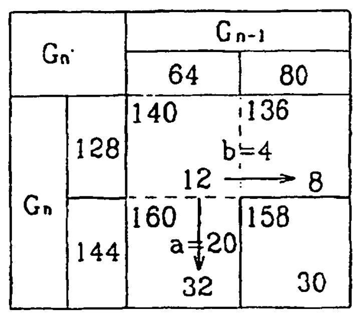


Fig. 15c

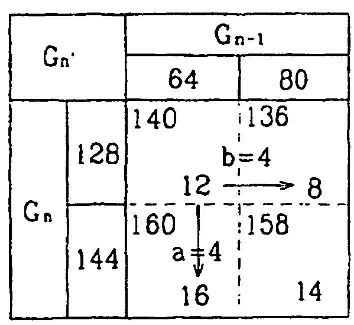
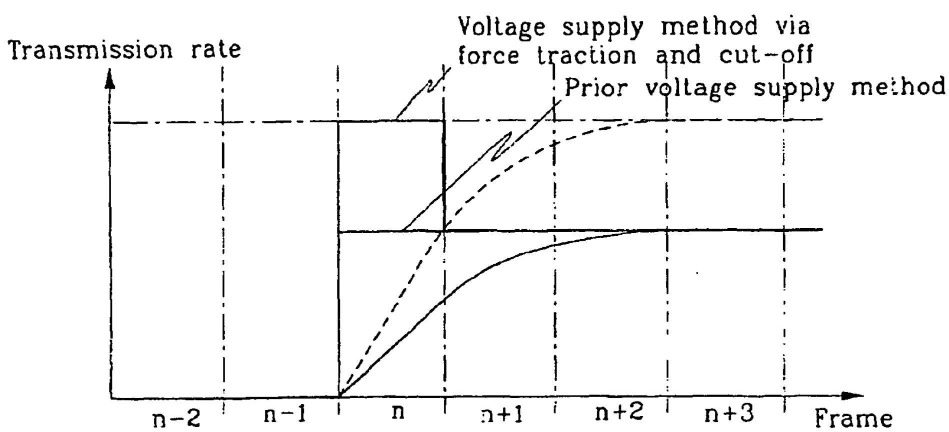


Fig.16


Transmission rate
Voltage supply method via force traction and cut-off
Prior voltage supply method
n-2
n-1
n
n+1
n+2
n+3
Frame

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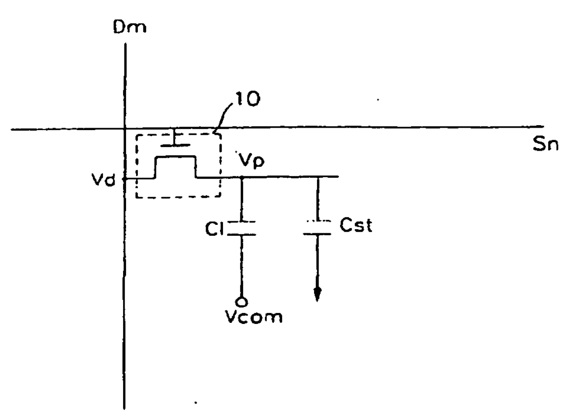
(54) **Liquid crystal display and driving method thereof**

(57) Disclosed is an LCD and driving method thereof. The present invention comprises a data gray signal modifier for receiving gray signals from a data gray signal source, and outputting modification gray signals by consideration of gray signals of present and previous frames; a data driver for changing the modification gray signals into corresponding data voltages and outputting image signals; a gate driver for sequentially supplying scanning signals; and an LCD panel comprising a plurality of gate lines for transmitting the scanning signals; a plurality of data lines, being insulated from the gate lines and crossing them, for transmitting the image signals; and a plurality of pixels, formed by an area surrounded by the gate lines and data lines and arranged as a matrix pattern, having switching elements connected to the gate lines and data lines.

Fig. 1



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EUROPEAN SEARCH REPORT

Application Number
EP 01 10 2227

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	EP 0 487 137 A (PHILIPS) 27 May 1992 (1992-05-27) * column 2, line 35 - line 38 * * page 3 - page 4 *	30	G09G3/36
A	EP 0 750 288 A (TOKYO SHIBAURA ELECTRIC) 27 December 1996 (1996-12-27) * column 14, line 42 - column 15, line 12; figure 12A *	1,30,37, 46,52	
A	WO 96 16393 A (PHILIPS) 30 May 1996 (1996-05-30) * abstract *	1,30,37, 46,52	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
			G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	28 June 2001	Lange, J

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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& : member of the same patent family, corresponding document

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 01 10 2227

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28-06-2001

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(54) A liquid crystal device and a method for driving the same.

(57) A liquid crystal device includes : a pair of substrates ; a liquid crystal layer interposed between the pair of substrates ; at least one polarizing element ; a plurality of pixels ; a retardation ($d \times \Delta n$) of the liquid crystal layer satisfying one of a relation :

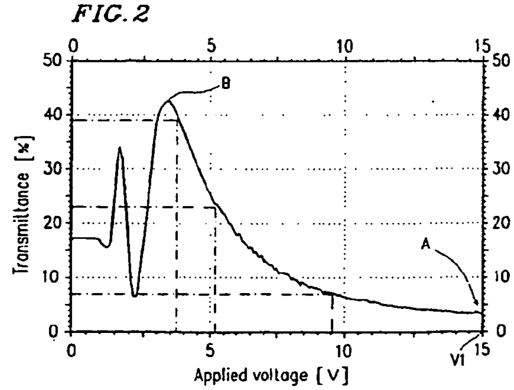
$$d \times \Delta n > \lambda/2$$

in a case where an incident light is output after passing through the liquid crystal layer once, and a relation :

$$2d \times \Delta n > \lambda/2$$

in a case where the incident light is outputted after passing through the liquid crystal layer twice, where a thickness of the liquid crystal layer is d, a birefringence is Δn and a wavelength of the light incident on the liquid crystal layer is λ ; and driving voltage supplying means for applying a driving voltage including a voltage higher than a maximum voltage providing an extremum of the output light intensity in a voltage-output light intensity characteristic of the pixels to the plurality of pixels.

FIG. 2



EP 0 660 297 A2

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to a liquid crystal device and a method for driving the same, more particularly to a liquid crystal device having a high response speed and a method for driving the same.

2. Description of the Related Art:

A conventional projection-type liquid crystal display device using a liquid crystal device is capable of obtaining a picture of a large size with relative ease by irradiating light onto a liquid crystal display so as to project the light onto a screen. There are two methods for obtaining a color display: a method in which a projected light beam is split into red, green and blue light beams, and a liquid crystal display device is used for each of the colors (simultaneous additive color mixing); and a method in which red, green and blue pixels are provided in a liquid crystal display device as in a direct-view type (juxtapositonal additive color mixing). However, both methods have problems. With the former method, while high resolution can be obtained with ease, it is expensive to realize such a liquid crystal display device. As shown in Figure **29**, light beams radiated from a lamp **1** as a light source propagate through three optical paths, that is, a dichroic mirror for a red light beam **2**, a dichroic mirror for a green light beam **3**, and a dichroic mirror for a blue light beam **4**. The light beams pass through liquid crystal panels **5**, **6** and **7**, respectively, and are output from a lens **8**. As described above, since the three liquid crystal display panels **5**, **6** and **7** are used, the optical system for projection becomes complex and large in size as a whole system. Moveover, if a defective pixel exists even in one liquid crystal display panel among the three, a bright spot with a single color or a mixed color occurs in the projected image at a portion corresponding to the defective pixel. On the other hand, while the latter method is inexpensive, it has a problem in that the quality of displayed image is deteriorated unless the size of red, green and blue pixels in a projected image is smaller than the spatial resolution of human eyes. As one of the methods for solving the above problem, a field sequential color mixing method, a color mixing method by using a field sepuential addressing method, is known which can display red, green and blue with one pixel. The characteristics of high precision and high brightness of the field sequential color mixing method have the following features.

(1) The principle of displaying color images by the field sequential color mixing method is the same as that by the simultaneous additive color mixing method. Therefore, the field sequential color mixing method provides high precision images.

(2) In the case where the liquid crystal panel has a defective pixel, the defective pixel is displayed as a white or black point. The white or black point is less conspicuous than the colored bright point. Accordingly, even if the defective pixel exists in the liquid crystal panel, the quality of the displayed image is not deteriorated.

(3) Full-color display or multi-color display can be realized with a single liquid crystal panel, and therefore the optical system can be miniaturized and lightened. Since it is not necessary to use a plurality of light shutters as in the simultaneous additive color mixing method, it is possible to miniaturize the system and lower the fabrication cost.

As described above, a compact and light color liquid crystal display device with high brightness and high precision, which is excellent in display quality, can be obtained with the use of the field sequential addressing method.

In the case of the field sequential addressing method, however, the time allowed for displaying images corresponding to each of Red, Green and Blue in one field is in the range of 5 to 6 msec. At the present time, the response time of Twisted Nematic (TN) mode used in an active matrix liquid crystal display device is approximately several tens msec. In the case of Figure **30**, the response times for rise and decay are 39.1 msec and 35.1 msec, respectively. Considering that the response time in a liquid crystal display mode, which utilizes optical switching between on/off states in the vicinity of a threshold voltage, is the same as or longer than that for the TN mode, it is practically impossible to realize the color liquid crystal display device of the field sequential addressing method.

As a conventional liquid crystal display mode having high-speed response, Surface Stabilized Ferroelectric Liquid Crystal (SSF-LC) mode is well-known (N.A.Clark and S.T.Lagerwall; Appl. Phys. Lett., 36,899: 1980). The feature of SSF-LC mode is as follows: the ferroelectric liquid crystal molecules have spontaneous polarization, and the display is performed by utilizing the property of the liquid crystal molecules which change their orientations so that the polarity of the spontaneous polarization and the polarity of an applied electric field are parallel with each other.

Regarding a liquid crystal display method with high-speed response other than the ferroelectric liquid crystal mode, Japanese Laid-Open Patent Publication No. 56-51352 describes that the response speed is increased by applying a voltage close to the threshold value and a voltage close to the saturation voltage at which an optical characteristic of the liquid crystal is saturated.

Another high-speed response display mode using nematic liquid crystal is described in a publication (Nematic liquid crystal modulator with response time less than 100 μs at room temperature: Shin-Tson Wu; Appl. Phys. Lett. 57(10), 3 1990). The method for driving the liquid crystal display described in the publication is shown in Figure **31**. A voltage (V_{off}) is continuously applied to the liquid crystal molecules such that the orientational deformation of the liquid crystal molecules from the initial orientation state becomes the largest. In this state, the transmittance of the liquid crystal display is zero. Then, zero voltage (V_0) is applied to the liquid crystal molecules such that the orientational deformation of the liquid crystal molecules is relaxed. The transmittance is changed by varying a time period for applying zero voltage, thereby obtaining a gray-scale display. The relaxation process of the liquid crystal molecules which are orientationally deformed is often compared to the movement of a spring. The potential energy due to the interaction of the liquid crystal molecules becomes higher as the degree of the orientational deformation of the liquid crystal molecules becomes larger. As a result, the liquid crystal molecules in the highly deformed orientation state relax with extremely high speed.

However, the conventional liquid crystal display mode using the ferroelectric liquid crystals (FLC mode), such as SSF-LC mode, suffers from the following problems. In addition to the difficulty in controlling the orientation of the ferroelectric liquid crystal molecules, the orientation of the molecules is easily destroyed by a mechanical shock. Moreover, since the orientation of the ferroelectric liquid crystals is in a bistable state, it is difficult to obtain the gray-scale display.

As for the driving method described in Japanese Laid-Open Patent Publication No. 56-51352, it is not capable of displaying gray-scale. Moreover, since the degree of the change in the orientation state of the liquid crystal molecules is large, it is difficult to increase the response speed higher than that for the TN mode.

The method in which the relaxation of the orientational deformation of liquid crystal molecules is adjusted by varying the voltage unapplied period in order to obtain the gray-scale display, such as the above-mentioned high-speed response display mode using the nematic liquid crystal, cannot be adopted to matrix driving used for commercial liquid crystal display devices and the like.

SUMMARY OF THE INVENTION

The liquid crystal device of this invention, includes:

a pair of substrates;

a liquid crystal layer interposed between the pair of substrates;

at least one polarizing element;

a plurality of pixels;

a retardation ($d \times \Delta n$) of the liquid crystal layer satisfying one of a relation:

$$d \times \Delta n > \lambda/2$$

in a case where an incident light is output after passing through the liquid crystal layer once, and a relation:

$$2d \times \Delta n > \lambda/2$$

in a case where the incident light is outputted after passing through the liquid crystal layer twice, where a thickness of the liquid crystal layer is d, a birefringence is Δn and a wavelength of the light incident on the liquid crystal layer is λ; and

driving voltage applying means for applying a driving voltage including a voltage higher than a maximum voltage providing an extremum of the output light intensity in a voltage-output light intensity characteristic of the pixels to the plurality of pixels.

In one embodiment of the present invention, the driving voltage applying means applies the driving voltage to the pixels by a field sequential addressing method.

In one embodiment of the present invention, the liquid crystal device includes retardation compensation means between the liquid crystal layer and the polarizing element.

In another embodiment of the present invention, the driving voltage applying means applies a voltage higher than the maximum voltage providing the extremum of the output light intensity in the voltage-output light intensity characteristic and a voltage between the voltage higher than the maximum voltage and the maximum voltage, thereby controlling the output light intensity of the pixels.

In still another embodiment of the present invention, the driving voltage applying means reverses a polarity of the driving voltage in each frame.

In still another embodiment of the present invention, the driving voltage applying means applies a first preliminary voltage having an absolute value larger than that of a signal voltage corresponding to a predetermined output light intensity before applying the signal voltage to the pixels.

In still another embodiment of the present invention, the driving voltage applying means further applies a second preliminary voltage having an absolute value smaller than that of the signal voltage before applying the signal voltage corresponding to the predetermined output light intensity and after applying the first preliminary voltage.

In still another embodiment of the present invention, the absolute value of the first preliminary voltage is larger than that of the maximum voltage providing an extremum in the voltage-output light intensity characteristic of the pixels.

In still another embodiment of the present invention, the output light intensity at a maximum value of the signal voltage is equal to or less than 10% of a maximum in the voltage-output light intensity characteristic of the pixels.

In still another embodiment of the present invention, the absolute value of the second preliminary voltage is smaller than that of the maximum voltage providing the extremum in the voltage-output light intensity characteristic of the pixels.

In still another embodiment of the present invention, a time period for applying the first preliminary voltage is one-fifth or less than that for applying the signal voltage.

In still another embodiment of the present invention, a sum of the time period for applying the first preliminary voltage and the time period for applying the second preliminary voltage is one-fifth or less than a time period for applying the signal voltage.

In still another embodiment of the present invention, the driving voltage applying means applies the first preliminary voltage to the pixels connected to each scanning line at the same time.

In still another embodiment of the present invention, the driving voltage applying means applies the first preliminary voltage to the pixels connected to at least one scanning line.

In still another embodiment of the present invention, the driving voltage applying means applies the first preliminary voltage and the second preliminary voltage to the pixels connected to at least one scanning line for display.

In still another embodiment of the present invention, a value of the first preliminary voltage is identical to all the pixels.

In still another embodiment of the present invention, at least one of the first preliminary voltage and the second preliminary voltage has an identical value for all the pixels.

In still another embodiment of the present invention, the retardation compensation means has at least a pair of substrates and a second liquid crystal layer interposed therebetween, and an electro-optical characteristic of the second liquid crystal layer is substantially identical with that of the liquid crystal layer.

In still another embodiment of the present invention, the retardation compensation means is selected from a phase plate and a phase film.

In still another embodiment of the present invention, the retardation compensation means is selected from a uniaxially oriented polymer film and a biaxially oriented film.

In still another embodiment of the present invention, one of the pair of substrates is a silicon single crystalline substrate, and the silicon single crystalline substrate has a transistor switching a voltage applied from the driving voltage applying means to each of the plurality of pixels.

According to another aspect of the present invention, a projection-type liquid crystal display device including a liquid crystal element, wherein the liquid crystal element includes:

a pair of substrates;
a liquid crystal layer interposed between the pair of substrates;
at least one polarizing element;
a plurality of pixels;
a retardation ($d \times \Delta n$) of the liquid crystal layer satisfying one of a relation:

$$d \times \Delta n > \lambda/2$$

in a case where an incident light is output after passing through the liquid crystal layer once, and a relation:

$$2d \times \Delta n > \lambda/2$$

in a case where the incident light is outputted after passing through the liquid crystal layer twice, where a thickness of the liquid crystal layer is d, a birefringence is Δn and a wavelength of the light incident on the liquid crystal layer is λ; and

driving voltage applying means for applying a driving voltage including a voltage higher than a maximum voltage providing an extremum of the output light intensity in a voltage-output light intensity characteristic of the pixels to the plurality of pixels, is provided.

According to another aspect of the present invention, a method for driving a liquid crystal device including: a pair of substrates; a liquid crystal layer interposed between the pair of substrates; at least one polarizing element; a plurality of pixels; and a retardation ($d \times \Delta n$) of the liquid crystal layer satisfying one of a relation:

$$d \times \Delta n > \lambda/2$$

in a case where an incident light is output after passing through the liquid crystal layer once, and a relation:

$$2d \times \Delta n > \lambda/2$$

in a case where the incident light is outputted after passing through the liquid crystal layer twice, where a thickness of the liquid crystal layer is d, a birefringence is Δn and a wavelength of the light incident on the liquid crystal layer is λ, is provided. The method includes a step of applying a driving voltage including a voltage higher than a maximum voltage providing an extremum of the output light intensity in a voltage-output light intensity characteristic of the pixels to the plurality of pixels.

In one embodiment of the present invention, the driving voltage applying step includes applying the driving voltage to the pixels by a field sequential addressing method.

In another embodiment of the present invention, the driving voltage applying step includes applying a voltage higher than the maximum voltage providing the extremum of the output light intensity in the voltage-output light intensity characteristic and a voltage between the voltage higher than the maximum voltage and the maximum voltage, thereby controlling the output light intensity of the pixels.

In still another embodiment of the present invention, a polarity of the driving voltage is reversed in each frame.

In still another embodiment of the present invention, the driving voltage applying step includes applying a first preliminary voltage having an absolute value larger than that of a signal voltage corresponding to a predetermined output light intensity before applying the signal voltage to the pixels.

In still another embodiment of the present invention, the driving voltage applying step further includes applying a second preliminary voltage having an absolute value smaller than that of the signal voltage before applying the signal voltage corresponding to the predetermined output light intensity and after applying the first preliminary voltage.

In still another embodiment of the present invention, the absolute value of the first preliminary voltage is larger than that of the maximum voltage providing an extremum in the voltage-output light intensity characteristic of the pixels.

In still another embodiment of the present invention, the absolute value of the second preliminary voltage is smaller than that of the maximum voltage providing the extremum in the voltage-output light intensity characteristic of the pixels.

In still another embodiment of the present invention, a time period for applying the first preliminary voltage is one-fifth or less than that for applying the signal voltage.

In still another embodiment of the present invention, a sum of the time period for applying the first preliminary voltage and the time period for applying the second preliminary voltage is one-fifth or less than a time period for applying the signal voltage.

In still another embodiment of the present invention, the driving voltage applying step includes applying the first preliminary voltage to the pixels connected to each scanning line at the same time.

In still another embodiment of the present invention, the driving voltage applying step includes applying the first preliminary voltage to the pixels connected to at least one scanning line.

In still another embodiment of the present invention, the driving voltage applying step includes applying the first preliminary voltage and the second preliminary voltage to the pixels connected to at least one scanning line for display.

In still another embodiment of the present invention, a value of the first preliminary voltage is identical to all the pixels.

In still another embodiment of the present invention, at least one of the first preliminary voltage and the second preliminary voltage has an identical value for all the pixels.

Thus, the invention described herein makes possible the advantages of (1) providing a liquid crystal device having sufficient high-speed response, and (2) providing a method for driving the same.

These and other advantages of the present invention will become apparent to those skilled in the art upon reading and understanding the following detailed description with reference to the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure **1** is a diagram showing a configuration of a liquid crystal device according to a first example of the present invention.

Figure **2** is a graph showing a voltage-transmittance characteristic of homogeneous ECB mode in the case where d x Δn > λ/2, in the liquid crystal device of Figure **1**.

Figures **3A** to **3C** are diagrams showing behaviors of liquid crystal molecules of homogeneous ECB mode due to an applied voltage.

Figures **4A** to **4C** are diagrams illustrating an apparent birefringence Δn when a liquid crystal molecule is inclined with respect to an incident light beam.

Figure **5** is a diagram showing a configuration of a liquid crystal cell of homogenous ECB mode in the liquid crystal device of Figure **1**.

Figure **6** is a graph showing the relation between an output light intensity I_o and the retardation (d x Δn).

Figure **7** is a graph showing voltage-transmittance characteristics of liquid crystal cells having for various retardations (d x Δn).

Figure **8** is a diagram showing a configuration of a liquid crystal cell of homogenous ECB mode in the liquid crystal device of Figure **1**.

Figure **9** is a diagram showing a liquid crystal display device according to a second example of the present invention.

Figures **10A** and **10B** are graphs showing driving voltage waveforms and optical response waveforms in the case where a signal voltage V_{on} alone is applied to a liquid crystal cell and in the case where a driving voltage waveform according to the second example is applied to the liquid crystal cell, respectively.

Figures **11A** and **11B** are graphs showing driving voltage waveforms and optical response waveforms in the case where a second preliminary voltage V_L according to a third example is not present between a first preliminary voltage V_H and the signal voltage V_{on} of the second example and in the case where the second preliminary voltage V_L is present between the first preliminary voltage V_H and the signal voltage V_{on} of the second example, respectively.

Figure **12** is a diagram showing another driving voltage waveform according to a third example of the present invention.

Figure **13** is a diagram showing a configuration of a liquid crystal cell of a liquid crystal display device according to a fourth example of the present invention.

Figure **14** is a cross-sectional view showing a configuration of a liquid crystal cell of a liquid crystal display device according to a fourth example of the present invention.

Figure **15** is a graph showing a voltage-transmittance characteristic of the liquid crystal cell shown in Figure **14** in the case where a compensating liquid crystal cell is used.

Figures **16A** and **16B** are graphs showing optical response characteristics and driving voltage waveforms in the case where a compensating liquid crystal cell of the third example is not used, and in the case where a compensating liquid crystal cell of the fourth example according to the present invention is used, respectively.

Figure **17** is a flow chart showing a process for fabricating TFTs of a liquid crystal display device according to a fifth example of the present invention.

Figure **18** is a cross-sectional view of a liquid crystal display device according to a fifth example of the present invention.

Figure **19** is a plane view of a liquid crystal display device using a TFT substrate according to the fifth example of the present invention.

Figure **20** is a schematic diagram showing a configuration of AM-LCD using TFTs according to the fifth example of the present invention.

Figures **21A** to **21C** are time charts of a driving voltage waveform used for the AM-LCD of Figure **20**.

Figures **22A** and **22B** are diagrams showing a driving waveform and an optical response waveform, respectively, in the case where a liquid crystal cell fabricated according to the fabrication process of TFTs shown in Figure **17** is driven by using a driving method of the present invention.

Figure **23** is a diagram showing a driving waveform in the case where polarities of the first preliminary voltage V_H and the signal voltage V_{on} of Figure **22A** are reversed.

Figures **24A** and **24B** are a plane view and a cross-sectional view taken along line **W-W'** of Figure **24A**, respectively, in a unit pixel region of a single crystalline silicon substrate of a color liquid crystal display device according to a sixth example of the present invention.

Figure **25** is an equivalent circuit diagram showing a configuration of a circuit in the unit pixel region of Figure **24**.

Figure **26A** is a diagram showing a configuration of a projection-type liquid crystal display device including a liquid crystal element using the single crystalline silicon substrate having the circuit configuration of Figures **24A** and **24B** and Figure **26B** is a diagram showing an example of a light selecting element used for the projection-type liquid crystal display device of Figure **26A**.

Figures **27(a)** to **27(e)** are timing charts for driving the liquid crystal display device.

Figure **28** is an equivalent circuit diagram showing an example of a structure of a circuit in the unit pixel region in the sixth example of the present invention.

Figure **29** is a diagram showing a configuration of an optical system of a conventional three-plate projection-type liquid crystal display device.

Figure **30** is a diagram showing a light transmittance response characteristic of TN mode in a conventional liquid crystal display device.

Figure **31** is a graph showing the relation between a driving applied voltage and a light transmittance in a conventional liquid crystal display device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, the present invention will be described by way of examples with reference to the accompanying drawings.

Example 1

Figure **1** shows a configuration of a transmissive liquid crystal device according to a first example of the present invention. In Figure **1**, a liquid crystal device **21** includes a pair of substrates **22** and **23**, a liquid crystal layer **24** interposed between the pair of substrates **22** and **23**, a polarizer **25**, an analyzer **26**, and a driving voltage supplying portion **27** for supplying a driving voltage to electrodes (not shown) formed on the pair of substrates **22** and **23**. A liquid crystal cell **28** is constituted by the pair of substrates **22** and **23** and the liquid crystal layer **24**. The liquid crystal cell **28** has a plurality of pixels (not shown). The pixel is the smallest portion of the liquid crystal cell **28** which can control the transmittance of light independently. The driving voltage supplying portion **27** drives the liquid crystal cell **28** by supplying voltages to the pixels in accordance with the field sequential addressing method.

Each of the pixels of the liquid crystal cell **28** exhibits the voltage-transmittance (V-T) characteristic shown in Figure **2**. The driving voltage supplying portion **27** supplies the voltages having values corresponding to point **A** from point **B** in Figure **2**, so that optical on/off switching is obtained between the maximum value (**B**) and the minimum value (**A**) of the transmittance in the V-T characteristic of Figure **2**.

The V-T characteristic shown in Figure **2** is obtained when the retardation ($d \times \Delta n$), which is an optical path difference between an ordinary ray and an extraordinary ray for the liquid crystal layer **24**, satisfies the relation:

$$d \times \Delta n > \lambda/2$$

where the thickness of the liquid crystal layer **24** is d, a difference between the refractive indices of the ordinary ray and the extraordinary ray (birefringence) is Δn, and a wavelength of the incident light for display is λ. More specifically, the V-T characteristic in Figure **2** is obtained in the case of $d \times \Delta n > 3\lambda/2$.

In the present specification, the point **A** on the uppermost voltage V_1 in Figure **2** is referred to as a mode 0, at which the transmittance has the lowest value in the V-T characteristic. At the mode 0 in the V-T characteristic, the transmittance of the liquid crystal cell **28** is substantially saturated. The voltage V_1 at which the transmittance of the liquid crystal cell is saturated will be referred to as a saturation voltage. The point **B** in the V-T characteristic is referred to as a first extremum, which is in a brightest state (a maximum point) obtained for the first time when the voltage is gradually lowered from the saturation voltage V_1 at which the optical characteristic becomes mode 0. The transmittance gradually decreases from the point **B** as the applied voltage increases. Therefore, the point **A** is determined by the value of the saturation voltage V_1. Practically, the value of the saturation voltage V_1 may be selected from a voltage higher than a maximum voltage providing an extremum of the transmittance of the liquid crystal cell taking a contrast ratio and a response speed into consideration. For example, in order to obtain a contrast ratio equal to or more than 10 for a display device having the V-T characteristic shown in Figure **2**, a signal voltage for display having a maximum voltage providing the output light intensity equal to or less than 10% of the maximum (point **B**) in the V-T characteristic is applied. In this case, the value of the saturation voltage V_1 is set higher than the maximum voltage of the signal voltage.

In this example, as will be described later, the polarizer and the analyzer are set in a crossed Nicol state, therefore the transmittance (point **A**) at the saturation voltage V_1 has the lowest value. On the other hand, in the case where the polarizer and the analyzer are set in a parallel Nicol state, the transmittance at the saturated voltage will have the highest value. In both cases, the transmittance of the liquid crystal cell is saturated near the saturation voltage. As for the point **B**, it has a maximum transmittance in the crossed Nicol state, as shown in Figure **2**. On the other hand, the point **B** has a minimum transmittance in a parallel Nicol state. In the present specification, the extremum is used to refer to a maximum or a minimum value. An extremum obtained at the maximum voltage is referred as to a first extremum and an extremum obtained at the second highest voltage is referred as to a second extremum, and so on.

The V-T characteristic shown in Figure **2** is obtained from an interference phenomenon between the ordinary ray and the extraordinary ray. As a typical display mode utilizing the interference between the ordinary ray and the extraordinary ray of incident light, Electrically Controlled Birefringence (hereinafter, referred to as ECB) mode is known. The operational principle of homogenous ECB mode is as follows. A light beam incident on the liquid crystal cell **28** through the polarizer **25** has a specific polarization direction. When the polarized light beam passes through the liquid crystal cell **28**, the retardation (d x Δn) is generated between the ordinary ray and the extraordinary ray of the polarized light beam. Therefore, the polarization direction of the polarized light beam is changed by passing through the liquid crystal cell **28**. The analyzer 26 allows a light beam having a specific polarization direction to pass through.

Accordingly, the transmittance of the incident light beam depends on the retardation for the liquid crystal layer **24** and the arrangement of the polarizer **25** and the analyzer **26**. Assuming that the thickness of the liquid crystal layer **24** is d, and the difference between the ordinary refractive index (n_o) and the extraordinary refractive index (n_e), which is generated by the refractive index anisotropy of the liquid crystal layer **24**, is Δn, the retardation for the liquid crystal layer **24** is give by the product (d x Δn). An optical response is obtained by electronically changing the retardation (the optical path difference) for the liquid crystal layer **24**. The liquid crystal molecules **29** interposed between the pair of substrates **22** and **23**, which are in a homogeneous orientation state, rise by applying a voltage **E** to the liquid crystal cell **28**, as shown in Figures **3A** to **3C**. Since an apparent birefringence Δn of the liquid crystal layer **24** changes when the liquid crystal molecules **29** are inclined at an angle, the retardation (d x Δn) changes with it.

Figures **3A**, **3B** and **3C** are schematic diagrams showing orientation states of the liquid crystal molecules **29** and energies of orientational deformation of liquid crystal molecules **29** in the respective orientation states as the extension of a spring in the cases where: a voltage less than a threshold voltage is applied; an intermediate voltage is applied; and a voltage close to a saturated voltage is applied, respectively. Since the liquid crystal molecules **29** having a positive dielectric anisotropy have the property to align parallel to the direction of the applied voltage, the orientation direction of the liquid crystal molecules **29** changes in accordance with the strength of the voltage applied to the liquid crystal cell **28** as shown in Figures **3A** to **3C**. The apparent birefringence of the liquid crystal layer **24** changes with the change in the orientation direction of the liquid crystal molecules **29** with respect to the incident light. This phenomenon is described with reference to Figures **4A** to **4C**.

In Figures **4A** to **4C**, an ellipsoid represents a refractive index ellipsoid of a liquid crystal molecule, and an **M** axis represents a molecular major axis of the liquid crystal molecule. The refractive index for the light having an electric field oscillating in the molecular major axis direction of the liquid crystal molecules is represented by $n_{\parallel}$, and the refractive index for the light having an electric field oscillating in the direction perpendicular to the molecular major axis of the liquid crystal molecules is represented by $n_{\perp}$. In Figure **4B**, the z-axis represents a propagation direction of the incident light, and the x-axis and the y-axis represent directions in which the electric fields of the incident light oscillate. As shown in Figure **4B**, in the case where the propagation direction of the incident light is not parallel to the molecular major axis **M** of the liquid crystal molecule, the refractive index $n_e(\theta)$ for the extraordinary ray having the electric field oscillating in the direction slant from the **M** axis by θ (in the x-axis direction in Figure **4B**) in the plane including the **M** axis and the x-axis is given by Formula (1), depending on θ. Figure **4C** shows the relation between $n_e(\theta)$, $n_{\perp}$ and $n_{\parallel}$ in the x-z plane of Figure **4B**. On the other hand, the refractive index $n_o(\theta)$ of the ordinary ray having the electric field oscillating in the y-axis direction does not depend on θ and is equal to $n_{\perp}$, as represented by Formula (2). Therefore, the apparent birefringence $\Delta n(\theta)$ depends on θ, as represented by Formula (3). Thus, the birefringence of the liquid crystal layer varies, depending on the relation between the incident light and the orientation direction of the liquid crystal molecules.

$$n_e(\theta) = n'_e = \frac{n_\perp}{\sqrt{1 - \{1 - (\frac{n_\perp}{n_\parallel})^2\}\cos^2\theta}} \qquad (1)$$

$$n_o(\theta) = n_o = n_\perp \qquad (2)$$

$$\Delta n(\theta) = n'_e - n_o = \left\{ \frac{1}{\sqrt{1 - \{1 - (\frac{n_\perp}{n_\parallel})^2\}\cos^2\theta}} - 1 \right\} n_\perp \qquad (3)$$

$n_\parallel$;refractive index in a molecular major axis direction
$n_\perp$;refractive index in a molecular minor axis direction

n_e ;extraordinary refractive index

n_o ;ordinary refractive index

In Figure 5, light propagates in the z-axis direction and passes through the polarizer **25**, the liquid crystal layer **24** and the analyzer **26** in this order. The light I_i, which passes through the polarizer **25** and is incident on the liquid crystal layer **24**, has only an electric field E_i oscillating in the direction parallel to a polarization axis **30** of the polarizer **25**. The direction of the director of the liquid crystal molecules in the liquid crystal layer **24** is oriented to the x-axis direction of Figure **5**. The refractive index of the liquid crystal layer **24** with respect to the light having the electric field parallel to the x-axis is represented by n_e and the refractive index of the liquid crystal layer **24** with respect to the light having the electric field parallel to the y-axis is represented by n_o. The phase difference of $\Delta n{\cdot}d$ occurs between components L_e and L_o having the electric fields parallel to the x-axis and the y-axis of the incident light I_i transmitting through the liquid crystal layer **24** having a thickness of d and the birefringence: $\Delta n = n_e - n_o$. In other words, the polarization direction of the light changes. The components of the light, which have the electric field E_o parallel to the polarization axis of the analyzer **26**, pass through the analyzer **26**.

Furthermore, if the case where the polarization axis **30** of the polarizer **25** is placed at 45° with respect to a director direction of the liquid crystal molecules **29** and an analyzing axis **31** of the analyzer **26** is placed so as to be perpendicular to the polarization axis **30** of the polarizer **25** (crossed Nicol state) is considered, the following expression holds between the retardation (d x Δn) and the output light intensity I_o.

$$I_o = I_i{\cdot}\sin^2(\Delta n{\cdot}d\pi/\lambda) \quad (4)$$

I_o: output light intensity

I_i: incident light intensity

$\Delta n{\cdot}d$: retardation

λ: wavelength of incident light

Figure **6** shows a characteristic curve obtained by the above expression. It is understood from Figure **6** that at least a retardation (d x Δn) of λ/2 or more is required with respect to the wavelength λ of the incident light in order to obtain the maximum on/off ratio for the output light intensity I_o.

In Figure 7, three types of V-T characteristic are shown. That is, case 1: $d \times \Delta n < \lambda/2$; case 2: $d \times \Delta n = \lambda/2$; and case 3: $d \times \Delta n > \lambda/2$. As shown in Figure **7**, a sufficient on/off ratio cannot be obtained for the case 1. As for the case 2, only the same V-T characteristic as that of the display mode which utilizes a voltage close to a threshold value, such as a conventional TN-type liquid crystal device, is obtained. Therefore, it is most suitable to use the case 3. It is understood that even a small change in the applied voltage can greatly change the transmitted light intensity.

As described above, the V-T characteristic of ECB mode liquid crystal display **21** having a suitable retardation (d x Δn) is as is shown in Figure **2**. In this case, as shown in Figure **8**, the polarization axis **30** of the polarizer **25** is set at 45° with respect to the director direction **32** of the liquid crystal molecules in the liquid crystal layer **24**, and the analyzing direction **31** of the analyzer **26** is arranged set to be perpendicular to the polarization axis **30** of the polarizer **25** (crossed Nicol state). In the case where the polarization axis **30** is arranged parallel to the analyzing axis **31** (parallel Nicol state), the change in transmittance of the characteristic of Figure **2** is reversed.

The method for increasing the response speed of a liquid crystal display will be described below. As shown in Figure **3**, the rise of the liquid crystal molecules **29** corresponds to the stretch of a spring. Normally, when the spring is stretched, the speed of the stretch depends on the force to pull the spring. The force for the spring corresponds to the electric field for the liquid crystal molecules **29**. Therefore, the response speed for rising the liquid crystal molecules **29** (the rise speed) can be increased by increasing the applied voltage **E**. However, it is difficult to increase the response speed for relaxing the liquid crystal molecules **29** (the decay speed). The relaxation time of the orientationally deformed liquid crystal molecules **29** corresponds to the time required for restoring the stretched spring. Since the initial speed for restoring the spring depends on the potential energy of the stretched spring, the highest speed is obtained for the fully stretched spring, which has the maximum potential energy. The fully stretched spring, however, has the longest distance to be in its initial state. Therefore, the fully stretched spring does not lead to the highest response speed in the case of decay. Provided the same analogy for the orientationally deformed liquid crystal molecules, the following phenomenon is understood. When the applied voltage is turned off, the highest response speed can be obtained in the case of abovementioned mode 0 in the V-T characteristic. However, the mode 0 has the largest degree of deformation in the orientation of the liquid crystal molecules from the initial orientation state. As a result, although the display mode using a voltage close to the threshold value, such as the TN-type LCD, can provide the highest initial decay speed, the overall response speed is slow in the case of decay.

On the other hand, in order to optically switch the on/off states of a liquid crystal device utilizing the birefringence of liquid crystal molecules such as an ECB mode device, the change in the retardation ($\Delta n{\cdot}d$: Δn =

refractive index anisotropy of liquid crystal, d = cell gap) in accordance with the orientational deformation of liquid crystal molecules for at least a half wavelength is sufficient. Therefore, if $\Delta n \cdot d/\lambda > 1/2$ is satisfied, the relaxation from the mode O to the initial state is not necessary. That is, the orientational deformation is not required to relax to the initial orientation state. In particular, if Δn of the liquid crystal layer is large and $\Delta n \cdot d > 3\lambda/2$ is satisfied, as is shown by the curve representing case 3 in Figure 7, optically sufficient contrast can be obtained even if the orientational deformation of the liquid crystal molecules is minute. This result in the highest response speed.

As mentioned above, for the transmissive liquid crystal device, by setting the retardation (d x Δn) for the liquid crystal layer to satisfy the relation:

$$d \times \Delta n > \lambda/2,$$

a high contrast ratio and a high response speed can be obtained. As for a reflective liquid crystal device where the incident light passes through the liquid crystal layer twice continuously without passing through the polarizing element, the relation to obtain a high contrast ratio and a high response speed is expressed as

$$2d \times \Delta n > \lambda/2 .$$

If the present example is adapted to the reflective liquid crystal display device where the incident light is outputted from the analyzing element after passing through the liquid crystal layer twice, the retardation caused by the optical path is equivalent to that for a transmissive liquid crystal device where the thickness of the liquid crystal cell is doubled. Therefore, the following relation holds between the retardation (d x Δn) and the output light intensity I_o.

$$I_o = I_i \cdot \sin^2(\Delta n \cdot 2d\pi/\lambda) \quad (5)$$

In the present specification, the output light intensity refers to the transmitted light intensity for the transmissive device and the reflected light intensity for the reflective device. The voltage-transmittance characteristics as shown in Figures **2** and **7** may be referred to as the voltage-output light intensity characteristics so as to include the optically equivalent voltage-reflectance characteristics.

For the reflective liquid crystal device, the case corresponding to those of Figure **7** are: case 1: d x $\Delta n < \lambda/4$; case 2: d x $\Delta n = \lambda/4$; and case 3: d x $\Delta n > \lambda/4$, respectively.

As described above, the liquid crystal device having an adequate retardation can be driven by applying the voltage to the pixels in the field sequential addressing method so that optical on/off states are switched by applying a maximum voltage corresponding to the extremum value (maximum value or minimum value) of the light transmittance in the V-T characteristic and the saturation voltage higher than the maximum voltage. In the case where $\Delta n \cdot d > \lambda$, preferably $\Delta n \cdot d > 3\lambda/2$, is satisfied and a plurality of extrema are obtained in the V-T characteristic, the on/off switching may be performed between the first extremum and the second extremum, as long as sufficient response speed is obtained.

By utilizing the highly deformed orientation state (mode 0), the liquid crystal device according to this example can provide a high response speed as well as a high contrast ratio. It is preferable that each of a rise time and a decay time of the optical response is one-fifth or less than a display period.

Example 2

Figure **9** is a cross-sectional view showing a configuration of a liquid crystal display device **40** according to a second example of the present invention. The liquid crystal display device **40** includes a liquid crystal cell **45** having a pair of substrates **45a** and **45b**, a liquid crystal layer **44** interposed between the pair of substrates **45a** and **45b**. On the sides of the liquid crystal cell **45**, a polarizer **47** and an analyzer **48** are provided. A driving voltage supplying portion **46** supplies a driving voltage to the liquid crystal cell **45**.

In this example, the driving voltage supplying portion **46** supplies a driving voltage waveform which applies a first preliminary voltage having an absolute value larger than a signal voltage before applying a signal voltage for obtaining a predetermined output light intensity (transmittance or reflectance) to the liquid crystal cell **45**.

A fabrication method of the liquid crystal cell **45** will be described. An ITO film **42a** having a thickness in the range of 0.1 to 1.1 μm is formed by using a sputtering method on a glass substrate (trade name: 7059, manufactured by Corning Inc.) **41a** having a thickness of 1.1 mm. The ITO film **42a** on the substrate **41a** is etched into an electrode with a desired shape (character, figure, matrix or the like) by using a photolithography process. Another ITO film **42b** is formed on the entire surface of another glass substrate **41b** in the same manner so as to form a counter electrode. Alignment films (trade name: Optomer AL4552, manufactured by Japan Synthetic Rubber Ltd.) **43a** and **43b** are formed over the surfaces of the substrates **45a** and **45b**. After being cured at 230°C, the alignment films **43a** and **43b** are subject to the rubbing treatment so that the rubbing directions become antiparallel when the pair of substrates **41a** and **41b** are attached to each other to form the liquid crystal cell **45**.

After the alignment treatment, a liquid crystal sealing layer (not shown) is formed by a screen printing method using an adhesive sealing material, in which glass fiber having a diameter of 4.5 μm is mixed. Then, the pair of the substrates **45a** and **45b** are attached to each other by the liquid crystal sealing layer interposing a glass beads spacer (not shown) having a diameter of 4 μm between them. A liquid crystal material is injected to a gap between the pair of substrates **45a** and **45b** by a vacuum injection method so as to obtain the liquid crystal layer **44**. The reference numeral **49** denotes a director direction of the liquid crystal molecules in the liquid crystal layer **44**. The liquid crystal material used in this example is BL035 (manufactured by Merck & Co., Inc.: Δn= 0.267). Other liquid crystal materials may be used.

The optical response characteristics in the cases where a signal voltage V_{on} alone is applied and where the driving voltage waveform is applied are shown in Figures **10A** and **10B**, respectively. Figure **10A** shows the case where the signal voltage: V_{on} = 3V, which is a step voltage, is applied, and Figure **10B** shows the case where the first preliminary voltage V_H and the signal voltage V_{on} are applied in this order. In this experiment, the measurement of the optical characteristics is carried out under the following conditions: the first preliminary voltage V_H = 20 V; time period T_H for applying the first preliminary voltage V_H = 0.25 msec; and time period T_{on} for applying the signal voltage V_{on} = 4.75 msec. As a result, as shown in Figure **10A**, the liquid crystal display device does not have an optically sufficient response in the case where the signal voltage V_{on} alone is applied. That is, the response speed is not sufficiently fast, resulting in that the transmittance does not reach the desired value (35%). However, in the case where the first preliminary voltage V_H and the signal voltage V_{on} are used, as in Figure **10B**, the optically sufficiently high response speed is obtained.

In this case, the time period T_H for applying the first preliminary voltage V_H is required to be shorter than the time period T_{on} for applying the signal voltage V_{on} which is a display signal. Preferably, it is desirable that the time period T_H for applying the first preliminary voltage V_H is one-fifth or less than the time period T_{on} for applying the signal voltage V_{on}.

Although the display mode of the liquid crystal used in this example is homogeneous EBC mode, the display mode utilizing the birefringence such as Super-Twisted Nematic (STN) may be used. An oblique vapor deposition method may be used as well as the rubbing method as an alignment controlling method. In this example, although both of the substrates are glass substrates, one of them may be an opaque substrate such as a semiconductor substrate for a reflective device.

<u>Example 3</u>

In this example, a second preliminary voltage V_L having an absolute value smaller than that of a signal voltage V_{on} is applied between the application of the signal voltage V_{on} and a first preliminary voltage V_H having an absolute value larger than the signal voltage V_{on}.

The comparison between the optical response characteristics of the cases where a second preliminary voltage V_L is present and is not present between the first preliminary voltage V_H and signal voltage V_{on} are shown in Figures **11A** and **11B**, respectively, using the liquid crystal cell similar to the liquid crystal cells **45** which are formed according to the second example. Figure **11A** shows the case where the second preliminary voltage V_L is not present, and Figure **11B** shows the case where the second preliminary voltage V_L is present. In this experiment, the measurement of the optical characteristics is carried out under the following conditions: the first preliminary voltage V_H = 20 V; the second preliminary voltage V_L = 0 V; a signal voltage V_{on} = 3 V; time period T_H for applying the first preliminary voltage V_H = 0.25 msec; time period T_L for applying the second preliminary voltage V_L = 0.25 msec; and time period T_{on} for applying the signal voltage V_{on} = 4.5 msec. As a result, as shown in Figures **11A** and **11B**, the distortion present in the waveform of the optical response characteristic can be eliminated by providing the time period for applying the second preliminary voltage V_L between the time period for applying the first preliminary voltage V_H and the signal voltage V_{on}.

As described above, the optical response speed becomes higher by applying the first preliminary voltage V_H having an absolute value larger than at least that of the signal voltage V_{on} and further applying the second preliminary voltage V_L having an absolute value smaller than at least that of the signal voltage V_{on} before applying the signal voltage V_{on} for obtaining the predetermined transmittance and reflectance to the respective pixels constituting the liquid crystal display.

In this case, it is necessary that the time period T_H for applying the first preliminary voltage V_H and the time period T_L for applying the second preliminary voltage V_L are shorter than the time period T_{on} for applying the signal voltage V_{on} which is a display signal, respectively. Preferably, it is desirable that the total of the time periods for applying the first preliminary voltage V_H and the second preliminary voltage V_L, i.e., $T_H + T_L$, is one-fifth or less than the time period T_{on} for applying the signal voltage.

In the third example described above, the display is performed in the following manner. The first preliminary voltage V_H for changing the molecular orientation to the mode ϕ is constantly applied immediately before performing the display, as shown in Figure **12**, utilizing the liquid crystal having Δn satisfying the above-mentioned condition: d x Δn > λ/2 or 2d x Δn > λ/2. Then, the liquid crystal molecules are relaxed by the second preliminary voltage V_L which is lower than the voltage corresponding to the first peak in the V-T characteristic after applying the first preliminary voltage V_H. Thereafter, the display is performed by the applied signal voltage V_{on}. At this moment, since the first preliminary voltage V_H is required to make the orientational state of the liquid crystal molecules be in mode ϕ as an optical response, the voltage V is preferably higher than the voltage V_1, which is a saturation voltage in the V-T characteristic. Considering that the speed in the orientational change of the liquid crystal molecules increases with the increase of the applied voltage, as described before, the liquid crystal molecule orientation is transitioned to mode ϕ with a higher speed in the case where the first preliminary voltage $V_H \geqq V_1$. The speed of relaxation is increased as the second preliminary voltage V_L becomes closer to 0 V since the difference in the potentials of the liquid crystal molecules becomes wider. Since the first and second preliminary voltages V_H and V_L are not used for displaying an image, the quality of the display image is deteriorated if $T_H + T_L$, which is the time period for applying the preliminary voltages, is unnecessarily long. However, the inventors confirmed the following fact by experiment. In view of the response characteristic and display quality of the liquid crystal display device itself, if the maximum value of time period $T_H + T_L$ for applying the voltages is one-fifth or less than the time period T_{on} for applying the display signal in one field, the conspicuous deterioration is not observed. Regarding the minimum value, since it is desirable to apply the first and second preliminary voltages for the time period in which the orientational change in the liquid crystal molecules can transition as described above, it is preferable to optimize each physical constant, such as viscosity and elasticity of the liquid crystal materials.

Although the display mode of the liquid crystal used in this example is homogeneous EBC mode, the display mode utilizing the birefringence such as STN may also be used. An oblique vapor deposition method can also be used as well as the rubbing method as an orientation controlling method. In this example, although both of the substrates are glass substrates, one of them may be an opaque substrate such as a semiconductor substrate for a reflective device.

Example 4

A liquid crystal cell capable of being driven with a lower voltage is shown as a fourth example. In the graph of Figure **2**, since the transmittance of the mode 0 is not completely saturated and therefore the transmittance does not reach the minimum value, a sufficiently high contrast ratio may not be obtained. Since the liquid crystal molecules at a surface of a substrate are under a strong influence of an anchoring, as compared with the bulk liquid crystal molecules in the middle of a liquid crystal layer in the thickness direction, the orientational change of the liquid crystal molecules at the surface does not occur unless an extremely high voltage is applied. Thus, as shown in Figure **3C**, although the bulk liquid crystal molecules rise, the liquid crystal molecules at the surface of the substrates remain in the initial orientation state. In such a state, since the retardation of the liquid crystal molecules at the surface remain, the leakage of light occurs. In order to obtain the transmittance of around 0% at mode 0, an extremely high voltage (several tens V or more) is necessary. A display method using such a high voltage is not preferable because the voltage ratio for on/off switching is increased for the driving voltage.

A configuration of a liquid crystal device as an example of solutions of the above problem is shown in Figure **13**. A method for solving the problem is as follows. A liquid crystal cell **51** on the driving side used for displaying image and an equivalent liquid crystal cell **52** on the compensation side are overlapped with each other so that the rubbing directions (the direction of directors of the liquid crystal molecules) **53a** and **53b** are perpendicular to each other in Figure **13**. The retardation of the liquid crystal cell **51** on the driving side is compensated by the retardation of the liquid crystal cell **52** on the compensation side. In this example, the reference numerals **54** and **56** denote a polarization axis of the polarizer **55** and an analyzing axis of the analyzer **57**, respectively.

The fourth example in accordance with the compensation method will be described with reference to Figure **14**. The liquid crystal cell **51** on the driving side is obtained in the following manner. A substrate **51a** is obtained by forming an ITO film **62a** by using a sputtering method having a thickness in the range of 0.1 to 1.1 μm on a glass substrate (trade name: 7059, manufactured by Corning Inc.) **61a** having a thickness of 1.1 mm. The ITO film **62a** on the glass substrate **61a** is etched to form a strip electrode by using a photolithography process. Liquid crystal alignment films (trade name: Optomer AL4552, manufactured by Japan Synthetic Rubber Ltd.) **63a** and **63b** are applied to the thus formed substrate **51a** and another substrate **51b** having a strip electrode formed of ITO film **62b** on a glass substrate **61b** in the same manner. After being cured at 230°C, the pair of substrates **51a** and **51b** are subject to the rubbing treatment so that the rubbing directions become antiparallel when the pair of substrates **51a** and **51b** are attached to each other.

After the alignment treatment, a liquid crystal sealing layer (not shown) is formed by a screen printing method using an adhesive sealing material, in which glass fiber having a diameter of 4.5 μm is mixed. Then, the pair of the substrates **51a** and **51b** are attached to each other by the liquid crystal sealing layer interposing a glass beads spacer (not shown) having a diameter of 4 μm between them. The pair of substrates **51a** and **51b** are attached to each other so that the strip electrodes are perpendicular to each other and the rubbing directions are antiparallel to each other. Portions of the liquid crystal cell **51** where the strip electrodes overlap function as pixels. A liquid crystal material is injected to a gap between the pair of substrates **51a** and **51b** by a vacuum injection method so as to obtain the liquid crystal layer **64**. The liquid crystal material used in this example is BL035 (manufactured by Merck & Co., Inc.: Δn= 0.267).

The liquid crystal cell **52** is fabricated in the same manner as the liquid crystal cell **51**. However, ITO films **162a** and **162b** formed on glass substrate **161a** and **161b** are not etched to form the strip electrodes. The surface of substrates **52a** and **52b** are covered by alignment films **163a** and **163b**, respectively. A liquid crystal layer **164** sandwiched between the pair of substrates **52a** and **52b** are aligned so that the director **165** is perpendicular to the director **65** of the liquid crystal layer **64**.

The liquid crystal cell **51** including the ITO films **62a** and **62b** having electrodes with a certain shape is called the driving liquid crystal cell **51**, and the other is called the compensating liquid crystal cell **52**. The pair of liquid crystal cells **51** and **52** are overlapped with each other so that the directors **65** and **165** of the liquid crystal molecules are perpendicular to each other. Then, the pair of liquid crystal cells **51** and **52** are attached to each other by using an adhesive resin **66** having the same refractive index and spectral characteristic as those of the insulating substrates **161b** and **161a**. A polarizer **67** and an analyzer **68** are provided on the sides of the combined liquid crystal cells.

The voltage-light transmittance characteristic of the liquid crystal device **60** is shown in Figure **15**. The voltage applied to the compensating liquid crystal cell **52** is a voltage V_{1c} (hereinafter, the point **C** is referred to as a pseud mode 0) at which the transmittance becomes minimum in the V-T characteristic of the liquid crystal device **60** having the driving liquid crystal cell **51** and the compensating liquid crystal cell **52**. The pseud mode 0 corresponds to the mode 0, which moves to the low voltage side due to the compensating liquid crystal cell **52**. A point **D** represents the first peak value having the maximum transmittance.

The driving voltage waveforms and the optical response characteristics of the cases where the compensating liquid crystal cell **52** is used and is not used are shown in Figures **16A** and **16B**, respectively. In this experiment, the measurement of the transmittance in Figure **16A** is conducted under the following conditions: the first preliminary voltage V_H = 20 V; the second preliminary voltage V_L = 0 V; and the signal voltage V_{on} = 3 V. The measurement in Figure **16B** is conducted under the following conditions: the first preliminary voltage V_H = 6 V; the second preliminary voltage V_L = 0 V; and the signal voltage V_{on} = 2.4 V. Furthermore, both measurements are conducted under the following conditions: time period T_H for applying the first preliminary voltage V_H = 0.25 msec; time period T_L for applying the second preliminary voltage V_L = 0.25 msec; and time period T_{on} for applying the signal voltage V_{on} = 4.5 msec.

As a result, the same optical response can be obtained with a lower driving voltage as shown in Figures **16A** and **16B** by providing the compensating liquid crystal cell **52** as a retardation compensation means for compensating the retardation for the liquid crystal cell **51**.

In this example, although the glass substrates **61a** and **61b** are used for both substrates of the driving liquid crystal cell **51**, the glass substrate **61a** may be an opaque substrate such as a silicon substrate for a reflective device. Although the display mode of the liquid crystal display device **60** of this example is a homogeneous EBC mode, the display mode utilizing the birefringence, such as STN mode, may also be used. An oblique vapor deposition method may be used as well as the rubbing method as an alignment controlling method. Furthermore, although the compensation liquid crystal cell **52** fabricated under the same conditions of the liquid crystal cell **51** is used in this example, a uniaxial or biaxial orientation film as a phase plate may also be used. The retardation of the phase plate is preferably equal to that of the driving liquid crystal cell at mode C.

Example 5

A specific driving method with a driving voltage waveform of the present invention in the case of the homogeneous EBC mode using the active matrix method will be described as a fifth example, with reference to Figures **17**, **18** and **19**.

Figure **17** shows the fabrication process of TFTs which are active elements in the fifth example, Figure **18** is a cross-sectional view of a liquid crystal display cell **180** in the fifth example, and Figure **19** is a plane view of an active matrix substrate **180a** of the liquid crystal display cell **180** in the fifth example. As shown in Figures **17** to **19**, at step **S1**, a Ta metal layer having a thickness of 300 nm is formed on an insulating substrate **71** made of glass by a sputtering method. Then, the patterning of the metal layer is performed by using a photolithography process and an etching process, thereby forming a gate bus wiring **72** and a gate electrode **73**. Next, at step **S2**, a gate insulating film **74** made of SiNx having a thickness of 400 nm is formed by a plasma

Chemical Vapor Deposition method. At step **S3**, an a-Si layer having a thickness of 100 nm to be a semiconductor layer **75** and an n^+-type a-Si layer having a thickness of 40 nm to be a contact layer **76** are successively formed in this order by the plasma CVD method. Then, the patterning of the n^+-type a-Si layer and the a-Si layer is performed, thereby forming the contact layer **76** and the semiconductor layer **75**. At step **S4**, a Mo metal layer having a thickness of 200 nm is formed by a sputtering method. Then, the patterning of the Mo metal layer is performed, thereby forming a source electrode **77**, a drain electrode **78** and a source bus line **79**. The drain electrode **78** are connected to a pixel electrode **88**. The source bus line **79**, which functions as a signal line, is connected to the source electrode **77** which functions as an input terminal of the TFT **80**. With the above process, the active matrix substrate **180a** having the TFT **80** is obtained.

A method for producing the liquid crystal display cell **180** using the active matrix substrate **180a** will be described. A counter substrate **180b** is obtained by forming an ITO film **82** with a thickness in the range of 0.1 to 1 μm on a glass substrate **81** (trade name: 7059, manufactured by Corning Inc.) having a thickness of 1.1 mm by using a sputtering method. The ITO film **82** is patterned to form a plurality of counter electrodes in strips. After liquid crystal alignment films (trade name: Optomer AL4552, manufactured by Japan Synthetic Rubber Ltd.) **83** are applied to cover the substrates **180a** and **180b**. Then the substrates **180a** and **180b** are cured at 230°C. The pair of substrates **180a** and **180b** are subject to the rubbing treatment so that the rubbing directions become antiparallel to each other when the pair of substrates **180a** and **180b** are attached to each other. An adhesive sealing material having a thickness of 4.5 μm, in which glass fiber is mixed, is used to form a liquid crystal sealing layer (not shown) by the screen printing method. The pair of the substrates **180a** and **180b** are attached to each other by the liquid crystal sealing layer, interposing a glass beads spacer (not shown) having a thickness of 4 μm therebetween. The substrates **180a** and **180b** are attached to each other so that the strip electrodes are parallel to the gate bus line **72** and overlaps with the pixel electrode **88**. Then, a liquid crystal material is injected between the pair of the substrates **180a** and **180b** to form a liquid crystal layer **84** by vacuum injection method. The liquid crystal used in this example is BL035 (manufactured by Merck & Co., Inc.: Δn = 0.267).

A polarizer **85** is formed on the light entering side of the thus fabricated liquid crystal display cell **180**. A phase plate **86** and an analyzer **87** are provided in this order on the light outputting side of the liquid crystal display cell **180**.

A driving method for driving an active matrix liquid crystal display device **190** (hereinafter, referred to as AM-LCD) with the driving voltage waveform according to the present invention will be described. Figure **20** shows an entire structure of the AM-LCD **190** according to the fifth example. As shown in Figure **20**, the AM-LCD **190** includes the active matrix liquid crystal cell **180**, a gate driving circuit **91**, source driving circuit **92** and a counter electrode driving circuit **93**. The active matrix liquid crystal cell **180** is driven by the gate driving circuit **91** and the source driving circuit **92** using a line sequential addressing method. The counter substrate **180b** of the active matrix liquid crystal cell **180** has a plurality of strip counter electrodes **94** arranged to be parallel to the gate bus line **72**. Therefore, it is possible to apply a counter voltage to the counter electrodes line by line synchronizing with a timing of the application of the gate voltage to the corresponding gate bus line **72**. The counter voltage is supplied by the counter electrode driving circuit **93**.

Figures **21A** through **21C** are time-charts of the driving voltage waveform of the present invention. Figure **21A**, **21B** and **21C** show a gate voltage **191**, a counter voltage **193** and a source voltage **192**, respectively. A source voltage **192** shown in Figure **21C** is applied through the source electrode to the pixel electrode while the gate of the TFT is opened by a gate voltage **191** shown in Figure **21A**. The source voltage **192** corresponds to the signal voltage V_{on}. A counter voltage **193** shown in Figure **21B**, which is a pulse voltage applied to the counter electrodes before the application of the source voltage **192** through the source electrode, is applied while the gates of TFTs are open. The counter voltage **193** corresponds to the first preliminary voltage V_H. A voltage unapplied time period, which occurs between the application of the first preliminary voltage V_H (**193** in Figure **21B**) and the application of the signal voltage V_{on} (**192** in Figure **21C**), corresponds to a period for the second preliminary voltage V_L.

Figures **22A** and **22B** shows the case where the active matrix liquid crystal cells, which are obtained according to the fabrication process of TFTs shown in Figure **17**, are driven by using the driving method of the present invention. Figure **22A** shows a driving waveform. The driving voltage is a voltage applied to a pixel, which is a voltage difference between a source voltage (a signal voltage) and a counter voltage. Figure **22B** shows an optical response characteristic. In Figure **22A**, the signal voltage V_{on} is changed to 6 V, 5 V, 4 V, 3 V, 2.4 V, under the conditions: the first preliminary voltage V_H = 10 V; and the second preliminary voltage V_L = 0 V. The polarity of the applied voltage is reversed in each frame in order to prevent the deterioration of the liquid crystal material. As described above, the liquid crystal display device, which is capable of responding with high speed and displaying half tone, is obtained by using the driving method of the present invention.

Although the display characteristic using the frame inversion driving method is shown in Figures **22A** and

22B, the driving method is not limited to the frame inversion driving method as long as the voltage applied to the liquid crystal material does not include a direct current component as the whole driving voltage. Although the polarity of the first preliminary voltage V_H is identical with that of the signal voltage V_{on} in one field, the polarity of the first preliminary voltage V_H may be inversed. That is, the polarity of the first preliminary voltage V_H may be identical with that of a signal voltage applied in the preceding field, as is shown in Figure **23**.

In this example, although the TFT is used as a switching element, a Metal-Insulator-Metal (MIM) element may be used. As for the substrate on which the TFTs are formed, instead of the insulating substrate, an opaque substrate such as a silicon substrate may also be used for a reflective device. Although the display mode of the liquid crystal display device used in this example is homogeneous EBC mode, the display mode utilizing the birefringence, such as STN mode, may be used. An oblique vapor deposition method may be used as well as the rubbing method as an alignment controlling method. Furthermore, although the liquid crystal cell similar to the liquid crystal cell for driving is used as a birefringent material for compensating the retardation of the driving liquid crystal cell, a film having a phase difference or a material having the same effect may also be used.

Example 6

As a sixth example, the case where a silicon single crystalline substrate is used for a back face substrate of a liquid crystal display device is described. In this example, a switching transistor for driving a pixel electrode is formed in the single crystalline silicon. Since the single crystalline silicon has high mobility (about $1500cm^2 \cdot V^{-1} \cdot s^{-1}$), TFTs far excellent than amorphous silicon thin film TFTs and polysilicon TFTs can be obtained. The performance of each transistor is shown in Table 1.

[Table 1]

		Single-crystalline Si	Poly-crystalline Si	Amorphous Si
Mobility ($cm^2 \cdot v^{-1} \cdot s^{-1}$)	Electron	1500	100	0.1 ~ 0.5
	Hole	600	50	-
Ion/Ioff		$>10^9$	10^7	10^5
Operation frequency (CMOS shift register)		Several GHz (1μm rule)	20 MHz (L=10 μm W=30 μm)	5 MHz (L=10 μm W=30 μm)

It is understood from Table 1 that the switching element having a high current driving ability and a large on/off ratio of a current can be obtained if transistors are formed in the single crystalline silicon.

As described above, the switching element with high operation speed can be obtained by forming switching transistors in a single crystalline silicon layer. Therefore, by combining the nematic liquid crystal driving method according to the present invention, which can provide a high response speed and is capable of displaying gray-scale, with the TFTs formed in the single crystalline silicon, a color display driven by the field sequential color mixing method can be realized easily.

Hereinafter, a solution for a problem in stability of the holding of signal voltages in the active matrix liquid crystal display device will be described.

In Figures **24A** and **24B**, a configuration of a circuit of a unit pixel region of a color liquid crystal display device is shown. Figure **24A** is a plane view, and Figure **24B** is a cross-sectional view taken along a line **W-W'** in Figure **24A**. As shown in Figures **24A** and **24B**, a switching circuit of NMOS is formed on a base substrate **101** which is made of P-type single crystalline silicon. In this device, two transistors, that is, a first transistor **Q1** and a second transistor **Q2**, are formed in a unit pixel region. Sources **Q1s** and **Q2s** and drains **Q1d** and

Q2d of the respective transistors **Q1** and **Q2** are formed as an N-type diffusion layer **102** in the P-type single crystalline silicon. Gate electrodes **Q1g** and **Q2g** of the respective transistors **Q1** and **Q2** are completely covered with a gate insulating layer **103**. In this example, polysilicon is used for the gate electrodes **Q1g** and **Q2g**, and a silicon oxide film is used for the gate insulating film **103**. The transistors **Q1** and **Q2** are separated from each other by a field silicon oxide film **104** and an aluminum electrode **105** on the base substrate **101**. A storage capacitor **Cs** is also provided in the unit pixel region. The storage capacitor **Cs** is constituted by the aluminum electrode **115** formed in the field silicon oxide film **104** adjacent to the second transistor **Q2**, the N-type diffusion layer **102** formed in the silicon layer corresponding to the position of the aluminum electrode **115**, and the field silicon oxide film **104** interposed therebetween.

A protection layer **106** is formed over the surface of the base substrate **101** so as to cover the gate oxide film (including the gate electrode) **103**, the field silicon oxide film **104**, the aluminum electrode **105** and an aluminum wiring. The protection layer **106** is provided for protecting the NMOS circuit formed on the base substrate **101**.

A through hole **110** is formed through the protection layer **106** at the position where the aluminum electrode **105** between the transistor **Q2** and the field silicon oxide film **104** formed adjacent thereto is formed on the field silicon oxide film **104**.

A pixel electrode **111** is formed in each unit pixel electrode region so as to cover the predetermined region on the protection film **106**. The pixel electrode **111** is connected to the aluminum electrode **105** of the lower layer through the through hole **110** and is electronically connected to the drain electrode **Q2d** of the transistor **Q2** through the aluminum electrode **105**.

The gate electrode **Q1g** of the first transistor **Q1** is connected to a scanning line **112**, and the source electrode **Q1s** of the first transistor **Q1** is connected to a signal line **113** crossing the scanning line **112**. The drain electrode **Q1d** of the first transistor **Q1**, the second gate electrode **Q2g** of the second transistor **Q2**, and the aluminum electrode **115** of the storage capacitor **Cs** are connected to the common aluminum electrode formed on the field silicon oxide film **104**.

A transparent counter electrode **108** is formed on the entire counter side face of a glass substrate **107** which is placed so as to be opposed to the base substrate **101**. An alignment film (not shown) is formed so as to cover the counter electrode **108**.

The glass substrate **107** and the base substrate **101** are placed so as to be opposed to each other, and a liquid crystal layer **109** is sealed therebetween. The glass substrate **107** is used as a side on which light is incident. In this example, the liquid crystal BL035 (manufactured by Merck & Co., Inc.: $\Delta n = 0.267$) is injected between the two substrates **101** and **107** to form the liquid crystal layer **109** by a vacuum injection method. Although not shown in Figures **24A** and **24B**, rubbing treatment is performed on the liquid crystal alignment films so that the liquid crystal molecules are homogeneously oriented. The phase plate and the polarizer, which are optimized by the retardation of the liquid crystal layer, are placed in this order.

Although the display mode of the liquid crystal used in this example is homogeneous EBC mode, the display mode utilizing the birefringence such as STN may also be used. An oblique vapor deposition method may be used as well as the rubbing method as an alignment controlling method. Furthermore, although the liquid crystal cell similar to the driving liquid crystal cell is used as a birefringent material for compensating the retardation of the driving liquid crystal cell, a film having a phase difference or a material having the same effect may also be used.

Next, a driving circuit of the liquid crystal display device according to the sixth example and a method for driving the same will be described.

In Figure 25, an equivalent circuit of the switching circuit for driving the liquid crystal cell shown in Figures **24A** and **24B** according to the sixth example is shown. Figure **25** shows a configuration of the circuit of the unit pixel region. As shown in Figure **25**, the first transistor **Q1** is connected to the scanning line **112** and the signal line **113**, respectively, in the vicinity of the intersecting point of the scanning line **112** and the signal line **113**. An end of the storage capacitor **Cs** and the gate **Q2g** of the second transistor **Q2** are connected to the drain **Q1d** of the first transistor **Q1**. On the other hand, the source **Q2s** of the second transistor **Q2** is connected to the source, and the drain **Q2d** of the second transistor **Q2** is connected to the pixel electrode **111**. The second transistor **Q2** has such performance that the electric potentials of the gate **Q2g** and the drain **Q2d** show a substantially linear relation. Since the first transistor **Q1** supplies the data signal to the second transistor **Q2**, it is desirable that the amount of leak current during an off state is small. The storage capacitance **Cs** functions so as to hold the data signal of the first transistor **Q1**. The second transistor **Q2** is for applying a voltage to the liquid crystal layer **109**. Since the voltage is directly applied to the liquid crystal layer **109** through the second transistor **Q2**, the second transistor **Q2** has a withstand voltage higher than a voltage required for switching the liquid crystal layer **109**.

With the above configuration, when the data signal is first input to the signal line **113** and the first transistor

Q1 in the pixel electrode region on the scanning line **112** is switched on by applying the scanning signal to the first scanning line **112**, the data signal is successively applied to each transistor **Q1** connected to the first scanning line **112**. At the same time, the data signal is held in the corresponding storage capacitor **Cs**. Since the second transistor **Q2** has a characteristic capable of controlling a source voltage in a linear relation with respect to a scanning signal voltage, a voltage proportional to the data signal voltage applied to **Q2g**, which corresponds to a scanning signal voltage to **Q2g**, is applied to the liquid crystal layer **109**. The voltage applied to the liquid crystal layer **109** is controlled by the voltage held in the storage capacitor **Cs**. Since the voltage held in the storage capacitor **Cs** is maintained to the next field, a constant voltage is continuously applied to the liquid crystal layer **109** during one field. Even when the first transistor **Q1** is switched off, the on state of the second transistor **Q2** is maintained until the first transistor **Q1** is switched on a next time. The second transistor **Q2** continuously applies a voltage proportional to the data signal voltage from the storage capacitor **Cs** to the liquid crystal layer **109**.

According to this example, it is possible to rapidly scan all of the first transistors **Q1** connected to a plurality of scanning lines so as to form an entire display image. Therefore, it is possible to rewrite the entire display image at substantially the same time.

As described above, the liquid crystal display device capable of being driven by the field sequential addressing method is obtained by employing the liquid crystal display device using the silicon substrate as the back face substrate according to this example. Since the incident light passes through the liquid crystal layer twice before being outputted through the polarizing element, the liquid crystal layer is required to adjust the liquid crystal cell gap (d) and the refractive index anisotropy (Δn) so as to satisfy the condition: $\Delta n \cdot d > \lambda/4$ (preferably, $\Delta n \cdot d > 3\lambda/4$, which is the condition for a high-response speed).

It is possible to constitute a projection-type liquid crystal display device capable of being driven by the field sequential addressing method by using the liquid crystal device described above in the optical system shown in Figures **26A** and **26B**. Hereinafter, a display method of the projection-type liquid crystal display device will be described.

As shown in Figures **26A** and **26B**, a beam splitter prism **121**, which is formed by combining the slant faces of a pair of prisms **122** and **123**, splits unpolarized light beam into an S-polarized light beam **120a** and a P-polarized light beam **120b** at a counter slant face **124**. The S-polarized light beam **120a** and the P-polarized light beam **120b** are output to a reflection-type liquid crystal display element **125** and a reflection-type liquid crystal display element **126**, respectively. Furthermore, the beam splitter prism **121** transmits the polarized light beam **120a** reflected by the reflection-type liquid crystal display element **125** and reflects the polarized light beam **120b** reflected by the reflection-type liquid crystal display element **126**. Accordingly, the polarized light beams **120a** and **120b** are combined to output a light beam **120c**. The output light beam **120c** is projected onto a display screen **128** through a projection lens **127**.

In the optical system of Figure **26A**, a light selecting element **129**, a UV-cut filter **131** and a rotor **132** equipped with red, green and blue color filters are placed in front of a light source **130** of Figure **26B**. The reference numeral **133** denotes a lens.

Figures **27(a)** and **27(b)** shows the timings for writing data in two liquid crystal elements **LC1** and **LC2** (corresponding to the liquid crystal elements **125** and **126** of Figure **26A**), respectively. Red, Green and Blue of the figures represent the time periods in which the data signals corresponding to the respective colors are written, and each of the time periods corresponds to one field period. Three field periods correspond to one frame period. Each of the data signals is alternately written in **LC1** and **LC2**. The ray output from the two liquid crystal elements **LC1** and **LC2** is selected with the timing shown in Figure **27(c)**. The output light intensity of the liquid crystal elements **LC1** and **LC2** changes in terms of time as schematically shown in Figure **27(d)**. Therefore, the output light intensities corresponding to R, G and B, respectively, reach the saturation intensity during the time period of **W2** and then keep the saturation intensity during the time periods of **DR**, **DG** and **DB**, respectively. Thus, the intensity of an output light **120c** in Figure **26A** changes as shown in Figure **27(e)**. The color of the output light is obtained by adjusting the timing of rotation of the color filter of the rotor **132** so as to correspond to the data signal written in either **LC1** or **LC2** in the previous field period. In such a manner, it is possible to drive the projection-type liquid crystal display device shown in Figure **26(a)** by the field sequential addressing method.

An optical element for beam-splitting is not limited to the beam splitter prism **121**. It is also possible to use the combination of a plurality of dichroic mirrors, which is capable of splitting an unpolarized light beam into an S-polarized light and a P-polarized light beam and outputting the reflected polarized light beams including the image information, which are reflected by the two reflective liquid crystal display elements **125** and **126**, while being aligned. As a light source, it is possible to prepare a plurality of monochromatic light sources for a red beam, a green beam and a blue beam and select the light sources so as to be synchronized with the driving timings of the liquid crystal display device.

Example 7

As a seventh example, another example of an equivalent circuit having the configuration in the unit pixel region in the sixth example is shown in Figure **28**. As shown in Figure **28**, the data signal is supplied to either a first holding capacitor C_{H11} or a first holding capacitor C_{H12} through transistors **Tr1** and **Tr2**. One electrode of the first holding capacitor C_{H11} and one electrode of the first holding capacitor C_{H12} are connected to one electrode of a second holding capacitor C_{H2}, which is common to the both first capacitors, through a transistor **Tr3** and a transistor **Tr4**, respectively. In this manner, when the first holding capacitor C_{H11} and the first holding capacitor C_{H12} are directly connected to the second holding capacitor C_{H2} through the transistor **Tr3** or **Tr4** alone, the charge of the first holding capacitor C_{H11} and the first holding capacitor C_{H12} are distributed to the second holding capacitor C_{H2}. Therefore, in order to avoid the effect due to reduction of the voltage, it is necessary to adjust the timing so that the transistors **Tr1** to **Tr4** are not switched on at the same time as well as keep the capacitance of the second holding capacitor C_{H2} at a sufficiently small value as compared with those of the first holding capacitor C_{H11} and the first holding capacitor C_{H12}.

One electrode of the second holding capacitor C_{H2} and one electrode of a pixel capacitor **Cp** are connected to a ground line **141** through transistors **Tr6** and **Tr7**, respectively. In the configuration of the circuit shown in Figure **28**, the other electrodes of the first holding capacitor C_{H11}, the first holding capacitor C_{H12} and the second holding capacitor C_{H12} are connected to the ground line **141**, thereby keeping their reference voltages at GND level.

One electrode of the second holding capacitor C_{H2} is connected to a gate terminal of the transistor **Tr5**, and a source terminal of the transistor **Tr5** is connected to one electrode of the pixel capacitor **Cp**. A drain terminal of the transistor **Tr5** is connected to a high-voltage line **142** and the other common electrode of the pixel capacitor **Cp** is connected to a common line **143**, thereby constituting a buffer amplifier circuit with a voltage follower circuit.

With the above configuration, regarding the pixel, when a first negative scanning signal **a1** becomes active, the transistor **Tr1** is switched on and the data signal is supplied to the first holding capacitor C_{H11}. Next, a second negative scanning signal **a2** becomes active, the transistor **Tr3** is switched on and the charge is distributed to the second holding capacitor C_{H2}. When a first positive scanning signal **b1** becomes active, the transistor **Tr2** is switched on and the data signal is supplied to the first holding capacitor C_{H12}. Next, when a second positive scanning signal **b2** becomes active, the transistor **Tr4** is turned on and the charge is distributed to the second holding capacitor C_{H2}. Before the second positive scanning signal **b2** becomes active, a refresh signal **c1** becomes active so as to switch the transistors **Tr6** and **Tr7** on and discharge the second holding capacitor C_{H2} and the pixel capacitor **Cp**. Then, the transistor **Tr5** supplies the current to the pixel capacitor **Cp** from the high voltage line **142** to charge the pixel capacitor **Cp** in accordance with the voltage of the second holding capacitor C_{H2}, to which the charge is distributed. The pixel capacitor **Cp** is charged until the voltage of the pixel capacitor **Cp** becomes lower than that of the second holding capacitor C_{H2} by the threshold voltage of the transistor **Tr5**. Thereafter, it is possible to maintain the voltage of the pixel capacitor **Cp** by compensating the charge due to the leak current. In the configuration of the circuit, when the transistors **Tr3** and **Tr4** are activated, the charge in the first capacitors for holding is discharged to the second holding capacitor. At the same time, the voltage is applied to the transistor **Tr5** in accordance with the signal (charge), thereby supplying the voltage to the liquid crystal layer. The field sequential color mixing method can be more easily realized by using the silicon substrate as a back face substrate of the light crystal display element of the projection-type liquid crystal display device shown in the sixth example.

The liquid crystal display driving waveform described in the second and the third examples are applied to the liquid crystal after the application of the refresh signal **c1**. At this moment, it is desirable to apply the first preliminary voltage V_H and the second preliminary voltage V_L to all the pixel capacitors constituting the entire image at the same time. It is desirable that the time period from the application of the second preliminary voltage V_L to the application of the signal voltage V_{on} of the display signal is short. In this example, it is possible to make the time period approximately zero, and therefore to eliminate the unevenness of the display image.

Although the configuration of the circuit as shown in Figure **28** is used in this example, the configuration is not limited as long as the similar effect can be obtained.

As described above, according to the present invention, the liquid crystal display device is driven by applying the voltage to the pixels in the field sequential addressing method so that optical on/off is carried out between the voltages corresponding to the maximum light transmittance and the minimum light transmittance in the V-T characteristic in the case: $d \times \Delta n > \lambda/2$, where the thickness of the liquid crystal layer is d, the birefringence for the liquid crystal layer is Δn, and the wavelength of light for display is λ. As a result, although the orientational deformation of the liquid crystal molecules is small, the liquid crystal display having a sufficient response speed and a sufficient contrast ratio can be obtained.

If the driving voltage waveform applying the first preliminary voltage having an absolute value larger than at least that of the signal voltage before applying the signal voltage for obtaining the predetermined transmittance or reflectance to the pixels, the sufficient optical response of the liquid crystal display is obtained. If the time period for applying the second preliminary voltage is provided between the time periods for applying the first preliminary voltage and the signal voltage, the deformation in the waveform of the optical response characteristic is eliminated, thereby increasing the optical response speed.

If a retardation compensation means for compensating the retardation which is the optical path difference in both substrates and the liquid crystal layer between the ordinary components and the extraordinary components is provided, the same optical response characteristic is obtained even with a lower driving voltage.

Furthermore, if the silicon single crystalline substrate is used for a substrate of the liquid crystal device and the transistor for driving pixels are formed in the single crystalline silicon, far excellent TFTs, as compared with amorphous silicon thin film TFTs or polysilicon TFTs can be obtained since the single crystalline silicon has a large mobility.

The light modulating elements which respond with high speed and the spatial light modulating elements such as projection-type liquid crystal display device and arithmetic device capable of being driven by the field sequential addressing method can be obtained by driving the liquid crystal device in accordance with the above procedure. If, for example, a CCD and the high-speed light modulating element are combined, a compact CCD element with high precision can be obtained since signals of red, green and blue can be detected by one pixel of the CCD.

As described above, since the liquid crystal display mode having high-speed response and capable of display half tone is realized, the liquid crystal devices such as a color liquid crystal display device capable of being driven by the field sequential addressing method can be obtained. In addition, the liquid crystal device according to the invention is suitable for an image input device using the liquid crystal device as a spatial light modulation element, which is used for an optical computing system.

Various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope and spirit of this invention. Accordingly, it is not intended that the scope of the claims appended hereto be limited to the description as set forth herein, but rather that the claims be broadly construed.

Claims

1. A liquid crystal device comprising:
   a pair of substrates;
   a liquid crystal layer interposed between the pair of substrates;
   at least one polarizing element;
   a plurality of pixels;
   a retardation ($d \times \Delta n$) of the liquid crystal layer satisfying one of a relation:
   $$d \times \Delta n > \lambda/2$$
   in a case where an incident light is output after passing through the liquid crystal layer once, and a relation:
   $$2d \times \Delta n > \lambda/2$$
   in a case where the incident light is outputted after passing through the liquid crystal layer twice, where a thickness of the liquid crystal layer is d, a birefringence is Δn and a wavelength of the light incident on the liquid crystal layer is λ; and
   driving voltage applying means for applying a driving voltage including a voltage higher than a maximum voltage providing an extremum of the output light intensity in a voltage-output light intensity characteristic of the pixels to the plurality of pixels.

2. A liquid crystal device according to claim 1, wherein the driving voltage applying means applies the driving voltage to the pixels by a field sequential addressing method.

3. A liquid crystal device according to claim 2, includes retardation compensation means between the liquid crystal layer and the polarizing element.

4. A liquid crystal device according to claim 1, wherein the driving voltage applying means applies a voltage higher than the maximum voltage providing the extremum of the output light intensity in the voltage-output light intensity characteristic and a voltage between the voltage higher than the maximum voltage and the maximum voltage, thereby controlling the output light intensity of the pixels.

5. A liquid crystal device according to claim 1, wherein the driving voltage applying means reverses a polarity of the driving voltage in each frame.

6. A liquid crystal device according to claim 1, wherein the driving voltage applying means applies a first preliminary voltage having an absolute value larger than that of a signal voltage corresponding to a predetermined output light intensity before applying the signal voltage to the pixels.

7. A liquid crystal device according to claim 6, wherein the driving voltage applying means further applies a second preliminary voltage having an absolute value smaller than that of the signal voltage before applying the signal voltage corresponding to the predetermined output light intensity and after applying the first preliminary voltage.

8. A liquid crystal device according to claim 6, wherein the absolute value of the first preliminary voltage is larger than that of the maximum voltage providing an extremum in the voltage-output light intensity characteristic of the pixels.

9. A liquid crystal device according to claim 6, wherein the output light intensity at a maximum value of the signal voltage is equal to or less than 10% of a maximum in the voltage-output light intensity characteristic of the pixels.

10. A liquid crystal device according to claim 7, wherein the absolute value of the second preliminary voltage is smaller than that of the maximum voltage providing the extremum in the voltage-output light intensity characteristic of the pixels.

11. A liquid crystal device according to claim 6, wherein a time period for applying the first preliminary voltage is one-fifth or less than that for applying the signal voltage.

12. A liquid crystal device according to claim 7, wherein a sum of the time period for applying the first preliminary voltage and the time period for applying the second preliminary voltage is one-fifth or less than a time period for applying the signal voltage.

13. A liquid crystal device according to claim 6, wherein the driving voltage applying means applies the first preliminary voltage to the pixels connected to each scanning line at the same time.

14. A liquid crystal device according to claim 6, wherein the driving voltage applying means applies the first preliminary voltage to the pixels connected to at least one scanning line.

15. A liquid crystal device according to claim 7, wherein the driving voltage applying means applies the first preliminary voltage and the second preliminary voltage to the pixels connected to at least one scanning line for display.

16. A liquid crystal device according to claim 6, wherein a value of the first preliminary voltage is identical to all the pixels.

17. A liquid crystal device according to claim 7, wherein at least one of the first preliminary voltage and the second preliminary voltage has an identical value for all the pixels.

18. A liquid crystal device according to claim 3, wherein the retardation compensation means has at least a pair of substrates and a second liquid crystal layer interposed therebetween, and an electro-optical characteristic of the second liquid crystal layer is substantially identical with that of the liquid crystal layer.

19. A liquid crystal device according to claim 3, wherein the retardation compensation means is selected from a phase plate and a phase film.

20. A liquid crystal device according to claim 19, wherein the retardation compensation means is selected from a uniaxially oriented polymer film and a biaxially oriented film.

21. A liquid crystal device according to claim 1, wherein one of the pair of substrates is a silicon single crystalline substrate, and the silicon single crystalline substrate has a transistor switching a voltage applied from the driving voltage applying means to each of the plurality of pixels.

22. A projection-type liquid crystal display device including a liquid crystal element, wherein the liquid crystal element comprising:
a pair of substrates;
a liquid crystal layer interposed between the pair of substrates;
at least one polarizing element;
a plurality of pixels;
a retardation (d x Δn) of the liquid crystal layer satisfying one of a relation:

$$d \times \Delta n > \lambda/2$$

in a case where an incident light is output after passing through the liquid crystal layer once, and a relation:

$$2d \times \Delta n > \lambda/2$$

in a case where the incident light is outputted after passing through the liquid crystal layer twice, where a thickness of the liquid crystal layer is d, a birefringence is Δn and a wavelength of the light incident on the liquid crystal layer is λ; and
driving voltage applying means for applying a driving voltage including a voltage higher than a maximum voltage providing an extremum of the output light intensity in a voltage-output light intensity characteristic of the pixels to the plurality of pixels.

23. A method for driving a liquid crystal device including: a pair of substrates; a liquid crystal layer interposed between the pair of substrates; at least one polarizing element; a plurality of pixels; and a retardation (d x Δn) of the liquid crystal layer satisfying one of a relation:

$$d \times \Delta n > \lambda/2$$

in a case where an incident light is output after passing through the liquid crystal layer once, and a relation:

$$2d \times \Delta n > \lambda/2$$

in a case where the incident light is outputted after passing through the liquid crystal layer twice, where a thickness of the liquid crystal layer is d, a birefringence is Δn and a wavelength of the light incident on the liquid crystal layer is λ,
wherein the method comprises a step of applying a driving voltage including a voltage higher than a maximum voltage providing an extremum of the output light intensity in a voltage-output light intensity characteristic of the pixels to the plurality of pixels.

24. A method according to claim 23, wherein the driving voltage applying step includes applying the driving voltage to the pixels by a field sequential addressing method.

25. A method according to claim 23, wherein the driving voltage applying step includes applying a voltage higher than the maximum voltage providing the extremum of the output light intensity in the voltage-output light intensity characteristic and a voltage between the voltage higher than the maximum voltage and the maximum voltage, thereby controlling the output light intensity of the pixels.

26. A method according to claim 23, wherein a polarity of the driving voltage is reversed in each frame.

27. A method according to claim 23, wherein the driving voltage applying step includes applying a first preliminary voltage having an absolute value larger than that of a signal voltage corresponding to a predetermined output light intensity before applying the signal voltage to the pixels.

28. A method according to claim 27, wherein the driving voltage applying step further includes applying a second preliminary voltage having an absolute value smaller than that of the signal voltage before applying the signal voltage corresponding to the predetermined output light intensity and after applying the first preliminary voltage.

29. A method according to claim 27, wherein the absolute value of the first preliminary voltage is larger than that of the maximum voltage providing an extremum in the voltage-output light intensity characteristic of the pixels.

30. A method according to claim 28, wherein the absolute value of the second preliminary voltage is smaller than that of the maximum voltage providing the extremum in the voltage-output light intensity characteristic of the pixels.

31. A method according to claim 27, wherein a time period for applying the first preliminary voltage is one-fifth or less than that for applying the signal voltage.

32. A method according to claim 28, wherein a sum of the time period for applying the first preliminary voltage and the time period for applying the second preliminary voltage is one-fifth or less than a time period for applying the signal voltage.

33. A method according to claim 27, wherein the driving voltage applying step includes applying the first preliminary voltage to the pixels connected to each scanning line at the same time.

34. A method according to claim 27, wherein the driving voltage applying step includes applying the first preliminary voltage to the pixels connected to at least one scanning line.

35. A method according to claim 28, wherein the driving voltage applying step includes applying the first preliminary voltage and the second preliminary voltage to the pixels connected to at least one scanning line for display.

36. A method according to claim 27, wherein a value of the first preliminary voltage is identical to all the pixels.

37. A method according to claim 28, wherein at least one of the first preliminary voltage and the second preliminary voltage has an identical value for all the pixels.

FIG. 1

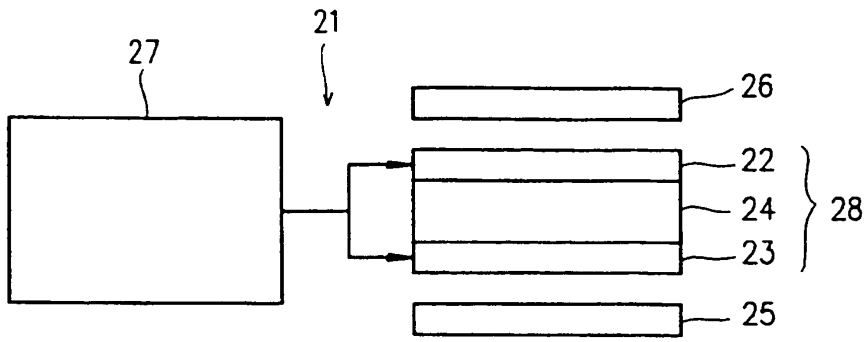

21
27
26
22
24
23
28
25

FIG. 2

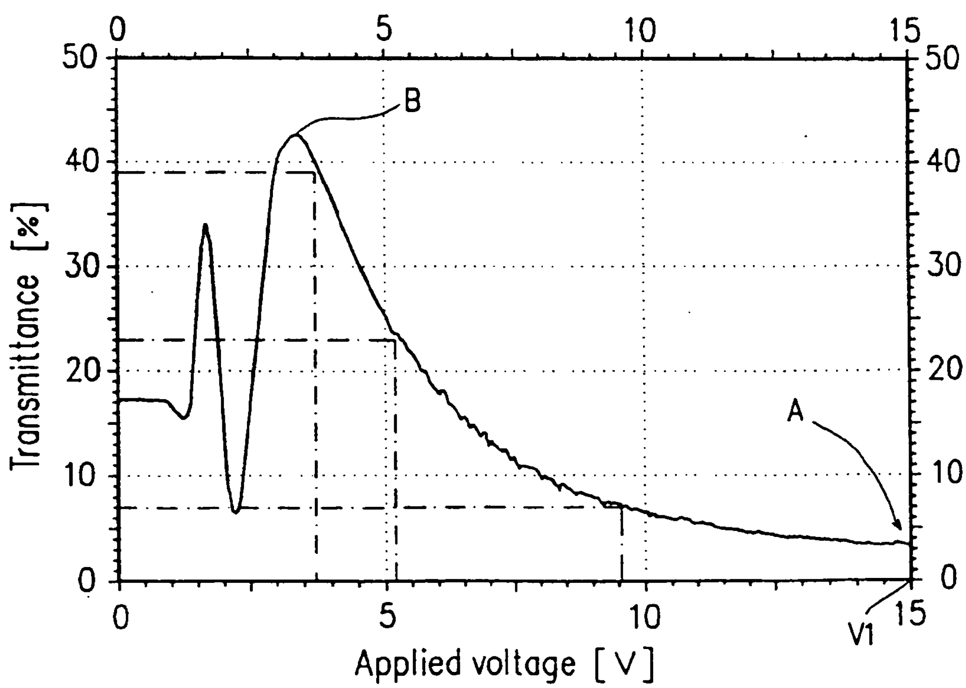

0
5
10
15
50
40
30
20
10
0
B
A
V1
Transmittance [%]
Applied voltage [V]

FIG.3A FIG.3B FIG.3C

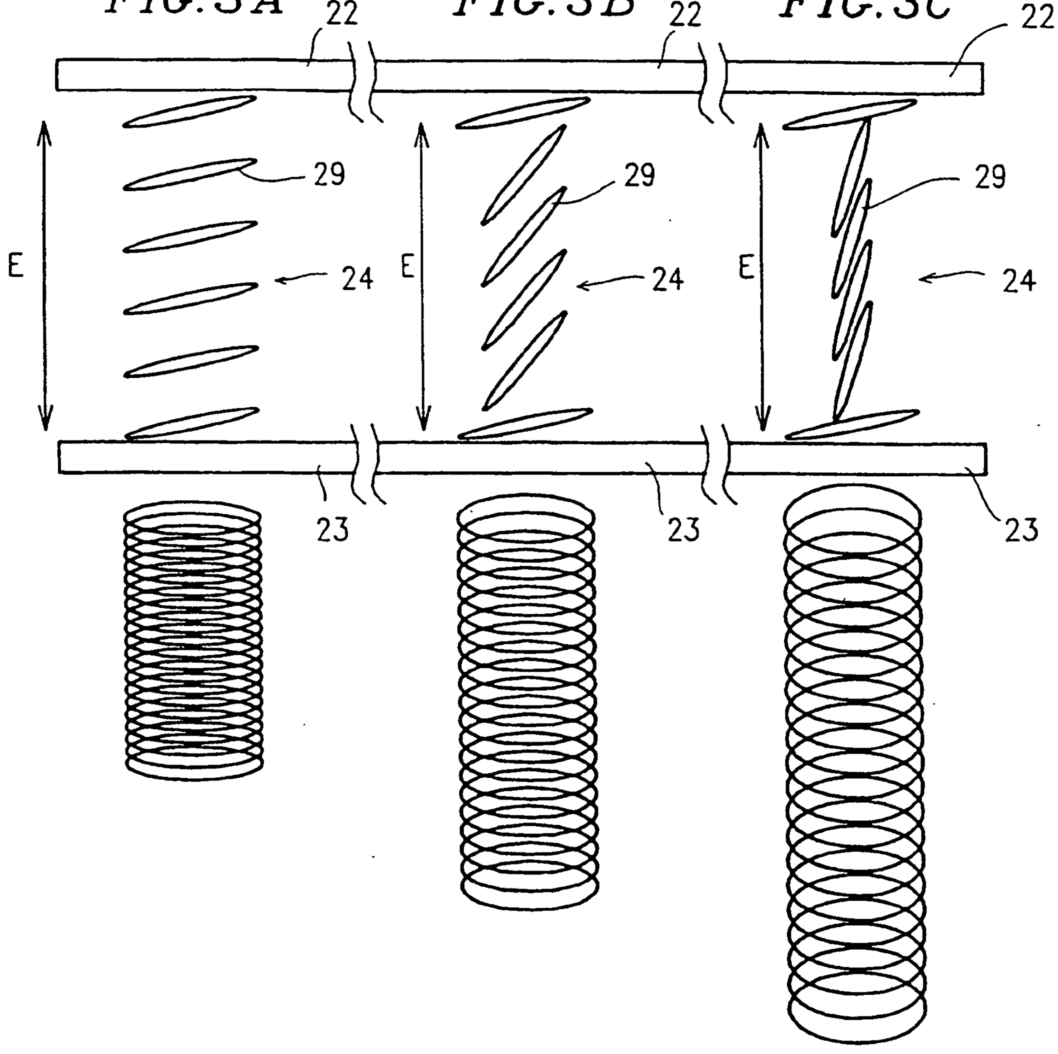


FIG. 4A

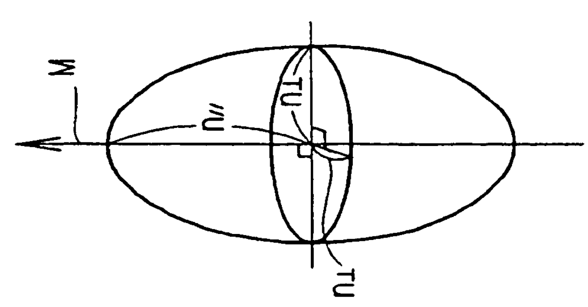


FIG. 4B

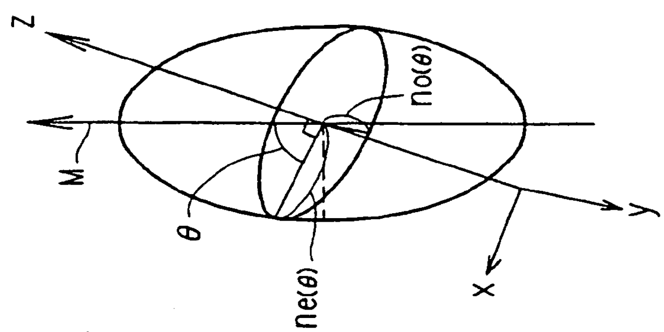


FIG. 4C

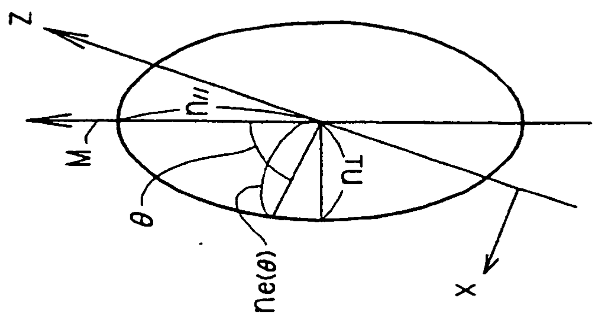


FIG. 5

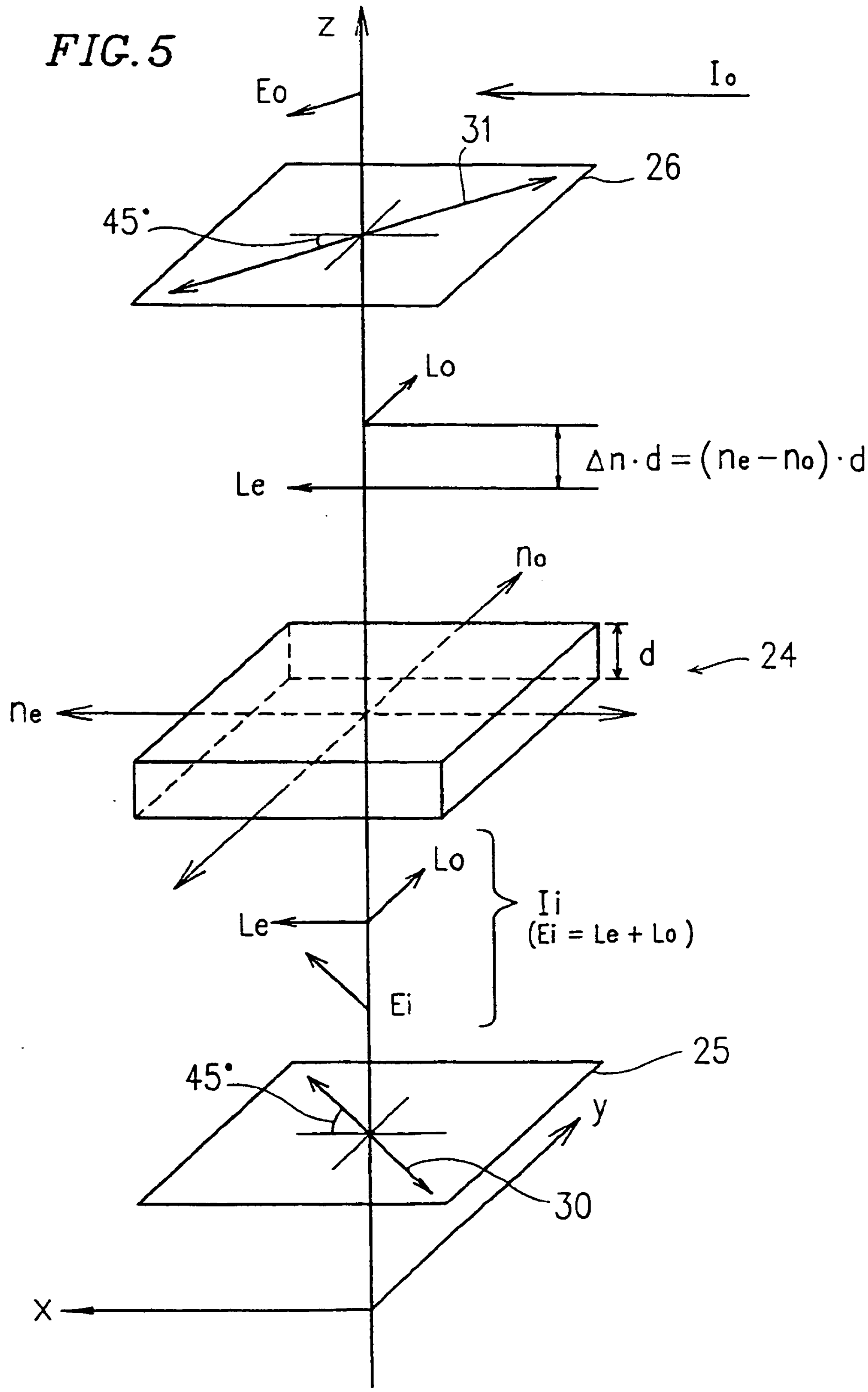

Z
Eo
Io
31
26
45°
Lo
Δn·d=(ne−no)·d
Le
no
d
24
ne
Lo
Ii
(Ei = Le + Lo)
Le
Ei
25
45°
y
30
X

FIG. 6

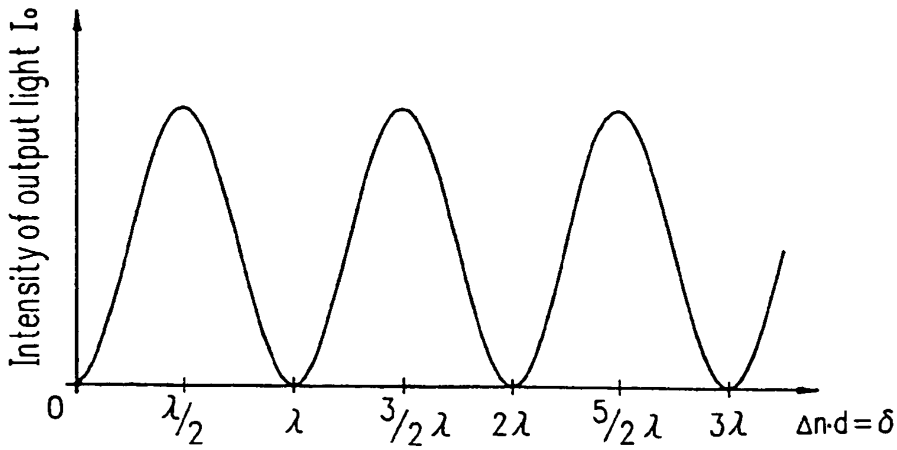

Intensity of output light Io
0
λ/2
λ
3/2 λ
2λ
5/2 λ
3λ
Δn·d = δ

FIG. 7

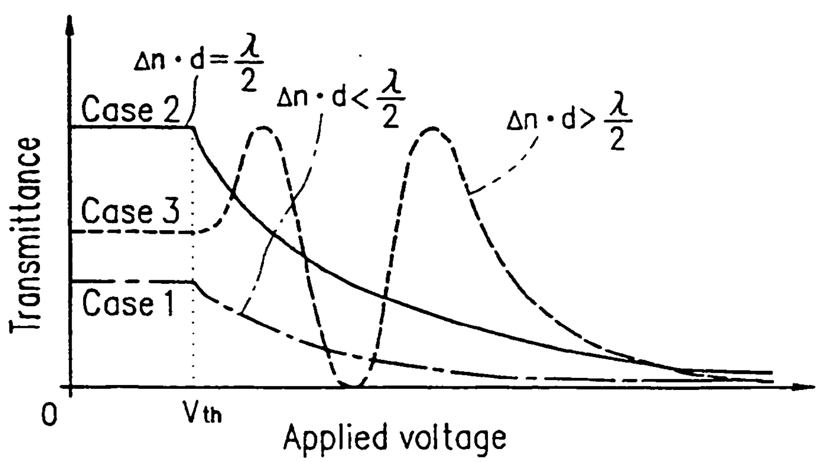

Δn · d = λ/2
Δn · d < λ/2
Δn · d > λ/2
Case 2
Case 3
Case 1
Transmittance
0
Vth
Applied voltage

FIG.8

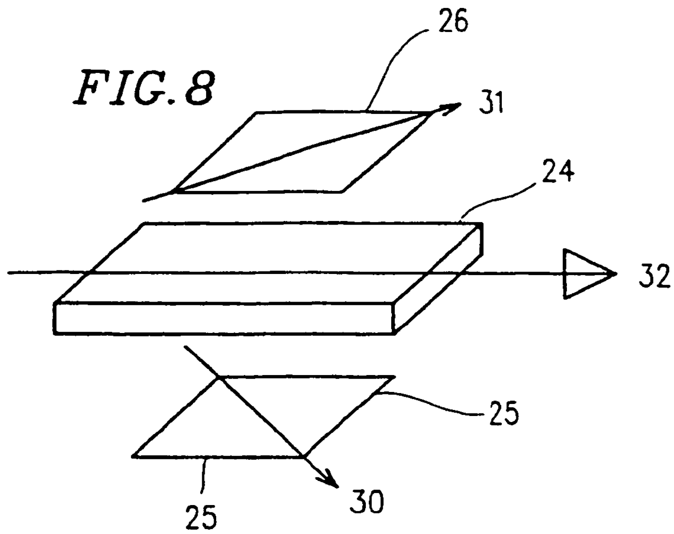

26
31
24
32
25
25
30

FIG.9

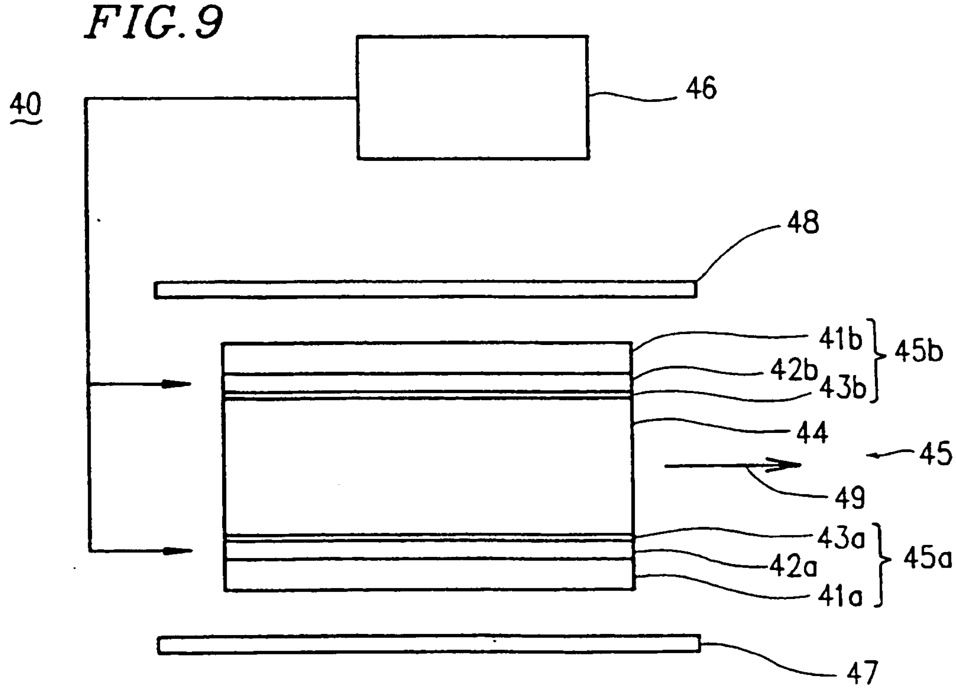

40
46
48
41b
42b
43b
45b
44
45
49
43a
42a
41a
45a
47

FIG.10A

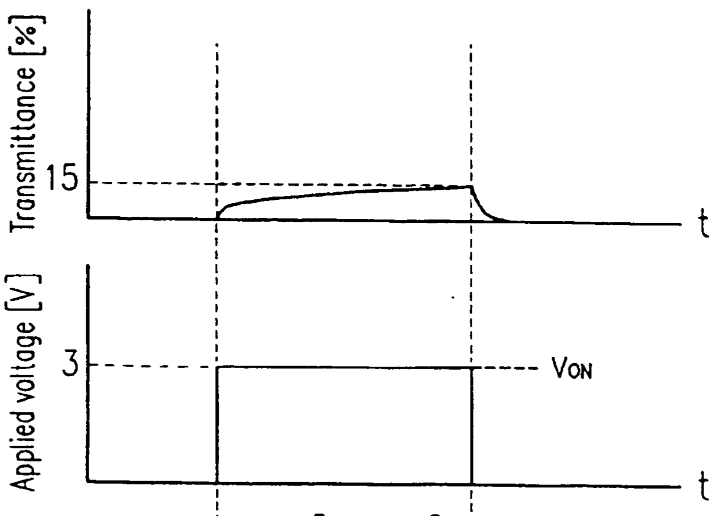


FIG.10B

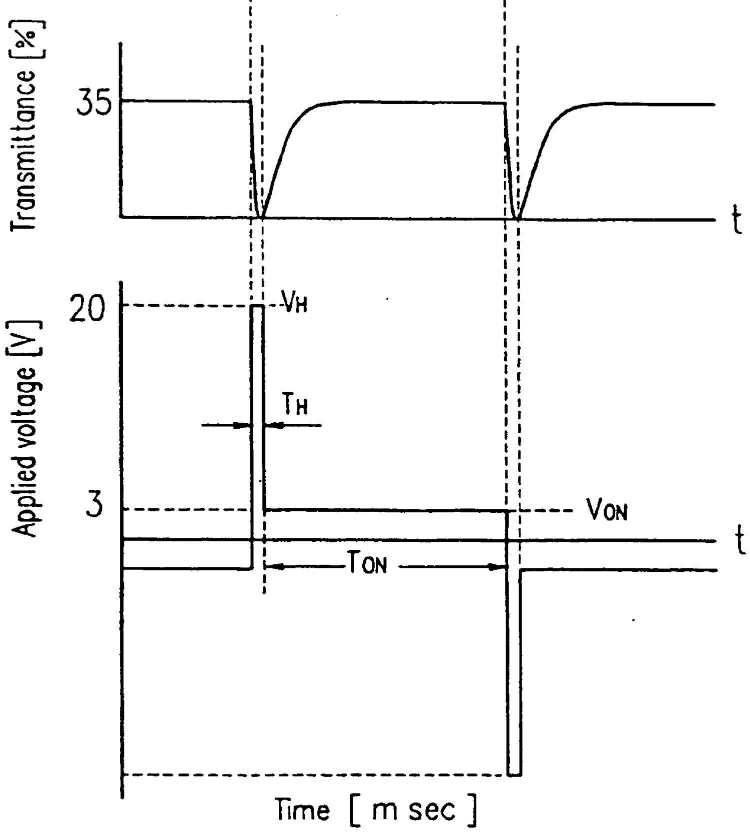


FIG.11A

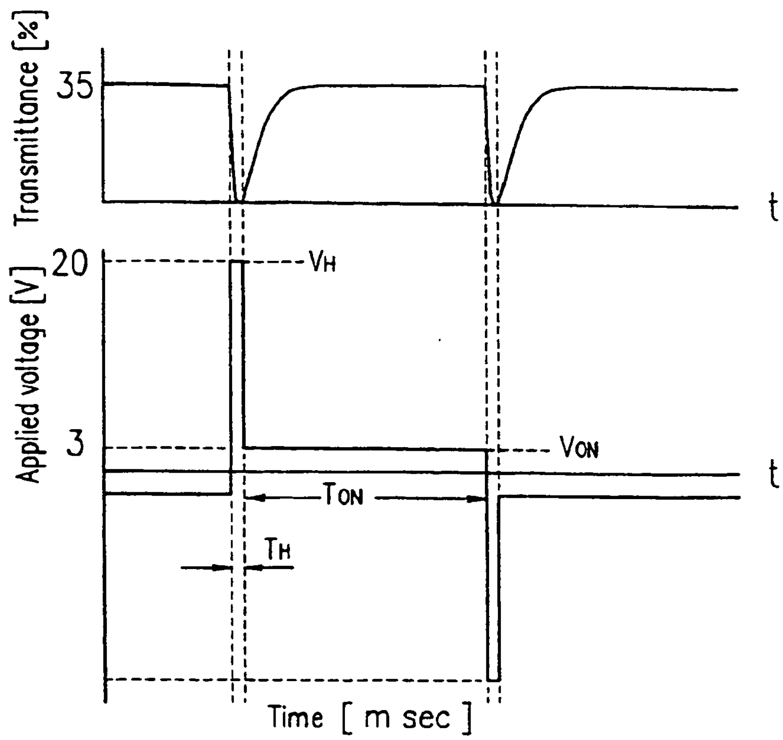


FIG.11B

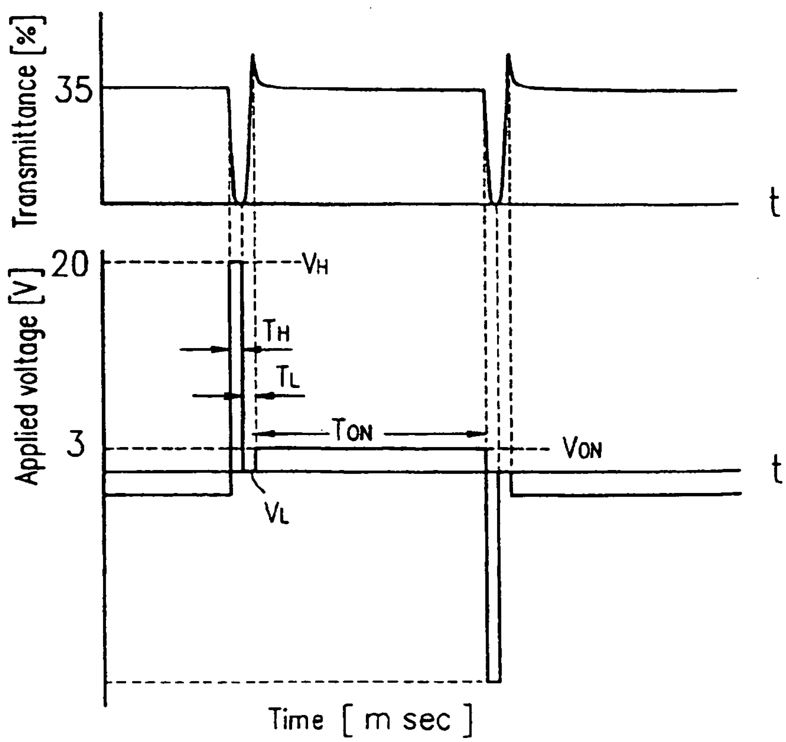


FIG.12

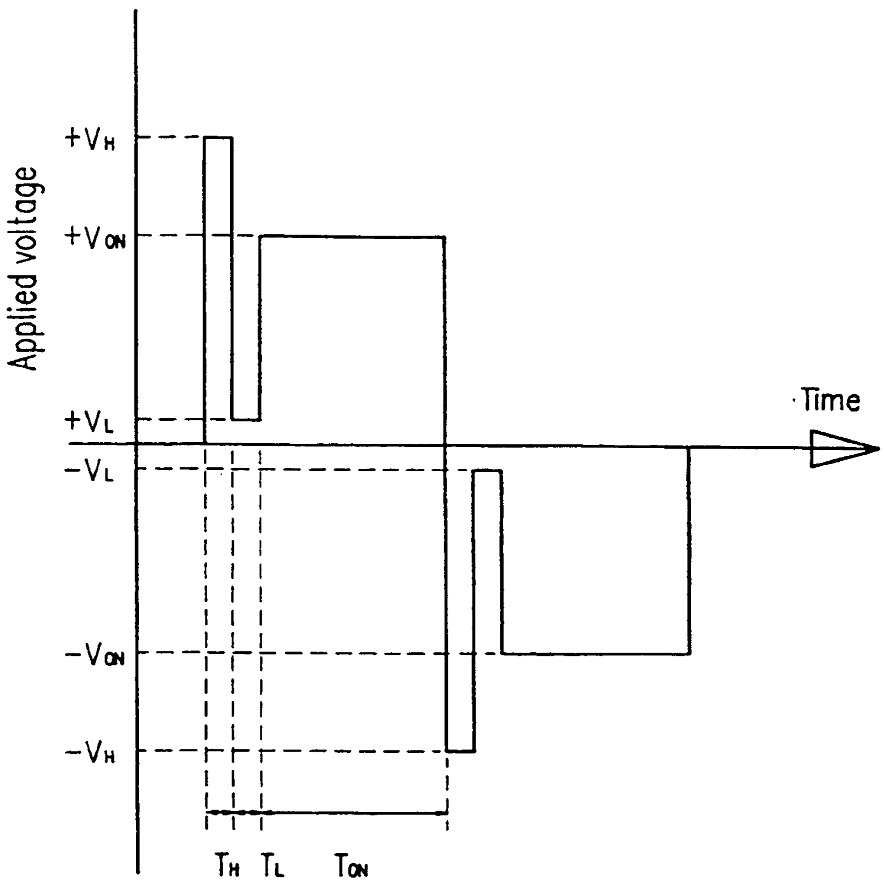


FIG.13

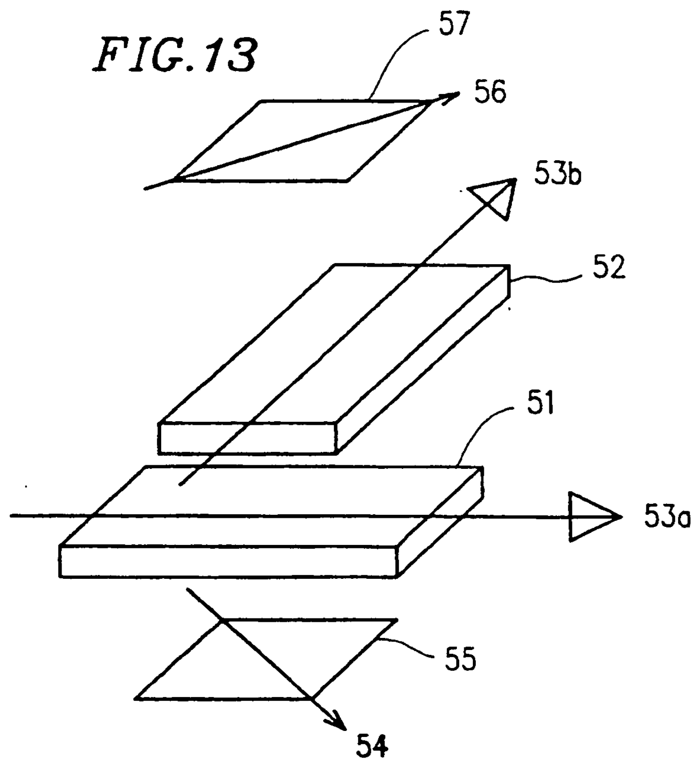


FIG.14

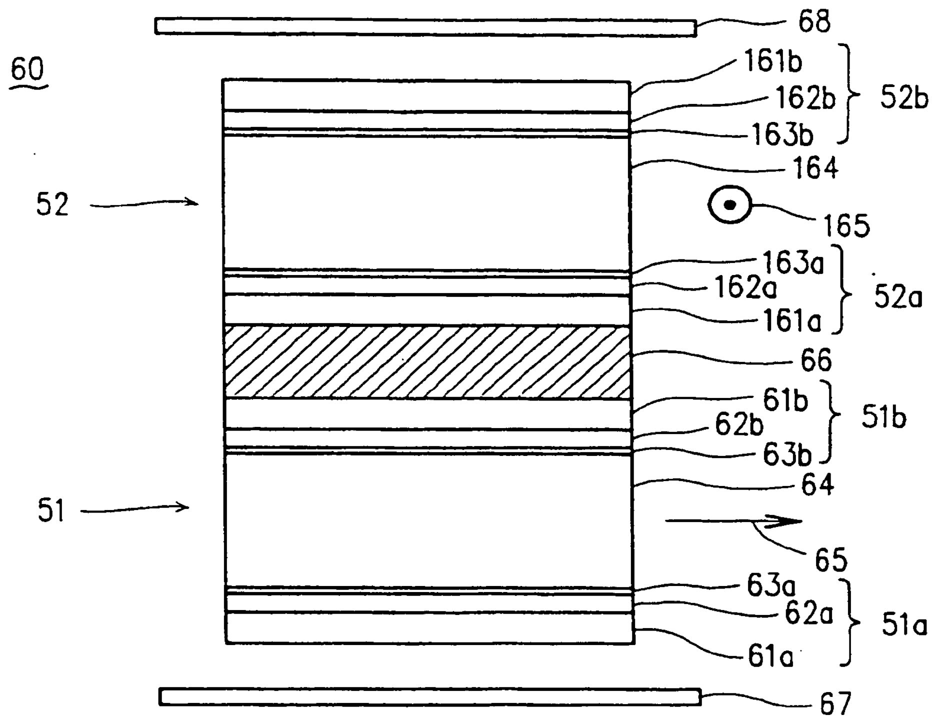

68
60
161b
162b
163b
52b
164
52
165
163a
162a
161a
52a
66
61b
62b
63b
51b
64
51
65
63a
62a
61a
51a
67

FIG.15

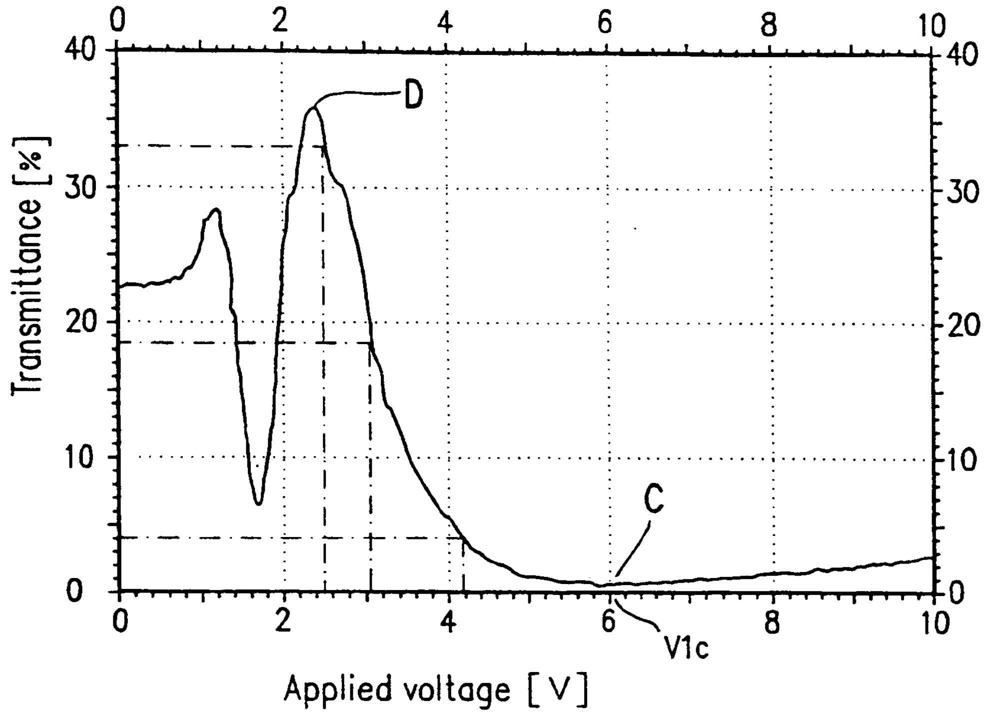


FIG.16A

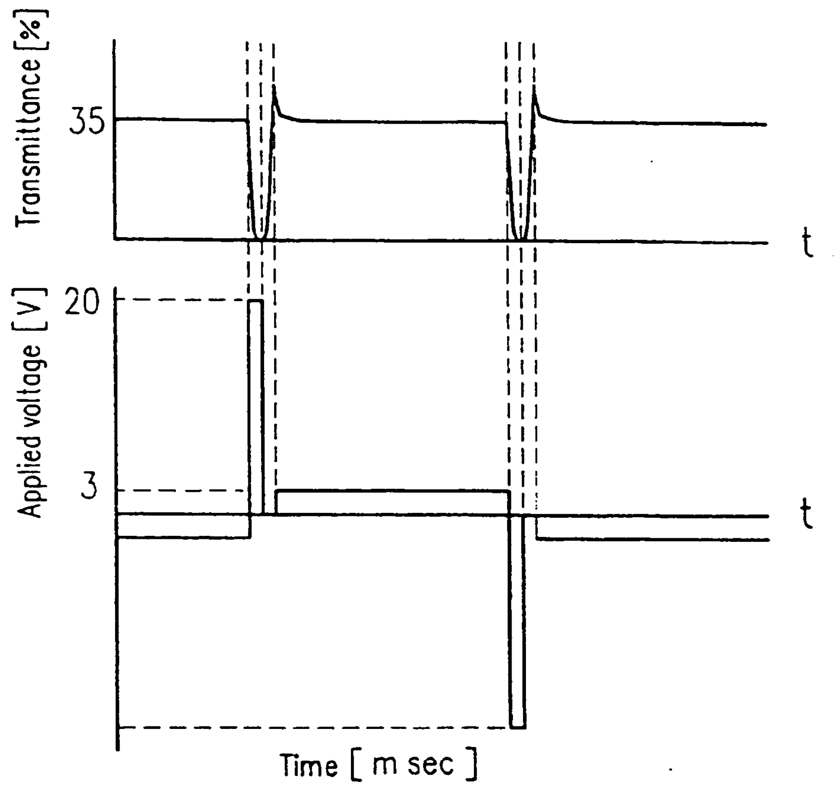


FIG.16B

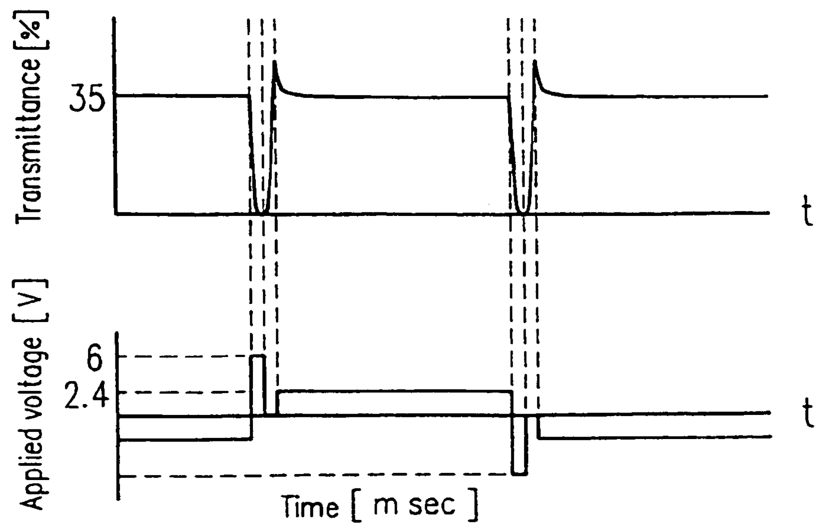


FIG.17

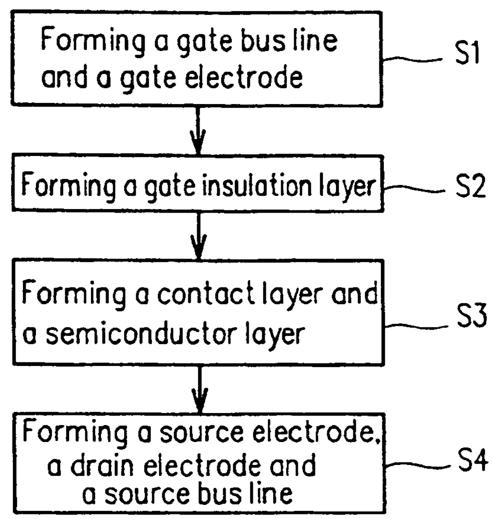

Forming a gate bus line and a gate electrode
S1
Forming a gate insulation layer
S2
Forming a contact layer and a semiconductor layer
S3
Forming a source electrode, a drain electrode and a source bus line
S4

FIG.18

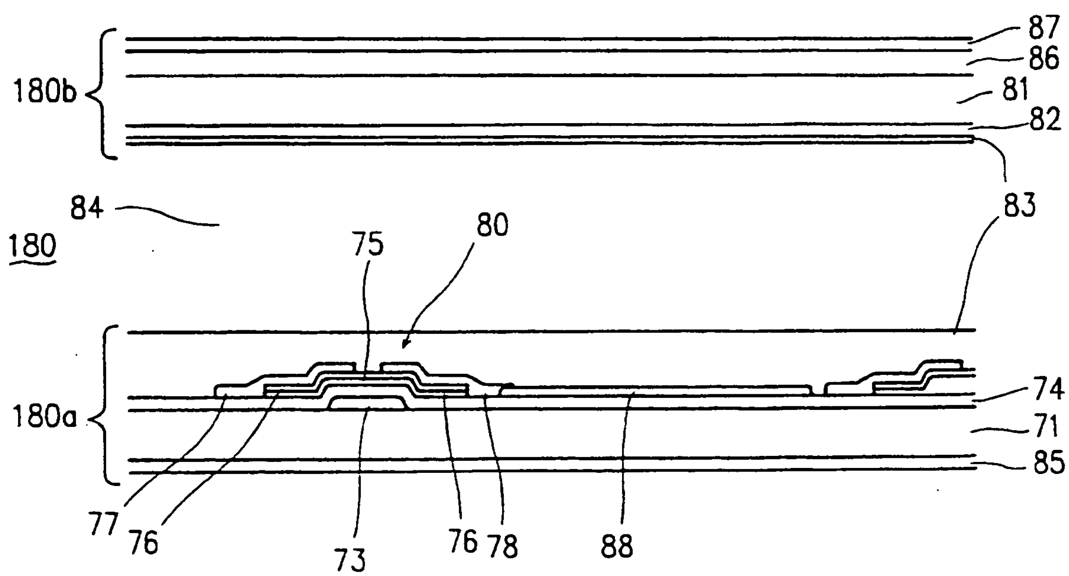

87
86
180b
81
82
83
84
180
80
75
83
74
180a
71
85
77
76
73
76
78
88

FIG.19

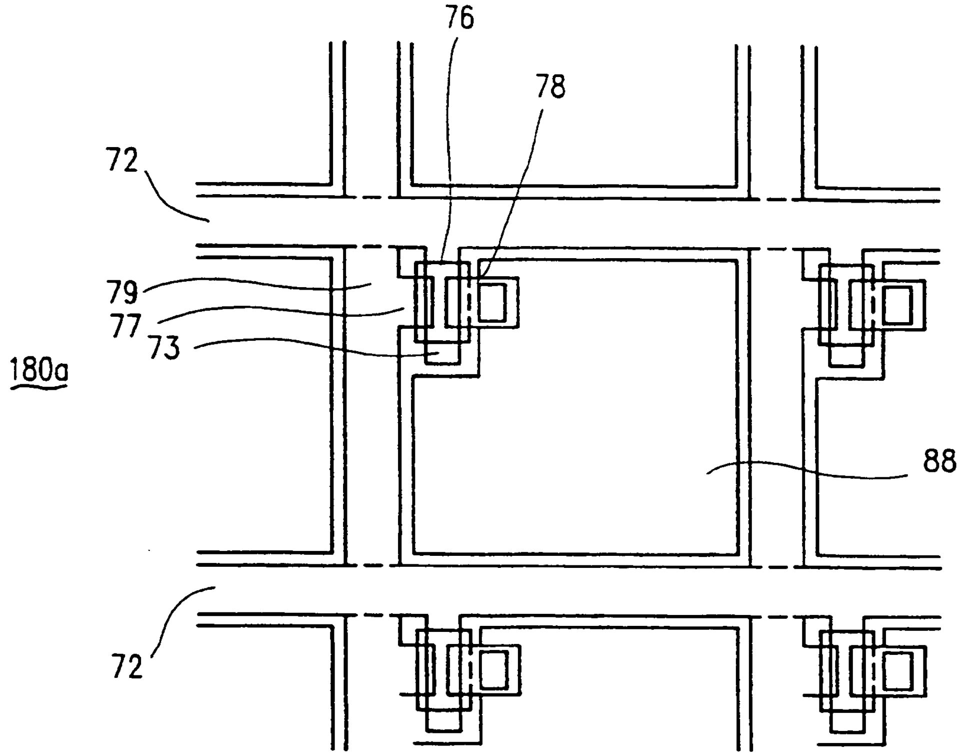
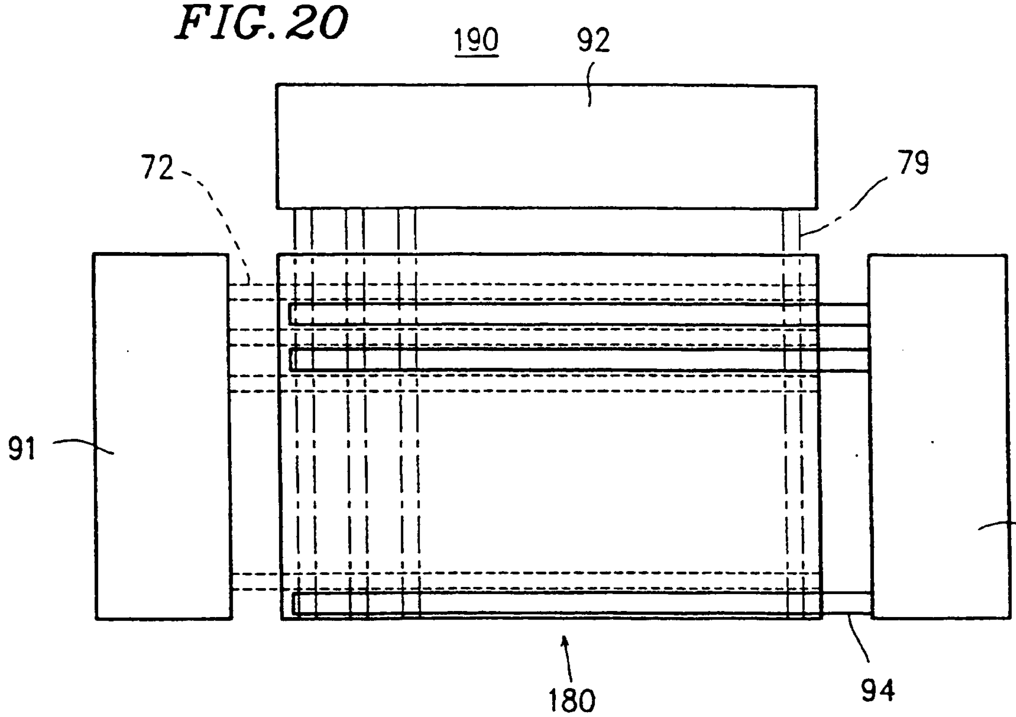


FIG. 20



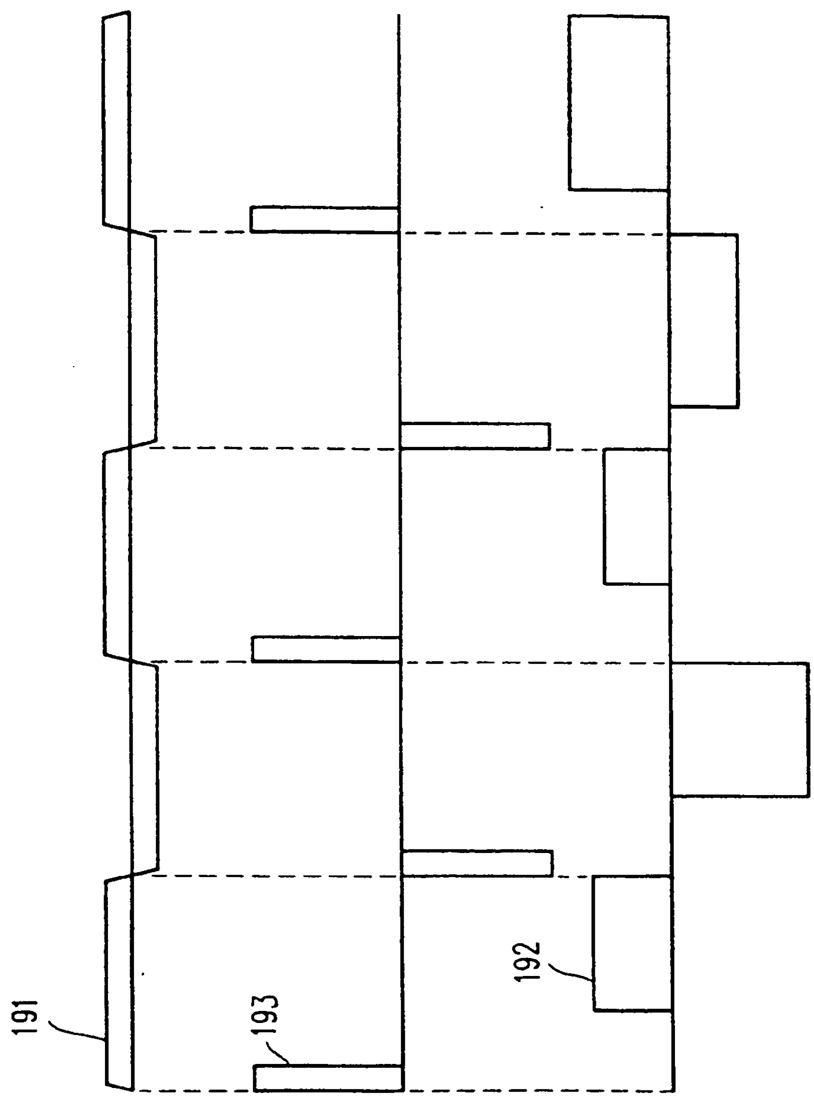


FIG.21A

FIG.21B

FIG.21C

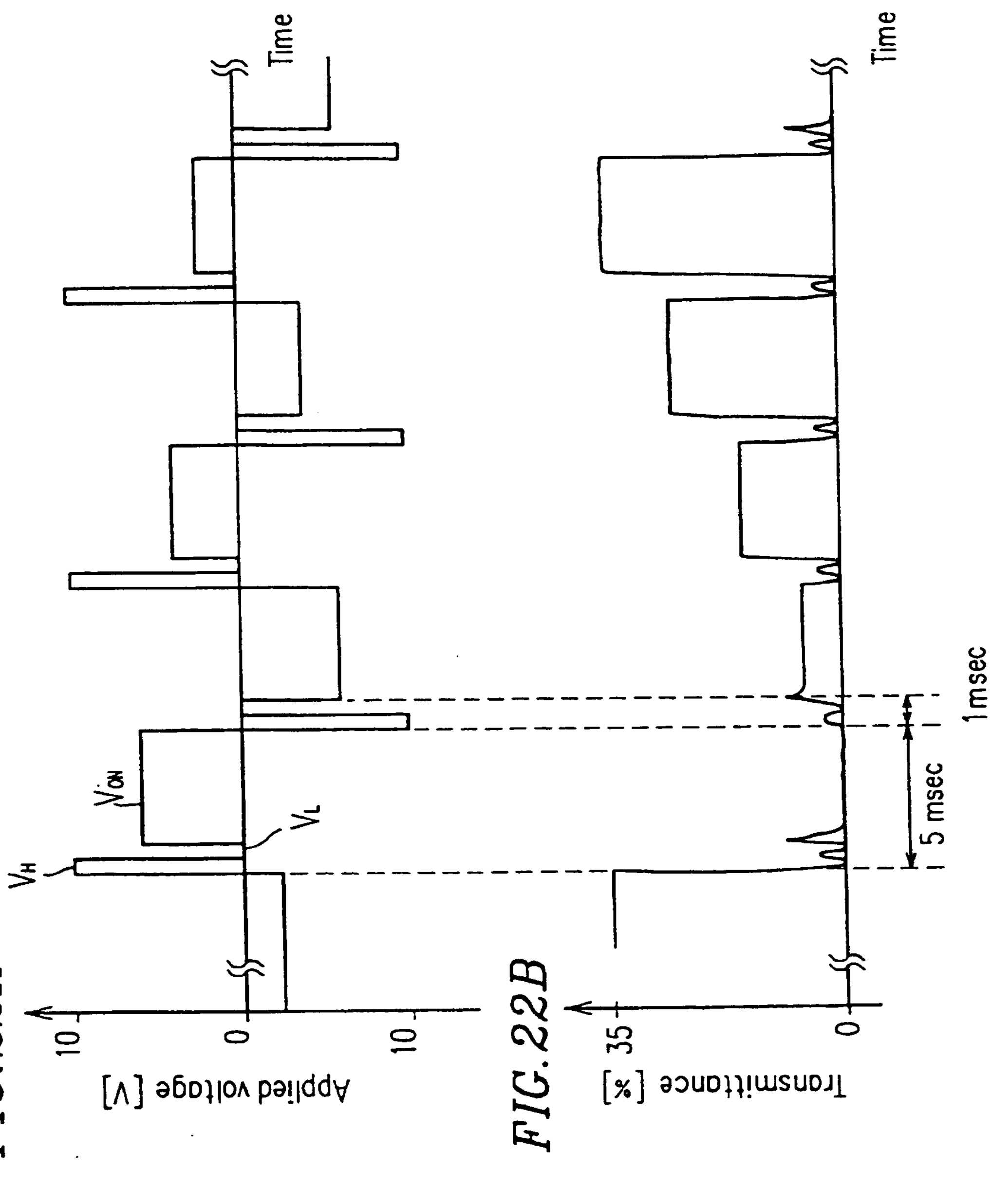
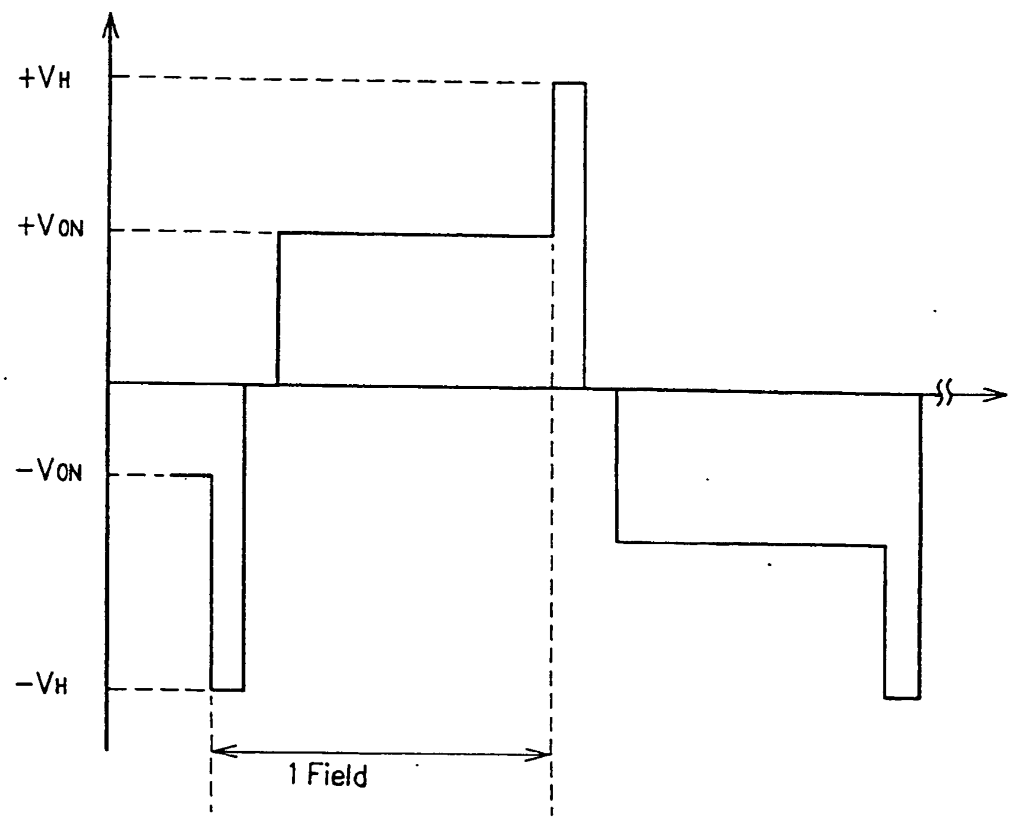


FIG. 22A

FIG. 22B

FIG. 23



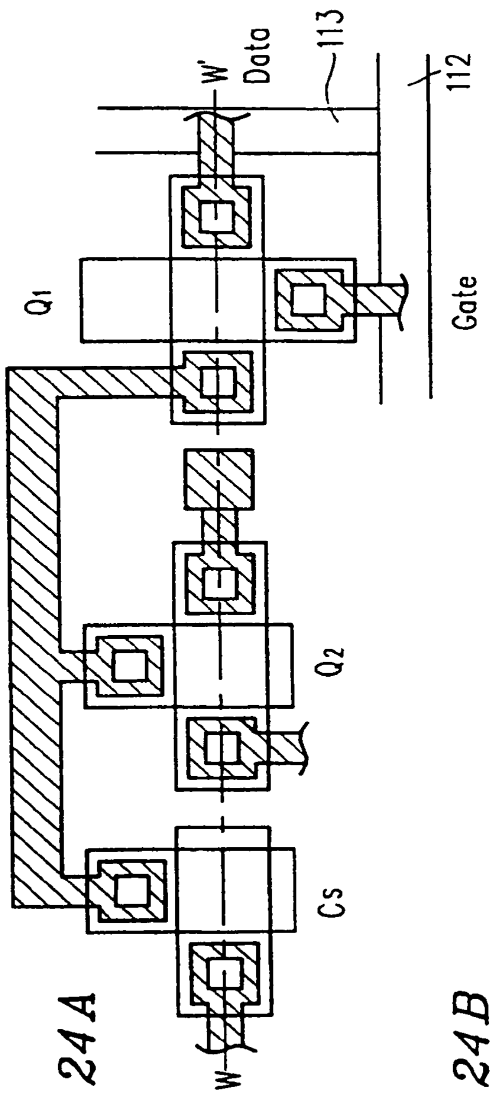


FIG.24A

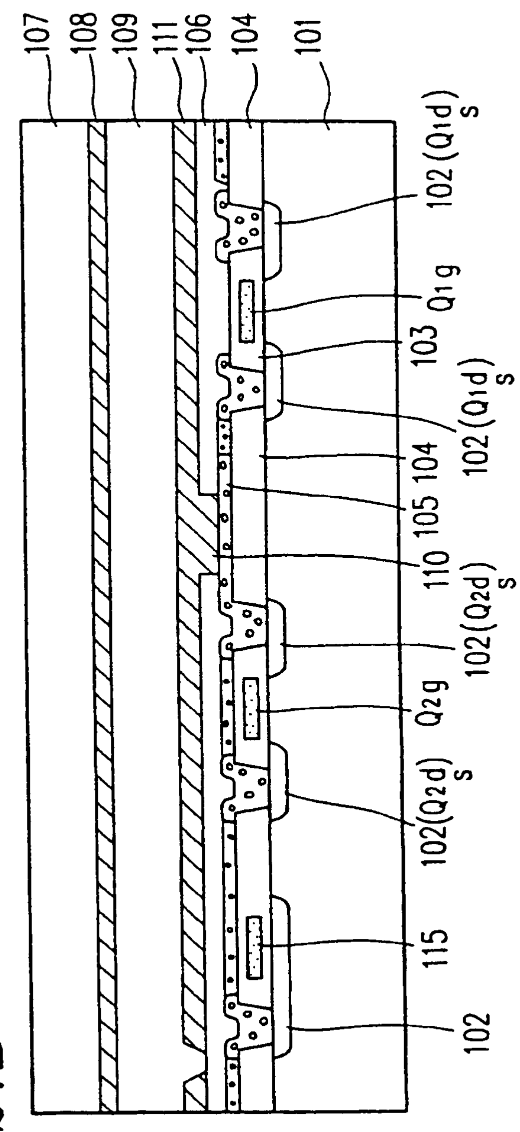


FIG.24B

FIG. 25

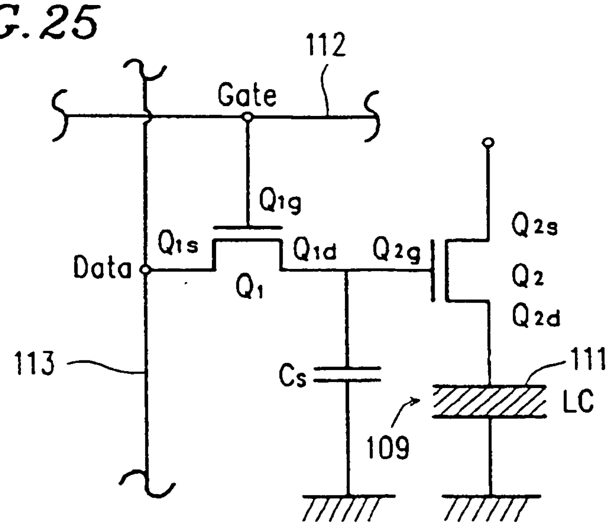


FIG. 26 A

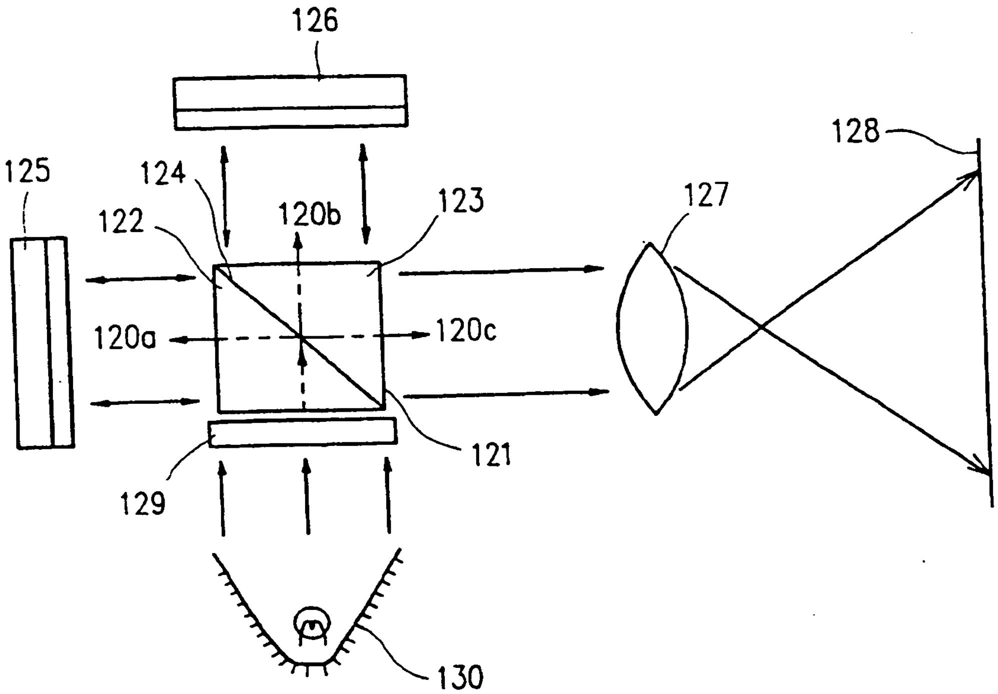


FIG. 26 B

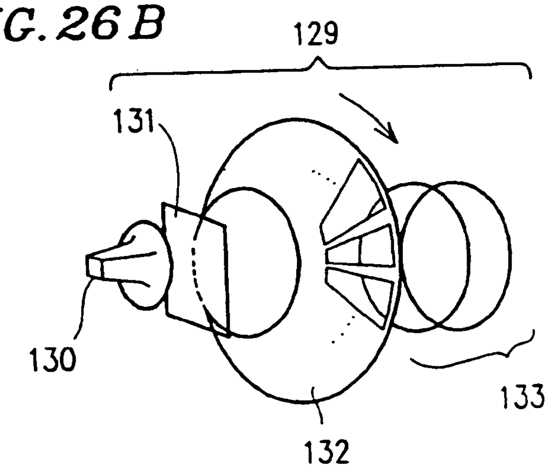


FIG. 27

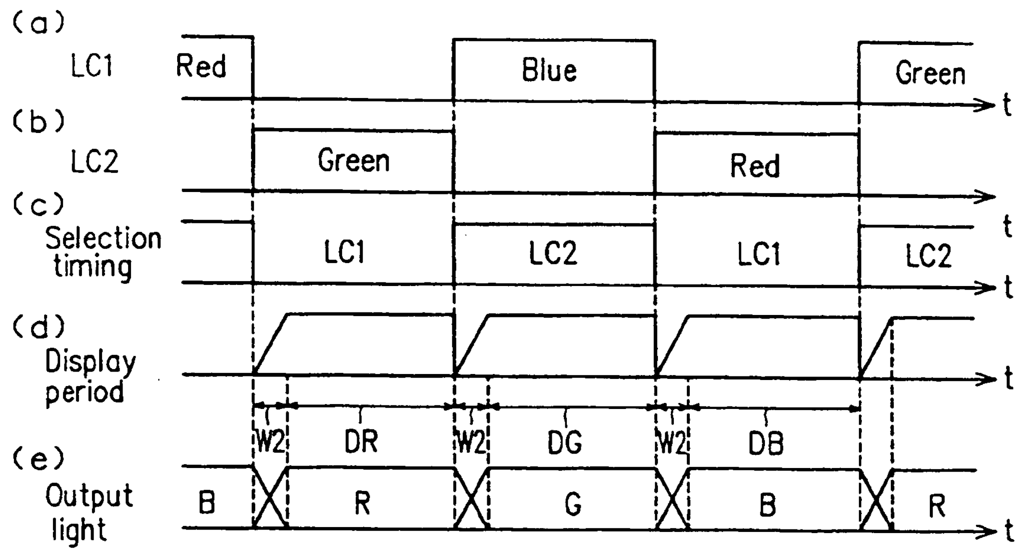

(a)
LC1
Red
Blue
Green
t
(b)
LC2
Green
Red
(c)
Selection timing
LC1
LC2
LC1
LC2
t
(d)
Display period
t
W2
DR
W2
DG
W2
DB
(e)
Output light
B
R
G
B
R
t

FIG. 28

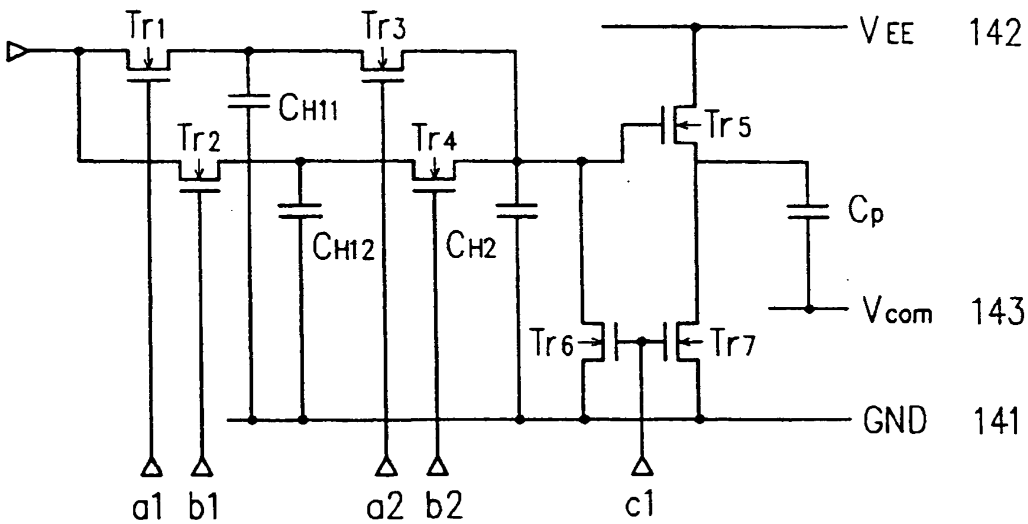

Tr1
Tr3
VEE
142
CH11
Tr2
Tr4
Tr5
Cp
CH12
CH2
Vcom
143
Tr6
Tr7
GND
141
a1
b1
a2
b2
c1

FIG. 29

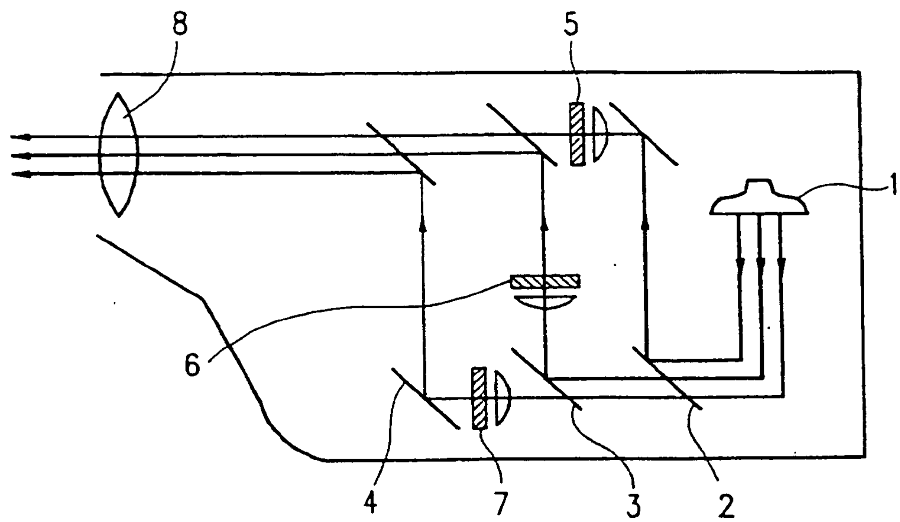
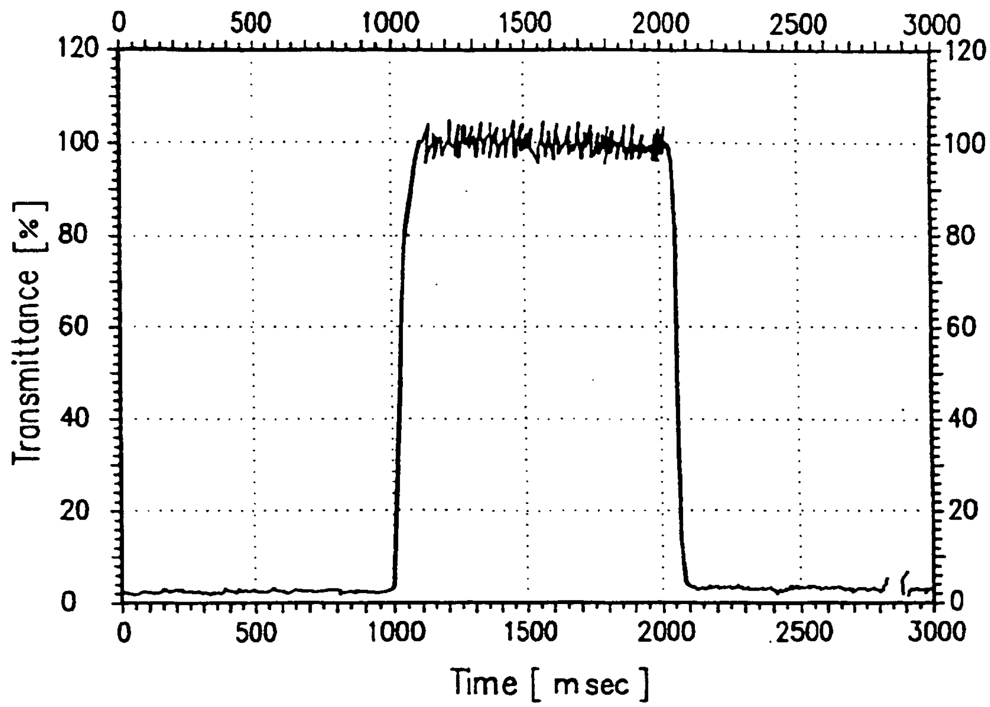
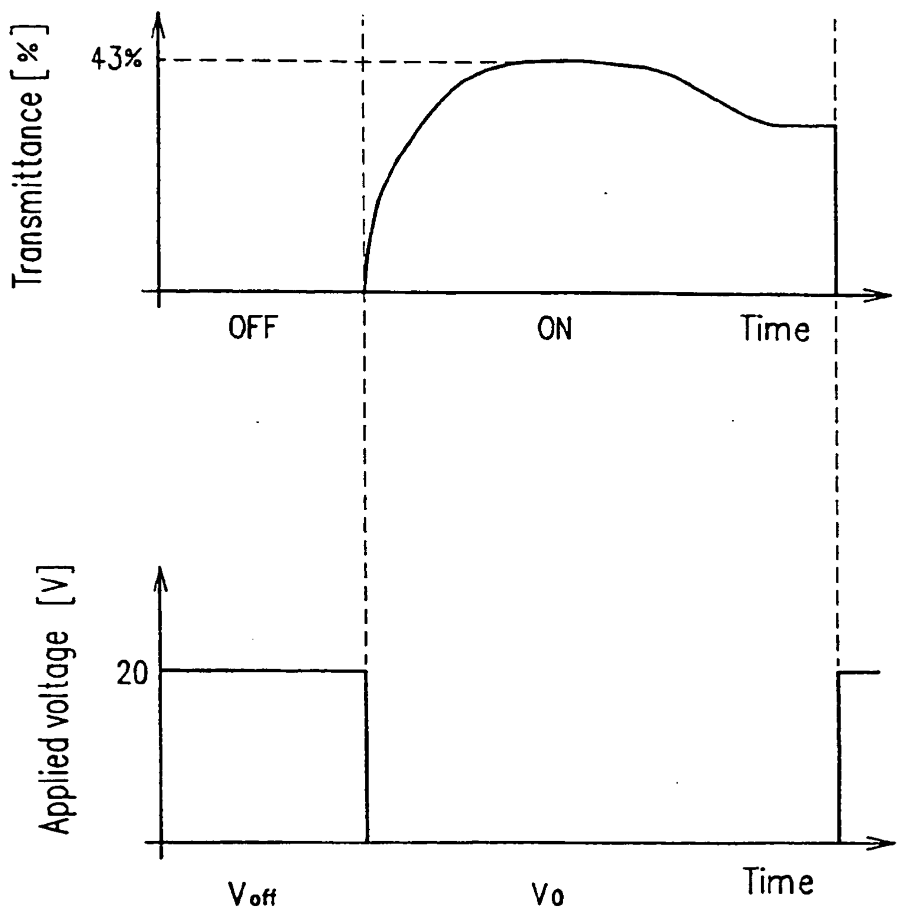


FIG. 30



Rise time 39.1 [m sec]
Decay time 35.1 [m sec]

FIG. 31


Transmittance [%]
43%
OFF
ON
Time
Applied voltage [V]
20
Voff
Vo
Time

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 660 297 A3**

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(30) Priority : **20.12.93 JP 320335/93**

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28.06.95 Bulletin 95/26

(84) Designated Contracting States :
GB NL

(88) Date of deferred publication of search report :
11.10.95 Bulletin 95/41

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MARKS & CLERK,
57/60 Lincoln's Inn Fields
London WC2A 3LS (GB)

(54) A liquid crystal device and a method for driving the same.

(57) A liquid crystal device includes : a pair of substrates ; a liquid crystal layer interposed between the pair of substrates ; at least one polarizing element ; a plurality of pixels ; a retardation ($d \times \Delta n$) of the liquid crystal layer satisfying one of a relation :

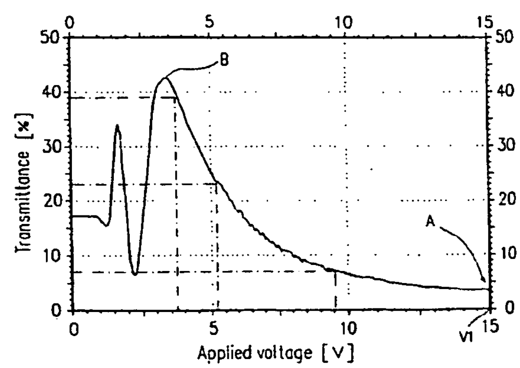
$$d \times \Delta n > \lambda/2$$

in a case where an incident light is output after passing through the liquid crystal layer once, and a relation :

$$2d \times \Delta n > \lambda/2$$

in a case where the incident light is outputted after passing through the liquid crystal layer twice, where a thickness of the liquid crystal layer is d, a birefringence is Δn and a wavelength of the light incident on the liquid crystal layer is λ ; and driving voltage supplying means for applying a driving voltage including a voltage higher than a maximum voltage providing an extremum of the output light intensity in a voltage-output light intensity characteristic of the pixels to the plurality of pixels.

FIG. 2



EP 0 660 297 A3

Jouve, 18, rue Saint-Denis, 75001 PARIS

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 30 9496

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y A	MOLECULAR CRYSTALS AND LIQUID CRYSTALS, vol. 123, no. 1/4, 1985 READING GB, pages 15-38, UCHIDA 'Application and device modeling of liquid crystal displays.' * page 26, line 10 - page 28, line 9; figures 11,12 *	1,4,6, 23,25,26 22	G09G3/36
P,Y	US-A-5 347 382 (RUMBAUGH) * column 5, line 48 - column 6, line 65; figures 3-6 *	1,4,6, 23,25,26	
A	MOLECULAR CRYSTALS AND LIQUID CRYSTALS, vol. 109, 1984 READING GB, pages 3-98, BAHADUR 'Liquid crystal displays' * page 32, line 10 - line 22 *	1,22,23	
A	SID INTERNATIONAL SYSMPOSIUM, DIGEST OF TECHNICAL PAPERS, May 1987 NEW YORK, N.Y. USA, pages 75-78, ARUGA ET AL. 'High resolution full color video projector with poly-Si TFT array light valves' * the whole document *	1,21-23	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G09G G02F
A	CONFERENCE RECORD OF 1980 BIENNIAL DISPLAY RESEARCH CONFERENCE, 21 October 1980 - 23 October 1980 NEW YORK, N.Y. USA, pages 177-179, FERGASON 'Performance of a matrix display using surface mode' * page 178, left column, line 1 - right column, line 12 *	1,3,23	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	2 August 1995	Farricella, L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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T : theory or principle underlying the invention
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EPO FORM 1503 03.82 (P04C01)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 30 9496

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	WO-A-87 01468 (CONSOLIDATED TECHNOLOGY PTY. LTD.) * page 6, line 1 - page 8, line 22; figures 1-4 * ---	1,23	
A	US-A-5 225 823 (KANALY) * column 1, line 1 - column 3, line 40 * -----	1,2,23, 24	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	2 August 1995	Farricella, L

CATEGORY OF CITED DOCUMENTS

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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

(19) Europäisches Patentamt
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MARKS & CLERK 57/60 Lincoln's Inn Fields
London WC2A 3LS (GB)

(54) Driving apparatus and method for an active matrix type liquid crystal display apparatus.

(57) A driving method is suitable for an active matrix type liquid crystal display apparatus having row and column electrodes. The driving method includes the steps of applying a gate-on pulse for writing data for one line to the column electrodes to each of the row electrodes. The gate-on pulse has a pulse waveform which includes at least one concave portion during horizontal period.

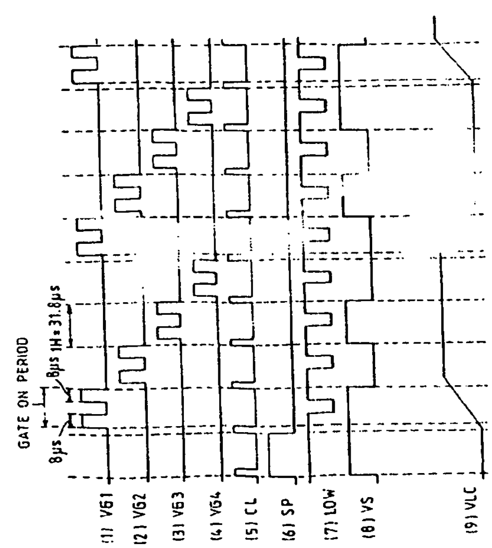

FIG.1

EP 0 539 185 A1

Jouve, 18, rue Saint-Denis, 75001 PARIS

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to a driving apparatus and method for an active matrix type liquid crystal display (LCD) apparatus having row and column electrodes in a lattice arrangement, picture element electrodes for display located in regions defined by the row and column electrodes in a matrix arrangement, and switching transistors connected to the picture element electrodes and the row and column electrodes.

2. Description of the Prior Art:

Figure 3 shows an exemplary active matrix type LCD apparatus of 4 x 4 matrix. Row electrodes (gate electrode wirings) 1-4 and column electrodes (source electrode wirings) 5 are arranged in a lattice in the row and column directions. In regions defined by the row and column electrodes, picture element electrodes 20 are arranged in a matrix. At each of the crossings of the row and column electrodes, a switching transistor 10 is provided. For the switching transistor 10, for example, a thin film transistor (TFT) is used. Gate terminals 11 of the switching transistors 10 are respectively connected to the row electrodes 1-4. Source terminals 12 of the switching transistors 10 are connected to the column electrodes 5, and drain terminals 13 thereof are connected to the corresponding picture element electrodes 20.

The column electrodes 5 are connected to a column electrode driving circuit 40. The column electrode driving circuit 40 periodically and sequentially applies data for one line to the column electrodes 5. When the switching transistors 10 are turned ON by a pulse applied from a row electrode driving circuit 30 to the row electrodes 1-4, a signal VS applied to each of the column electrodes 5 is applied to each of the picture element electrodes 20. By sequentially scanning a pulse applied from the row electrode driving circuit 30 to the row electrodes 1-4, and by varying column electrode data in synchronous with the timing, an image is displayed on the active matrix type LCD apparatus.

Figure 4 schematically shows a configuration of the row electrode driving circuit 30. The row electrode driving circuit 30 includes a shift register 31, and four AND gates 32 respectively connected to output terminals Q1, Q2, Q3, and Q4 of the shift register 31. The shift register 31 inputs data SP at a data terminal (a terminal D) and a clock pulse CL at a clock terminal (a terminal CK), and shifts the data SP in accordance with the clock pulse CL. As a result, the shift register 31 outputs the shifted data SP to the AND gates 32 at the respective output terminals Q1, Q2, Q3, and Q4. The clock pulse CL and a LOW signal are also input into the AND gates 32. The AND gates 32 AND these input signals, and output gate-on pulses VG1-VG4 onto the row electrodes 1-4, respectively.

Figure 5 shows waveforms of signals. Hereinafter, a waveform indicated by (N) in a figure is referred to as an Nth waveform. For example, in Figure 5, the first to fourth waveforms shows those of the gate-on pulses VG1-VG4, the fifth waveform shows that of the clock pulse CL, the sixth waveform shows that of the data SP, and the seventh waveform shows that of the LOW signal.

Conventionally, each of the gate-on pulses VG1-VG4 applied to the row electrodes 1-4 is a one-shot pulse, as shown by the first to fourth waveforms in Figure 5. The gate-on pulses have a waveform including an HI (high level) period and a LOW (low level) period. During the HI period, the corresponding switching transistor 10 is in an ON state, and during the LOW period, the corresponding switching transistor 10 is in an OFF state. As a result, only during the HI period of each of the gate-on pulses VG1-VG4, the signal VS shown by the eighth waveform in Figure 5 is applied to the picture element electrodes 20 connected to the respective row electrodes 1-4 through the corresponding switching transistors 10. Accordingly, electrical charges are charged in a liquid crystal layer as a display medium of picture elements. The electrical charges are held in the liquid crystal layer during the LOW period of the gate-on pulses VG1-VG4, and each of the picture elements exhibits a transmissivity depending on the voltage applied to the picture element.

According to the conventional driving method shown in Figure 5, in order to prevent the liquid crystals to deteriorate due to a DC voltage applied to an LCD apparatus, the polarity of the applied voltage is inverted for every line (for each of the row electrodes 1-4). In other words, a 1H inversion (the polarity is inverted every one horizontal period) system is adopted. The 1H period (one horizontal period) coincides with a period of a National Television System Committee (NTSC) television signal (1H = 63.5 μs).

When the gate-on pulse VG1 of the first waveform in Figure 5 is applied to the row electrode 1 in Figure 3, and the signal VS of the eighth waveform in Figure 5 is applied to the column electrode 5 in Figure 3, according to the driving method mentioned above, the potential of a picture element electrode 20 at the crossing of the row and column electrodes 1 and 5 varies. If the gate-on period is sufficiently long, the liquid crystal layer is sufficiently charged. The potential variation VLC of the picture element 20 at the crossing is saturated, as shown by the ninth waveform in Figure 5.

In order to increase the scanning speed for improving the functionality of the LCD apparatus, it is necessary to shorten the gate-on period. On the contrary, if the gate-on period is shortened, the liquid crystal layer is insufficiently charged. This results in an insufficient voltage application to the liquid crystal layer, and causes problems in displaying an image as follows.

For example, we consider the case of a transmission type LCD apparatus of a normally white system (during no voltage application : white (light is transmitted), during voltage application : black (light is shielded)). As the scanning speed is increased, the gate-on time period is not sufficient. This causes a shortage of charge phenomenon in which sufficient voltage is not applied to the liquid crystal layer. As a result, there arises problems in that the resulting display is whitish and a sufficient display contrast cannot be obtained, as compared with the case where the charge is sufficiently performed by applying a voltage of the same level to a column electrode.

The above-mentioned problems are specifically shown by a ninth waveform in Figure 6. Figure 6 shows signal waveforms in a driving method which improves the scanning speed. In this driving method, one horizontal scanning period is set to be one-half of the period of the NTSC television signal. The gate-on pulses VG1-VG4 respectively shown by first to fourth waveforms in Figure 6 are applied to the row electrodes 1-4. The gate-on pulses VG1-VG4 are produced by inputting a clock pulse CL of a fifth waveform, data SP of a sixth waveform, and a LOW signal of a seventh waveform in Figure 6 into the respective input terminals of the row electrode driving circuit 30. The signal VS shown by an eighth waveform in Figure 6 indicates a signal to be applied to the column electrodes 5 shown in Figure 3.

A ninth waveform VLC in Figure 6 represents the variation in potential applied to a picture element electrode 20 at the crossing of the row electrode 1 and the column electrode 5, when the signal VS shown by the eighth waveform in Figure 6 is applied to the column electrode 5. Since the gate-on period of the gate-on pulse of the first waveform is shorter than that of the first waveform shown in Figure 5, the charge to the liquid crystal layer is not sufficient. As a result, the potential of VLC cannot reach a sufficient level. The potential of VLC should reach the level indicated by a broken line of the ninth waveform in Figure 6. However, in actuality the potential of VLC only reaches the level indicated by the solid line thereof.

For the reasons mentioned above, there arises a problem that a display contrast sufficient for the display quality of the LCD apparatus cannot be obtained according to the driving method shown in Figure 6.

SUMMARY OF THE INVENTION

The driving apparatus and method of this invention for an active matrix type liquid crystal display apparatus having row and column electrodes includes the step of applying a gate-on pulse for writing data for one line to the column electrodes to each of the row electrodes. The gate-on pulse has a pulse waveform which includes at least one concave portion during a horizontal period.

Alternatively, the driving apparatus and method of this invention for an active matrix type liquid crystal display apparatus having row and column electrodes includes the step of applying a gate-on pulse for writing data for one line to the column electrodes to each of the row electrodes. The gate-on pulse varies between a first level and a second level at least two times during a horizontal period.

In a preferred embodiment, the horizontal period may include three periods, a first period, a second period and a third period in this order. The gate-on pulse is at the first level during the first period, at the second level during the second period and at the first level during the third period.

According to the above-mentioned driving apparatus and method of the invention, the charging efficiency to the liquid crystal layer per unit time period is improved accorded to the invention. Accordingly, the driving apparatus and method of the invention is suitable for an LCD apparatus in which the gate-on period is shortened and the scanning ability would be improved, because the liquid crystal layer is always sufficiently charged, and the display contrast can be improved.

Thus, the invention described herein makes possible the advantage of providing a driving apparatus method for an active matrix type LCD apparatus in which the charging efficiency to a liquid crystal layer per unit period time is improved, and hence the scanning ability and the display quality can be improved.

These and other advantages of the present invention will become apparent to those skilled in the art upon reading and understanding the following detailed description with reference to the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows signal waveforms illustrating a driving method for an active matrix type LCD apparatus of the invention;

Figure 2 is a graph comparatively showing a transmissivity curve of a liquid crystal panel in the method of the invention and a transmissivity curve in a prior art method;

Figure 3 shows a schematic configuration of the active matrix type LCD apparatus;

Figure 4 shows a schematic configuration of a row electrode driving circuit;

Figure 5 shows signal waveforms showing the prior art driving method;

Figure 6 shows signal waveforms showing a prior art driving method in which a gate-on period is shortened.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows a driving method for an active matrix type LCD apparatus of the invention. The configuration of the active matrix type LCD apparatus to which the method of the invention is applied is the same as that of the active matrix type LCD apparatus shown in Figure 3. A row electrode driving circuit has the same configuration as that of the row electrode driving circuit shown in Figure 4. The detailed description of the configuration is omitted and like components have like reference numerals.

In Figure 1, first to fourth waveforms represent gate-on pulses VG1-VG4 respectively output from the row electrode driving circuit 30 onto the row electrodes 1-4. In these gate-on pulses VG1-VG4, one horizontal scanning period (1H) coincides with one-half of the period of the NTSC television signal (1H = about 31.8 μs). That is, the length of one horizontal scanning period is the same as that used in the prior art method of Figure 6.

These gate-on pulses VG1-VG4 are produced by inputting a clock pulse CL of a fifth waveform, data SP of a sixth waveform, and a LOW signal of a seventh waveform into the respective input terminals of the row electrode driving circuit 30, as in the prior art method. The gate-on period of each of the gate-on pulses VG1-VG4 is 24 μs which is the same as in the prior art method. However, each of the gate-on pulses VG1-VG4 has a pulse waveform including a concave portion during the gate-on period. Specifically, each of the pulses are set to be a LOW level during one-third of the gate-on period (i.e., the intermediate 8 μs period), as shown in Figure 1. Accordingly, each of the gate-on pulses VG1-VG4 has a pulse waveform including two HI periods and one LOW period (8 μs) therebetween. The length of one of the HI periods is obtained by subtracting the intermediate period from the gate-on period, and by dividing the subtracted result into two equal periods, i.e., (24 - 8) / 2 = 8 μs.

The gate-on pulses VG1-VG4 having such pulse waveforms may be produced by superimposing the LOW signal of the seventh waveform on the gate-on pulses VG1-VG4 produced by the use of the prior art method. As shown by the seventh waveform, the polarity of the LOW signal is inverted in the intermediate period of the gate-on period.

As shown by an eighth waveform in Figure 1, the waveform of a signal VS to be applied to each of the column electrodes 5 shown in Figure 3 is the same as that of the prior art method shown in Figure 6.

When the signal VS of the same level is applied to the same column electrode 5 both in the method of the invention and in the prior art method of Figure 6, the charging efficiency to a liquid crystal layer in the method of the invention can be improved as compared with the prior art method for the following reasons with reference to the graph shown in Figure 2. In Figure 2, the vertical axis represents a transmissivity of a liquid crystal panel (%) and the horizontal axis represents an amplitude V of the signal VS applied to a column electrode (arbitrary unit). In Figure 2, a transmissivity in the method of the invention is shown by a curve ①, and a transmissivity in the prior art method is also shown by a curve ② for comparison. The transmissivity is measured by using a transmission type LCD apparatus of a normally white system.

Since the transmissivity is measured by using an LCD apparatus of a normally white system as described above, it is decreased as the level of the signal VS is increased. As seen from the curves ① and ② at the point indicated by A in Figure 2, the transmissivity in the method of the invention is lower than that in the prior art method.

In the case of the LCD of a normally white system, the lower transmissivity at the same level of the voltage applied to a column electrode means that the level of a voltage applied to the liquid crystal layer is increased. That is, the charging efficiency to the liquid crystal layer is superior. More specifically, as seen from Figure 2, the charging efficiency to the liquid crystal layer can be improved in the method of the invention, as compared with the prior art method. Accordingly, it is clear by comparing the ninth waveform in Figure 1 with the ninth waveform in Figure 6 that insufficient charge does not occur when the invention is applied to an LCD apparatus in which the scanning is performed with a shortened gate-on period.

In the above embodiment, the gate-on pulse has a pulse waveform including a concave portion in a horizontal period. Alternatively, the gate-on pulse may have a pulse waveform which is divided into a plurality of portions and includes at least one concave portion during a horizontal period.

As described above, according to the driving method for an active matrix type LCD apparatus of the invention, the charging efficiency to a liquid crystal layer per unit time period can be improved as compared with the prior art method. Accordingly, the driving method of the invention is suitable for an LCD apparatus in which the gate-on period is shortened and the scanning ability is attempted to be improved, because the liquid crystal layer is always sufficiently charged and hence the display contrast can be improved.

Various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope and spirit of this invention. Accordingly, it is not intended that the scope of the claims appended hereto be limited to the description as set forth herein, but rather that the claims be broadly construed.

Claims

1. A driving method for an active matrix type liquid crystal display apparatus having row and column electrodes, said driving method comprising the step of:
applying a gate-on pulse for writing data for one line to said column electrodes to each of said row electrodes, said gate-on pulse having a pulse waveform which includes at least one concave portion during a horizontal period.

2. A driving method for an active matrix type liquid crystal display apparatus having row and column electrodes, said driving method comprising the step of:
applying a gate-on pulse for writing data for one line to said column electrodes to each of said row electrodes, said gate-on pulse varying between a first level and a second level at least two times during a horizontal period.

3. The method according to claim 2, wherein said horizontal period includes three periods, a first period, a second period and a third period in this order, said gate-on pulse being at said first level during said first period, at said second level during said second period and at said first level during said third period.

4. A driving apparatus for an active matrix type liquid crystal display having row and column electrodes, said driving apparatus comprising:
means for applying a gate-on-pulse for writing data for one line to said column electrodes to each of said row electrodes, said gate-on pulse having a pulse waveform which includes at least one concave portion during a horizontal period.

5. A driving apparatus for an active matrix type liquid crystal display having row and column electrodes, said driving apparatus comprising:
means for applying a gate-on-pulse for writing data for one line to said column electrodes to each of said row electrodes, said gate-on pulse varying between a first level and a second level at least two times during a horizontal period.

6. The apparatus according to claim 5, wherein said horizontal period includes three periods, a first period, a second period and a third period in this order, said gate-on pulse being at said first level during said first period, at said second level during said second period and at said first level during said third period.

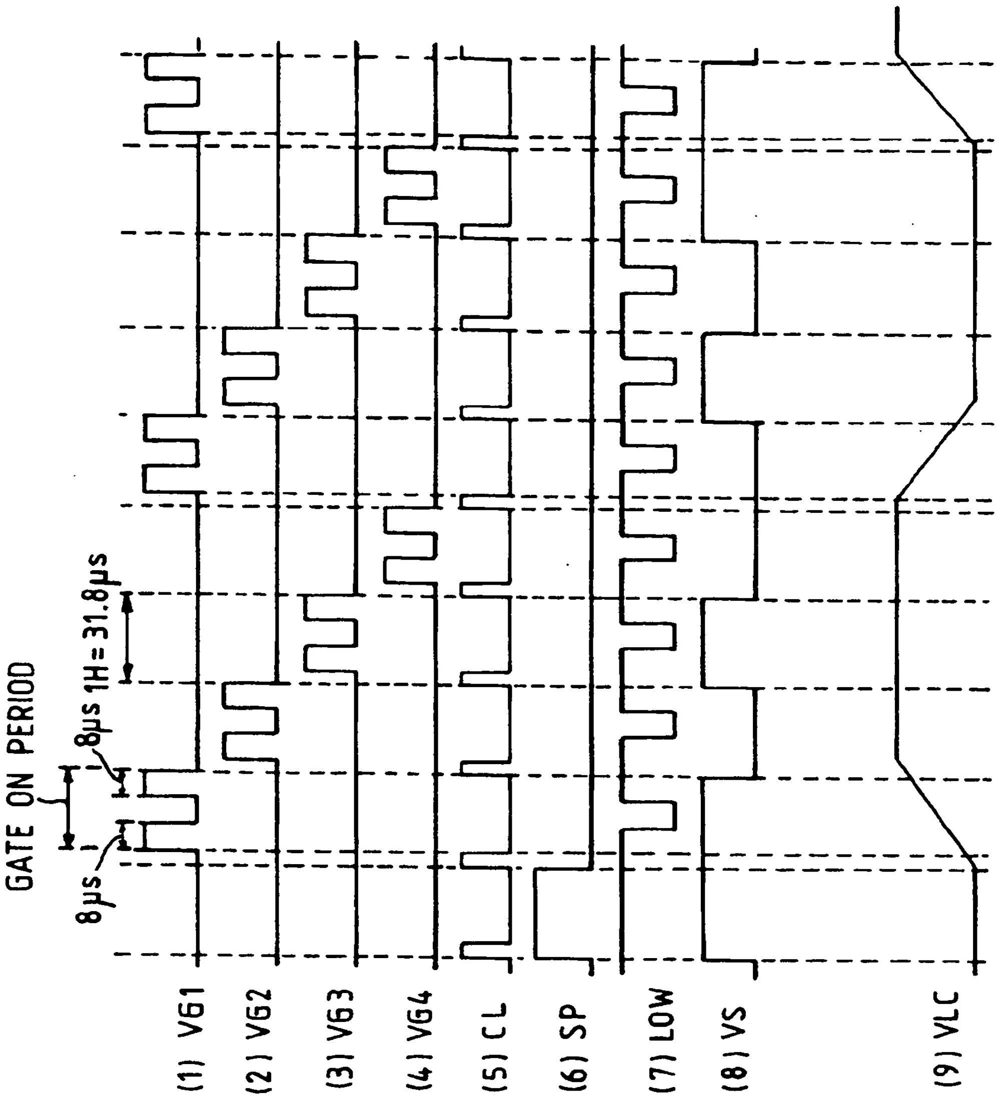
GATE ON PERIOD
8μs
8μs
1H = 31.8μs
(1) VG1
(2) VG2
(3) VG3
(4) VG4
(5) CL
(6) SP
(7) LOW
(8) VS
(9) VLC

FIG.1

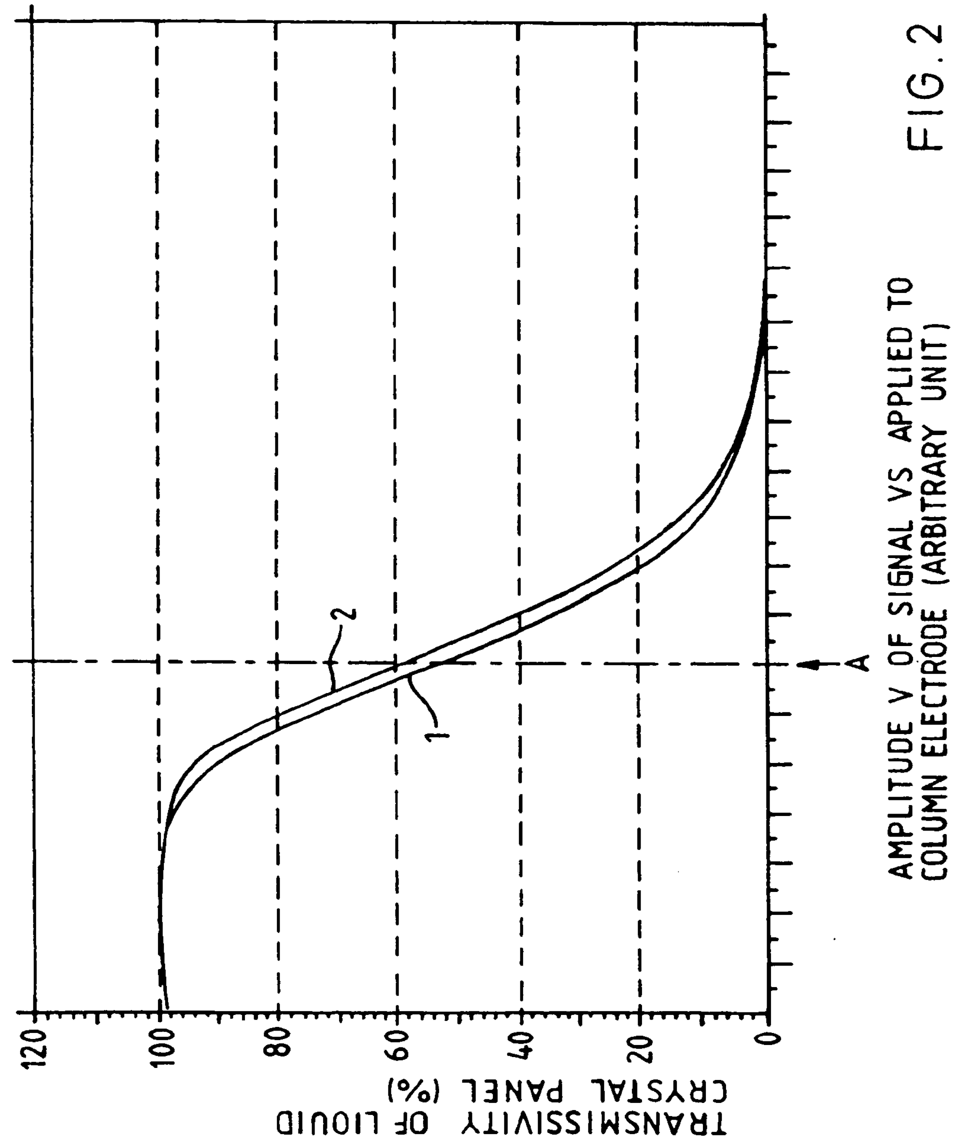
TRANSMISSIVITY OF LIQUID CRYSTAL PANEL (%)
120
100
80
60
40
20
0
AMPLITUDE V OF SIGNAL VS APPLIED TO COLUMN ELECTRODE (ARBITRARY UNIT)
A
1
2

FIG. 2

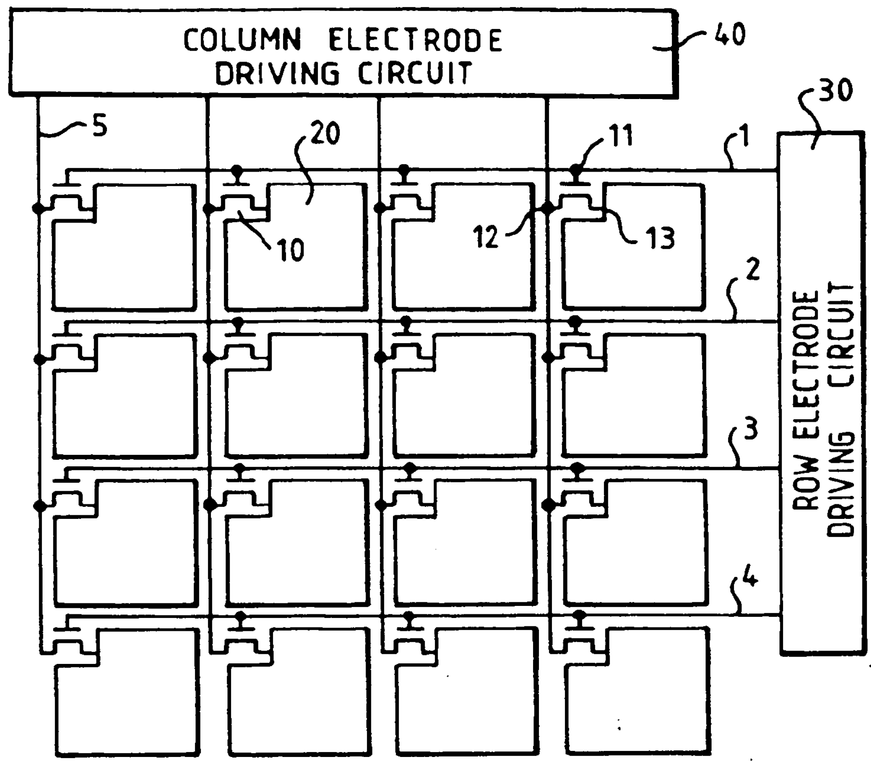
COLUMN ELECTRODE
DRIVING CIRCUIT
40
30
5
20
11
1
10
12
13
2
3
4
ROW ELECTRODE
DRIVING CIRCUIT

FIG.3

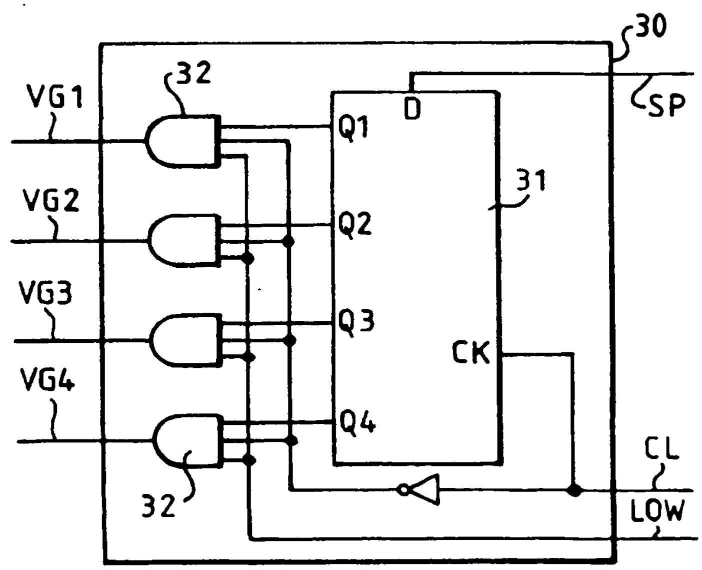
30
32
D
SP
VG1
Q1
31
VG2
Q2
VG3
Q3
CK
VG4
Q4
CL
32
LOW

FIG.4

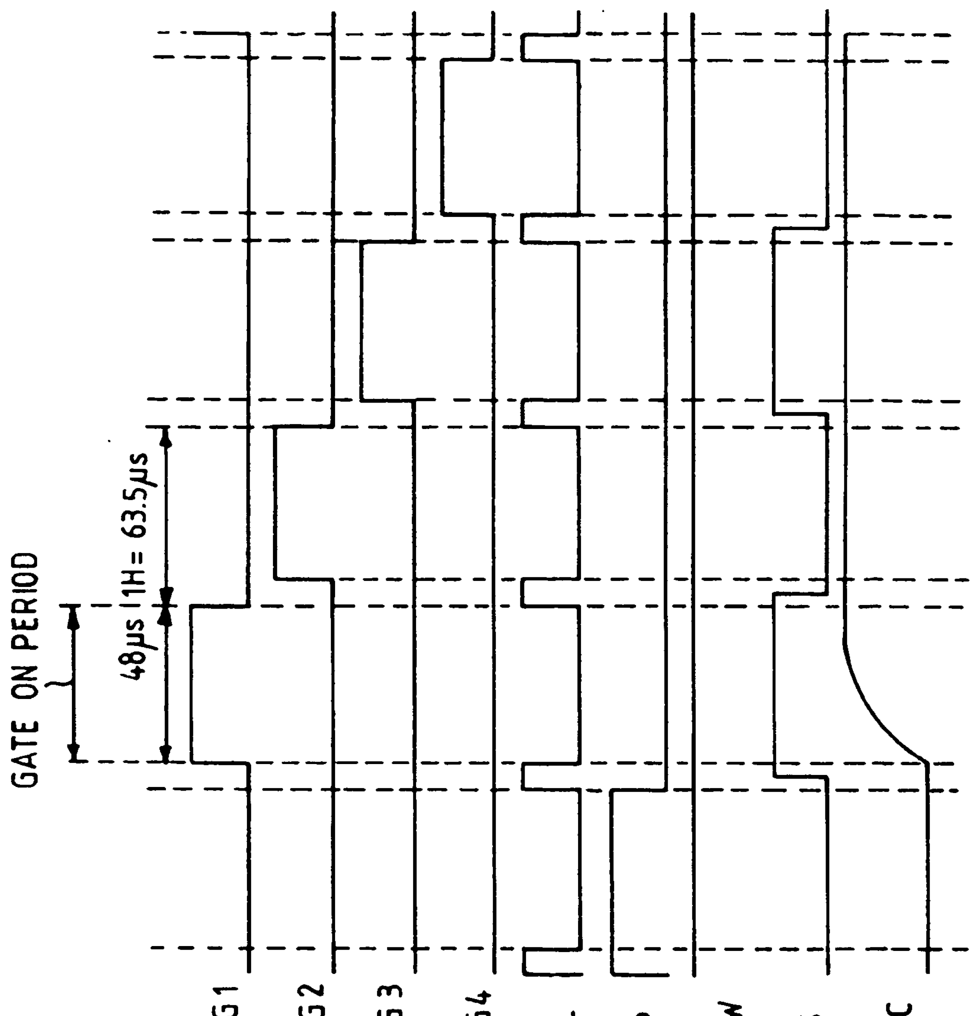
GATE ON PERIOD
48μs
1H = 63.5μs
(1) VG1
(2) VG2
(3) VG3
(4) VG4
(5) CL
(6) SP
(7) LOW
(8) VS
(9) VLC

FIG. 5

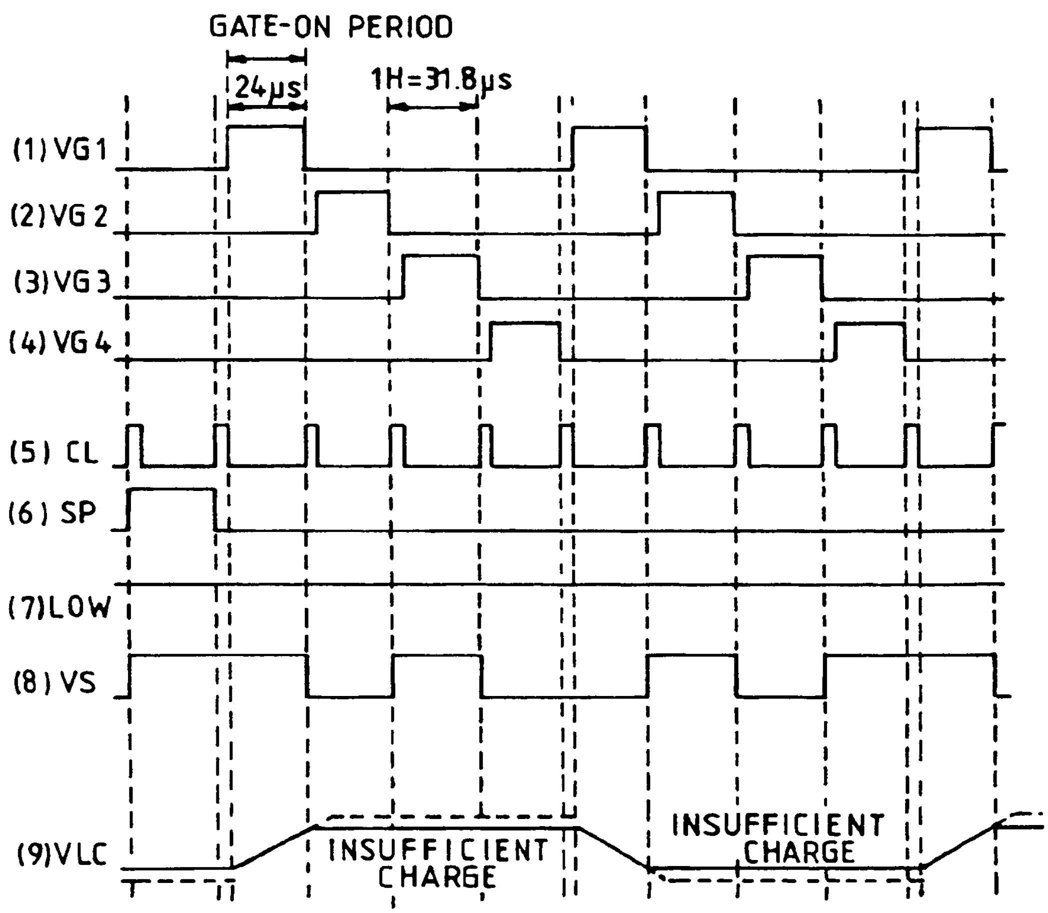
GATE-ON PERIOD
24μs
1H=31.8μs
(1) VG1
(2) VG2
(3) VG3
(4) VG4
(5) CL
(6) SP
(7) LOW
(8) VS
(9) VLC
INSUFFICIENT CHARGE
INSUFFICIENT CHARGE

FIG.6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 92 30 9629

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	EP-A-0 373 565 (MATSUSHITA) * column 10, line 12 - line 55; figures 8,10 * * column 13, line 43 - column 14, line 12; figure 14B *	1,2,4,5	G09G3/36
X	EP-A-0 079 496 (HITACHI) * page 9, line 5 - page 11, line 20; figures 5,8 *	1,2,4,5	
X	IBM TECHNICAL DISCLOSURE BULLETIN. vol. 33, no. 9, February 1991, NEW YORK US pages 309 - 310 'Gate drive scheme for thin film transistor/liquid crystal displays' * the whole document *	1,4	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G09G
G02F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	21 JANUARY 1993	SAAM C.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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PTO/SB/21 (08-03)
Approved for use through 08/30/2003. OMB 0651-0031
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/707,741
Filing Date	01/08/2004
First Named Inventor	Yung-Hung Shen
Art Unit	
Examiner Name	
Attorney Docket Number	VASP0001USA
Total Number of Pages in This Submission	3

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [x] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
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- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) ____________
- [ ] After Allowance communication to Technology Center (TC)
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
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- [ ] Status Letter
- [ ] Other Enclosure(s) (please Identify below):

Remarks

Response to the office action has been sent to the examiner by fax on 12/04/2003

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Date	3/12/2004

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Signature		Date	

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Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 0.00

Complete if Known	
Application Number	10/707,741
Filing Date	01/08/2004
First Named Inventor	Yung-Hung Shen
Examiner Name	
Art Unit	
Attorney Docket No.	VASP0001USA

METHOD OF PAYMENT *(check all that apply)*

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1. BASIC FILING FEE

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1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		x		=
Independent Claims		- 3** =		x		=
Multiple Dependent						=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) ____________

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 0.00

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	Winston Hsu	*Registration No. (Attorney/Agent)*	41,526	*Telephone*	886289237350
Signature	Winston Hsu			*Date*	3/12/2004

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DECLARATION — Supplemental Priority Data Sheet

Additional foreign applications:

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
092132122	Taiwan R.O.C	11/17/2003	☐	☑	☐
			☐	☐	☐
			☐	☐	☐
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			☐	☐	☐

VAS-001-TWN

中華民國經濟部智慧財產局

INTELLECTUAL PROPERTY OFFICE
MINISTRY OF ECONOMIC AFFAIRS
REPUBLIC OF CHINA

茲證明所附文件，係本局存檔中原申請案的副本，正確無訛，
其申請資料如下 ：

This is to certify that annexed is a true copy from the records of this office of the application as originally filed which is identified hereunder：

申　請　日 ： 西元 2003 年 11 月 17 日
Application Date

申 請 案 號 ： 092132122
Application No.

申　請　人 ： 鈺瀚科技股份有限公司
Applicant(s)

局　　長
Director General

蔡練生

發文日期： 西元 2004 年 1 月 5 日
Issue Date

發文字號： 09320010010
Serial No.

LGD_000269

申請日期：	IPC分類
申請案號：	

(以上各欄由本局填註)

發明專利說明書

一、發明名稱	中文	用來驅動一液晶顯示面板之驅動電路及其驅動方法
	英文	DRIVING CIRCUIT AND DRIVING METHOD THEREOF FOR A LIQUID CRYSTAL DISPLAY
二、發明人(共4人)	姓名(中文)	1. 申雲洪 2. 王世忠
	姓名(英文)	1. SHEN, YUNG-HUNG 2. WANG, SHIH-CHUNG
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	名稱或姓名(英文)	1. VASTVIEW TECHNOLOGY INC.
	國籍(中英文)	1. 中華民國 TW
	住居所(營業所)(中文)	1. 新竹科學工業園區新安路八號三樓 (本地址與前向貴局申請者相同)
	住居所(營業所)(英文)	1. 3F, No. 8, Hsin-Ann Rd., Science-Based Industrial Park, Hsinchu 300, Taiwan, R.O.C.
	代表人(中文)	1. 梁育正
	代表人(英文)	1. LIANG, YU-CHENG

申請日期：	IPC分類
申請案號：	

（以上各欄由本局填註）

發明專利說明書

<table>
<tr><td rowspan="2">一、發明名稱</td><td>中 文</td><td></td></tr>
<tr><td>英 文</td><td></td></tr>
<tr><td rowspan="6">二、發明人（共4人）</td><td>姓 名（中文）</td><td>3. 沈毓仁</td></tr>
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<tr><td>名稱或姓 名（英文）</td><td></td></tr>
<tr><td>國 籍（中英文）</td><td></td></tr>
<tr><td>住居所（營業所）（中 文）</td><td></td></tr>
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<tr><td>代表人（中文）</td><td></td></tr>
<tr><td>代表人（英文）</td><td></td></tr>
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申請日期：	IPC分類
申請案號：	

(以上各欄由本局填註)

發明專利說明書

一、發明名稱	中 文	
	英 文	
二、發明人(共4人)	姓 名(中文)	4.陳政嶸
	姓 名(英文)	4.CHEN, CHENG-JUNG
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	住居所(營業所)(中 文)	
	住居所(營業所)(英 文)	
	代表人(中文)	
	代表人(英文)	

四、中文發明摘要　（發明名稱：用來驅動一液晶顯示面板之驅動電路及其驅動方法）

本發明係揭露一種驅動一液晶顯示面板的電路及其方法，該液晶顯示面板包含有：複數條掃瞄線、複數條資料線以及複數個像素。每一像素連接於一對應的掃瞄線以及一對應的資料線，且每一像素包含有一開關元件及一液晶元件，該開關元件連接於該對應的掃瞄線、該對應的資料線以及該液晶元件。該方法包含：連續地接收複數筆圖框資料；每間隔一圖框週期（frame period），依據該等圖框資料，針對每一像素產生複數個資料電壓脈波；以及於一個圖框週期內，將所產生的該等資料電壓脈波藉由該像素所連接之該資料線施加于該像素之液晶元件，以控制該液晶元件之光線穿透率的變化。

五、英文發明摘要　（發明名稱：DRIVING CIRCUIT AND DRIVING METHOD THEREOF FOR A LIQUID CRYSTAL DISPLAY)

The present invention discloses an apparatus and method thereof for driving a liquid crystal display (LCD) panel. The LCD panel has a plurality of scan lines, a plurality of data lines, and a plurality of pixels. Each of the pixels is connected to a corresponding scan line and a corresponding data line. Each of the pixels has a liquid crystal element and a switch element

四、中文發明摘要　（發明名稱：用來驅動一液晶顯示面板之驅動電路及其驅動方法）

五、英文發明摘要　（發明名稱：DRIVING CIRCUIT AND DRIVING METHOD THEREOF FOR A LIQUID CRYSTAL DISPLAY）

connected to the corresponding scan line, the corresponding data line, and the liquid crystal element. The method has: sequentially receiving a plurality of pieces of frame data; generating a plurality data impulses for each pixel every frame period according to the pieces of the frame data; and applying the data impulses to the data line connected to the liquid crystal element of

四、中文發明摘要　（發明名稱：用來驅動一液晶顯示面板之驅動電路及其驅動方法）

五、英文發明摘要　（發明名稱：DRIVING CIRCUIT AND DRIVING METHOD THEREOF FOR A LIQUID CRYSTAL DISPLAY）

the pixel within one frame period so as to control a transmission rate of liquid crystal element.

六、指定代表圖

(一)、 本 案 代 表 圖 為 :第 ___五 _____圖

(二)、 本 案 代 表 圖 之 元 件 代 表 符 號 簡 單 說 明 :

GN~ GN+3(2) 像 素 資 料

一、本案已向

國家(地區)申請專利　　申請日期　　案號　　主張專利法第二十四條第一項優先權

無

二、☐主張專利法第二十五條之一第一項優先權:

申請案號:

無

日期:

三、主張本案係符合專利法第二十條第一項☐第一款但書或☐第二款但書規定之期間

日期:

四、☐有關微生物已寄存於國外:

寄存國家:

寄存機構:

無

寄存日期:

寄存號碼:

☐有關微生物已寄存於國內(本局所指定之寄存機構):

寄存機構:

寄存日期:

無

寄存號碼:

☐熟習該項技術者易於獲得,不須寄存。

【技術領域】

本發明係有關於一種液晶顯示器之驅動電路及其驅動方法，尤指一種於一圖框週期施加兩個以上之資料電壓脈波於像素電極之驅動電路及其驅動方法。

【先前技術】

一般而言，液晶顯示器具有重量輕、功率消耗少以及低輻射等等的優點，因此，液晶顯示器已廣泛地應用於市面上多種可攜式資訊產品，例如筆記型電腦(notebook)以及個人數位助理(personal digital assistant, PDA)等商品。此外，液晶螢幕以及液晶電視亦已逐漸普及，取代傳統使用的陰極射線管(cathode ray tube, CRT)顯示器和電視。但是液晶顯示器亦有其缺點。因為液晶分子特性的限制，在影像資料切換的時候，必須扭轉液晶分子改變其排列方向，所以會出現畫面延遲的情形。為了因應多媒體影像的快速切換，提昇液晶反應速度的要求也愈趨重要。

一般來講，當驅動電路驅動驅動液晶顯示器時，驅動電路會連續地接收複數筆圖框(frame)資料，之後再依據該等圖框資料來產生相關的資料電壓脈波、掃瞄線電壓、時序信號等，以控制液晶顯示器之像素的操作。其

中上述的每一個圖框資料係包含液晶顯示器於一圖框週期(frame period)內，用來重整(refresh)其所有像素時的資料，因此每一圖框資料即可視為包含有複數筆像素資料，而每一像素資料即是用來定義某一個像素於一個圖框週期內所須達到的灰階狀態，而以目前一般所採用電腦之液晶顯示器標準來說，每一像素可於256(等於2^8)種灰階狀態間切換，因此每一像素資料的資料長度等於8位元。

請參考圖一，圖一為習知液晶顯示器中像素資料值對應於圖框之時序圖。當驅動一像素時，驅動電路會依序地接收用來驅動該像素的複數筆像素資料，如圖一所示，GN、GN+1、GN+2即表示了驅動電路於各圖框週期N、N+1、N+2內所接收到的像素資料，而驅動電路會依據像素資料GN、GN+1、GN+2所記錄的像素資料值來驅動某一像素分別於圖框週期N、N+1、N+2的灰階狀態。一般來講，像素資料所記錄的值越大，則代表經驅動電路驅動後的像素其灰階值越大，而驅動電路會依據像素資料GN、GN+1、GN+2，於相對應的圖框週期內產生一資料電壓脈波，並將所產生的資料電壓脈波施加於該對應像素的像素電極(pixel electrode)，以使所驅動的像素於各圖框週期內處於對應的灰階狀態下。

請參考圖二，圖二為習知像素之穿透率對應於圖框之時

序圖。圖二中，標示了兩條曲線C1及C2，而兩曲線C1及C2皆是在驅動電路欲將某一像素於圖框週期N之期間，將其光線穿透率由穿透率T1驅換成穿透率T2時所量測而得，其中曲線C1表示未經過激(over drive)驅動時所量測得的像素於各圖框週期內的光線穿透率，而曲線C2則表示經習知的過激驅動方式驅動時所量測得的像素於各圖框週期內的光線穿透率。關於習知的過激驅動方法，可參考美國早期公開專利申請案US 2002/0050965等文獻資料，在此即簡單地說明如下。因為像素的液晶分子的特性，在其充電時會有一個延遲時間，使得其液晶分子無法在一個圖框週期內偏轉到達預定的角度以達到預定的光線穿透率。如曲線C1所示，在未經過激的情況下，光線穿透率無法在圖框N的圖框週期中到達預定的穿透率，而必須等到圖框N+2的圖框週期才會到達預定的穿透率，然而這樣的延遲卻會使液晶顯示器出現殘影的現象。為了改善此一現象，一些習知的液晶顯示器即採用過激驅動方法，其係將比原先更高或更低的資料電壓脈波施加於像素的像素電極，以加快其液晶分子的反應速度，進而使得像素可在預定的圖框週期內達到預定的灰階狀態。如曲線C2所示，在經過激的情況下，液晶分子的反應速度雖然較未經過激驅動時的快，其光線穿透率在圖框週期N+1內即達到預定的穿透率T2，但仍比預定穿透率須在圖框週期N即須達到預定的穿透率T2的理想狀態慢了許多。

【內容】

因此本發明之主要目的在於提供一種液晶顯示器之驅動電路及其驅動方法，以解決上述習知的問題。

根據本發明之申請專利範圍，係揭露一種液晶顯示器之驅動電路及其驅動方法。該液晶顯示面板包含有複數條掃瞄線、複數條資料線，以及複數個像素。其中每一像素連接於一對應的掃瞄線以及一對應的資料線，且每一像素包含有一開關元件以及一液晶元件。該開關元件連接於該對應的掃瞄線、該對應的資料線以及該液晶元件。該方法包含：連續地接收複數筆圖框資料；每間隔一圖框週期（frame period），依據該等圖框資料，針對每一像素產生複數個電壓脈波；以及於一個圖框週期內，將所產生的該等電壓脈波藉由該像素所連接之該資料線施加于該像素之液晶元件，以控制該液晶元件之光線穿透率的變化。

此外，本發明之驅動電路包含有一殘影消除器、一源極驅動器，以及一閘極驅動器。該殘影消除器用來每間隔一圖框週期接收一圖框資料，而每一圖框資料包含有複數筆像素資料，每一筆像素資料皆對應於一像素。該殘影消除器會延遲一當時圖框資料，以產生一延遲圖框資

料，並依據該當時圖框資料以及該延遲圖框資料，於每一圖框週期內為每一像素產生複數筆過激像素資料。該源極驅動器用來於每一圖框資料內根據該殘影消除器對每一像素所產生複數筆過激像素資料，對每一像素產生複數個電壓脈波，並將該等電壓脈波藉由該像素所連接之該資料線施加于該像素之液晶元件，以控制該液晶元件之光線穿透率的變化。該閘極驅動器則是用來施加一掃瞄線電壓于該等像素之開關元件，以使該等電壓脈波可被施于該像素之液晶元件。

【實施方法】

請參考圖三，圖三為本發明驅動電路 10與一液晶面板 30之功能方塊圖。驅動電路 10係用來驅動液晶面板 30，其包含有一訊號控制器 12、一殘影消除器 14、一時序控制器 16、一源極驅動器 18以及一閘極驅動器 20。訊號控制器 12係用來接收一複合式影像訊號 Sc，此複合式影像訊號 Sc包含有用來驅動液晶面板 30時所需的各圖框資料以及時序資料等，而訊號控制器 12會處理所接收到的複合式影像訊號 Sc，以將複合式影像訊號 Sc區分為一圖框訊號 G以及一控制訊號 C。之後，殘影消除器 14會持續地接收圖框訊號 G所包含複數筆圖框資料以及控制訊號 C，並依據圖框訊號 G所包含複數筆圖框資料來產生一處理後的

圖框訊號G'，而其中圖框訊號G'包含有複數筆過激像素資料，其更詳細的作用後面的說明中將會提及。時序控制器16會依據所接收到的圖框訊號G'以及控制訊號C來控制源極驅動器18與閘極驅動器20的操作，以使源極驅動器18與閘極驅動器20依據圖框訊號G'所包含的複數筆過激像素資料來產生對應的資料線電壓與掃瞄線電壓，以驅動液晶面板30產生對應於複合式影像訊號Sc之影像。

請參考圖四，圖四為圖三中液晶面板30之電路圖。液晶面板31包含有複數條掃瞄線32、複數條資料線34以及複數個像素36。每一像素36連接於一對應的掃瞄線32以及一對應的資料線34，且每一像素36包含有一開關元件38以及一液晶元件39，而一般液晶元件39會被稱作一像素電極(pixel electrode)。另外，開關元件38連接於該對應的掃瞄線32及該對應的資料線34，源極驅動器18與閘極驅動器20會藉由掃瞄線32及資料線34來控制每一像素36的操作。一般驅動液晶顯示器30的方法係施加一掃描電壓於該掃描線32以開啟開關元件38，然後再藉由該資料線34將一資料電壓脈波經由開關元件38寫入像素電極39。因此，當掃描電壓被施加於掃描線32上而使開關元件38開啟時，資料線34上的資料電壓脈波會經由開關元件38對像素電極39進行充電，而使其液晶分子偏轉；而當掃描線上的掃描電壓被移除而使得開關元件38關閉時，資料線34與畫素36的電連結會被切斷，像素電極39

則保持其被充電的狀態。掃描線32會控制開關元件38重複地開關，使得像素電極39可重複地被資料線34充電。掃描線32上不同的資料線電壓會使畫素36的液晶分子產生不同角度的偏轉，而使畫素36呈現出不同的透光率，而如此一來，液晶顯示器30即可呈現出不同的顯示畫面。

請參考圖五，圖五為依據本發明方法所產生的像素資料其值對應於圖框之時序圖。依據本發明之方法，當驅動液晶面板30的任一像素36時，驅動電路10會依序地產生用來驅動該像素的複數筆像素資料，如圖一所示，GN、GN(2)、GN+1、GN+1(2)、GN+2、GN+2(2)、GN+3、GN+3(2)即表示了驅動電路於各圖框週期N、N+1、N+2、N+3內所產生的像素資料，且驅動電路10於每一圖框週期內對每一像素36皆會產生兩筆像素資料，而此特徵即是本發明與習知技術之間最大的不同點。驅動電路10會依據像素資料GN～GN+2(2)所記錄的像素資料值來驅動某一像素分別於圖框週期N、N+1、N+2的灰階狀態。舉例來說，當像素資料GN、GN(2)產生後，驅動電路10的源極驅動器18即會將像素資料GN、GN(2)轉換成對應的兩資料電壓脈波，再將所產生的兩資料電壓脈波於圖框週期N內，藉由資料線32施加到像素36的液晶元件39，已控制液晶元件39之光線穿透率。同理，相對應於像素資料GN+1～GN+3(2)的資料電壓脈波，會每間隔半個圖框週期，分別被施

加在對應的像素電極39上。同樣的，在本實施例中，像素資料所記錄的值越大，則其對應的資料電壓脈波的電壓值會越高，且代表經驅動電路10驅動後的像素36其灰階值越大。

請參考圖六，圖六為採用本發明之方法後其像素36之穿透率對應於圖框之時序圖。如前所述，驅動電路10會於每一圖框週期內產生兩筆像素資料，之後源極驅動器18會依據此兩筆像素資料產生兩相對應的資料電壓脈波，並於一個圖框週期內將所產生的兩資料電壓脈波施加於對應的像素36之像素電極39，以控制該像素電極39之光線穿透率及其灰階狀態。如圖六所示，驅動電路10在圖框週期N+1期間將某一像素36之像素電極39的光線穿透率由T1驅換到T2時，該像素電極39會於圖框週期N+1的期間，被施予兩相對應於像素資料GN+1、GN+1(2)的資料電壓脈波，其中兩資料電壓脈波所施加的時間點間隔半個圖框週期。如圖六所示，雖然在圖框週期N+1的前半個週期n+2內，像素電極39的光線穿透率無法達到預期的T2，但因為在圖框週期N+1的後半個週期n+3內，像素電極39還會被再施予另一資料電壓脈波，故其光線穿透率可如預期般地，在一個圖框週期N+1內成功地由T1切換到T2。因此，利用本發明之方法所驅動的液晶面板，並不會產生殘影的現象。

本實施例中，在每一圖框週期的期間內，為每一像素產生兩筆像素資料的工作係由殘影消除器14來負責完成。請參考圖七，圖七為圖三殘影消除器14之功能方塊圖。殘影消除器14包含有一倍頻器40、一處理電路42、一第一影像記憶體44、一第二影像記憶體46、一第一記憶體控制器48，以及一第二記憶體控制器50。其中，倍頻器40用來將控制訊號C之頻率倍頻，以產生一倍頻訊號C2。第一影像記憶體44會受到第一記憶體控制器48之控制，而依據控制訊號C來延遲一當時的像素資料Gm一圖框週期，以產生一延遲的像素資料Gm-1。處理電路42會依據當時的像素資料Gm以及第一影像記憶體44所延遲的像素資料Gm-1，來產生複數筆過激驅動像素資料GN。第二影像記憶體46會儲存過激驅動像素資料GN，而第二記憶體控制器50會依據倍頻訊號C2來控制第二影像記憶體46於每一圖框週期內，對任一像素36輸出兩筆過激驅動像素資料GN、GN(2)，以使源極驅動器18根據第二影像記憶體46所輸出的兩筆過激像素資料GN、GN(2)，於每一圖框週期內對一特定的像素36施加兩資料電壓脈波。

請參考圖八，圖八為本發明第二實施例中一殘影消除器60之功能方塊圖。殘影消除器60的功能與殘影消除器14的作用相同，皆用來於每一圖框週期內，為每一像素36產生兩筆像素資料。殘影消除器60包含有一倍頻器62、一第一影像記憶體66、一第二影像記憶體68、一第三影

像記憶體70、一記憶體控制器64、一處理電路74，以及一比較電路72。其中倍頻器62用來將一控制訊號C之頻率倍頻，以產生一倍頻訊號C2，而第一影像記憶體66用來接收以及暫存複數筆像素資料G。第二影像記憶體68會將第一影像記憶體66所輸出的像素資料G延遲一圖框週期後輸出為像素資料Gm-1，而第三影像記憶體70會將第二影像記憶體68所輸出的像素資料Gm-1延遲一圖框週期後輸出為像素資料Gm-2，所以像素資料Gm-2在時脈上落後像素資料Gm-1一個圖框週期，而像素資料Gm-1在時脈上也落後像素資料Gm一個圖框週期。記憶體控制器64會依據倍頻訊號C2，來控制第二影像記憶體68以及第三影像記憶體70的操作，以使第二影像記憶體68與第三影像記憶體70於每一圖框週期內分別輸出兩筆像素資料。處理電路74則用來依據經第二影像記憶體68以及第三影像記憶體70延遲後所輸出的像素資料Gm-1、Gm-2，於每一圖框週期內，為每一像素36產生兩筆過激驅動像素資料GN-1、GN-1(2)。此外，比較電路72則是用來比較第二影像記憶體68所輸出的像素資料Gm-1以及第三影像記憶體70所輸出的等像素資料Gm-2，以決定處理電路74所產生的過激驅動像素資料GN-1、GN-1(2)之資料值，而關於過激驅動像素資料GN-1、GN-1(2)之資料值的決定方式，將於下面說明。

請參考圖九及圖十，圖九為圖八殘影消除器60所接收到

的原始像素資料對應於圖框之時序圖，圖十為圖八殘影消除器 60所輸出的過激像素資料對應於圖框之時序圖。如圖九所示，殘影消除器 60於圖框週期 N與 N+1內所接收到的原始像素資料分別為 Gm以及 Gm+1，其中兩原始像素資料 Gm與 Gm+1之間的差異值為 Diff。殘影消除器 60會依據兩原始像素資料 Gm與 Gm+1來產生對應於圖框週期 N+1的兩筆過激像素資料 GN+1以及 GN+1(2)，而其中兩筆過激像素資料 GN+1以及 GN+1(2) 之間的差異值為△ G，且須特別說明的是差異值△ G係由圖八中的比較電路 72所決定，以使驅動電路 10得以因應不同的狀況來對各像素 36，做出適當的驅動。當比較電路 72決定差異值△ G時，其會依據前後兩原始像素資料 Gm與 Gm+1之間的差異值 Diff來決定。舉例來說，當差異值 Diff小於某一數值時，比較電路 72會讓差異值△ G等於零，也就是讓過激像素資料 GN+1等於過激像素資料 GN+1(2)；或者是當差異值 Diff大於某一數值時，比較電路 72會依據差異值 Diff來調整差異值△ G的大小，以使液晶面板 30得到適合的驅動。

相較於習知的液晶面板的驅動方法，本發明係揭露一種新的驅動電路以及其驅動方法，而於每一圖框週期內，為液晶面板上的每一像素產生兩筆像素資料，之後並依據所產生的兩筆像素資料，來產生兩資料電壓脈波，且於一個圖框週期內對每一像素施加上述所產生的兩資料電壓脈波，以改變其像素電極的光線透光率。因此，依

據本發明據以實施之液晶顯示器，因一圖框週期內被施予複數個資料電壓脈波，而可促進其液晶分子的扭轉，故其在一個圖框週期內即可完成灰階的轉換，且不會有產生殘影的情況發生

以上所述僅為本發明之較佳實施例，凡依本發明申請專利範圍所做之均等變化與修飾，皆應屬本發明專利之涵蓋範圍。

圖式之簡單說明

圖一為習知液晶顯示器中像素資料值對應於圖框之時序圖。
圖二為習知像素之穿透率對應於圖框之時序圖。
圖三為本發明驅動電路與一液晶面板之功能方塊圖。
圖四為圖三中液晶面板之電路圖。
圖五為依據本發明方法所產生的像素資料其值對應於圖框之時序圖。
圖六為採用本發明之方法後其像素之穿透率對應於圖框之時序圖。
圖七為圖三殘影消除器之功能方塊圖。
圖八為本發明第二實施例中一殘影消除器之功能方塊圖。
圖九為圖八殘影消除器所接收到的原始像素資料對應於圖框之時序圖。
圖十為圖八殘影消除器所輸出的過激像素資料對應於圖框之時序圖。

圖式之符號說明

10 驅動電路
12 訊號控制器
14 殘影消除器
16 時序控制器
18 源極驅動器
20 閘極驅動器

圖式簡單說明

30	液晶面板	32	掃瞄線
34	資料線	36	像素
38	開關元件	39	液晶元件
40	倍頻器	42	處理電路
44	第一影像記憶體	46	第二影像記憶體
48	第一記憶體控制器	50	第二記憶體控制器
60	殘影消除器	62	倍頻器
64	記憶體控制器	66	第一影像記憶體
68	第二影像記憶體	70	第三影像記憶體
72	比較電路	74	處理電路

六、申請專利範圍

1.一種用來驅動一液晶顯示面板之方法，該液晶顯示面板包含有：
複數條掃瞄線；
複數條資料線；以及
複數個像素，每一像素連接於一對應的掃瞄線以及一對應的資料線，且每一像素包含有一開關元件以及一液晶元件，該開關元件連接於該對應的掃瞄線、該對應的資料線以及該液晶元件；
該方法包含：
連續地接收複數筆圖框資料；
每間隔一圖框週期（frame period），依據該等圖框資料，針對每一像素產生複數個資料電壓脈波；以及
於一個圖框週期內，將所產生的該等資料電壓脈波藉由該像素所連接之該資料線施加于該像素之液晶元件，以控制該液晶元件之光線穿透率的變化。

2.如申請專利範圍第1項之方法，其另包含：
延遲該等圖框資料，以產生複數個相對應的延遲圖框資料；以及
當產生該等資料電壓脈波時，藉由比對一當時的圖框資料與一對應的延遲圖框資料，來決定該等資料電壓脈波之電壓值。

3.如申請專利範圍第2項之方法，其中該等資料電壓脈波

分別為一第一資料電壓脈波以及一第二資料電壓脈波，而該等第一資料電壓脈波以及該等第二資料電壓脈波會於一圖框週期內先後地被施加于該等像素之液晶元件。

4.如申請專利範圍第3項之方法，其另包含：
依據該當時的圖框資料與該對應的延遲圖框資料，來決定該第一資料電壓脈波與該第二資料電壓脈波之間的差異值。

5.如申請專利範圍第1項之方法，其中每一圖框資料包含有複數筆像素資料，而每一筆像素資料皆對應於一像素。

6.如申請專利範圍第1項之方法，其另包含：
藉由該像素所連接之掃瞄線施加一掃瞄線電壓于該像素之開關元件，以使該等資料電壓脈波可被施于該像素之液晶元件。

7.一種用來驅動一液晶顯示面板之驅動電路，該液晶顯示面板包含有：
複數條掃瞄線；
複數條資料線；以及
複數個像素，每一像素連接於一對應的掃瞄線以及一對應的資料線，且每一像素包含有一開關元件以及一液晶

元件，該開關元件連接於該對應的掃瞄線、該對應的資料線以及該液晶元件；

該驅動電路包含有：

一殘影消除器，用來每間隔一圖框週期接收一圖框資料，而每一圖框資料包含有複數筆像素資料，每一筆像素資料皆對應於一像素，該殘影消除器會延遲一當時圖框資料，以產生一延遲圖框資料，並依據該當時圖框資料以及該延遲圖框資料，於每一圖框週期內為每一像素產生複數筆過激像素資料；

一源極驅動器，用來於每一圖框資料內根據該殘影消除器對每一像素所產生複數筆過激像素資料，對每一像素產生複數個資料電壓脈波，並將該等資料電壓脈波藉由該像素所連接之該資料線施加于該像素之液晶元件，以控制該液晶元件之光線穿透率的變化；以及

一閘極驅動器，用來施加一掃瞄線電壓于該等像素之開關元件，以使該等資料電壓脈波可被施于該像素之液晶元件。

8.如申請專利範圍第7項之驅動電路，其中該殘影消除器包含有：

一倍頻器，用來將一控制訊號之頻率倍頻，以產生一倍頻訊號；

一第一影像記憶體，用來依據該控制訊號來延遲該等像素資料一圖框週期；

六、申請專利範圍

一處理電路，用來依據該等像素資料以及該第一影像記憶體所延遲的該等像素資料，產生複數筆過激驅動像素資料；

一第二影像記憶體，用來儲存該等過激驅動像素資料；以及

一記憶體控制器，用來依據該倍頻訊號，來控制該第二影像記憶體於每一圖框週期內，對任一像素輸出複數筆該等過激驅動像素資料，以使該源極驅動器根據該第二影像記憶體所輸出的該等過激像素資料，於每一圖框週期內對每一像素產生該等資料電壓脈波。

9.如申請專利範圍第 7項之驅動電路，其中該殘影消除器包含有：

一倍頻器，用來將一控制訊號之頻率倍頻，以產生一倍頻訊號；

一第一影像記憶體，用來接收以及暫存該等像素資料；

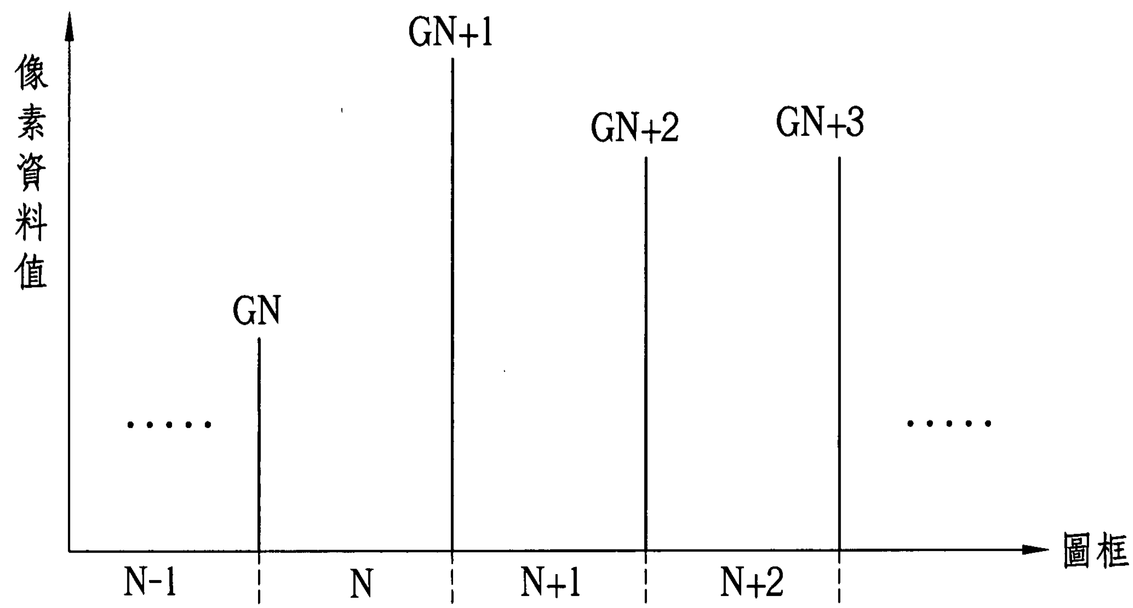
一第二影像記憶體，用來將該第一影像記憶體所儲存並輸出的該等像素資料延遲一圖框週期後輸出；

一第三影像記憶體，用來將該第二影像記憶體所儲存並輸出的該等像素資料延遲一圖框週期後輸出；

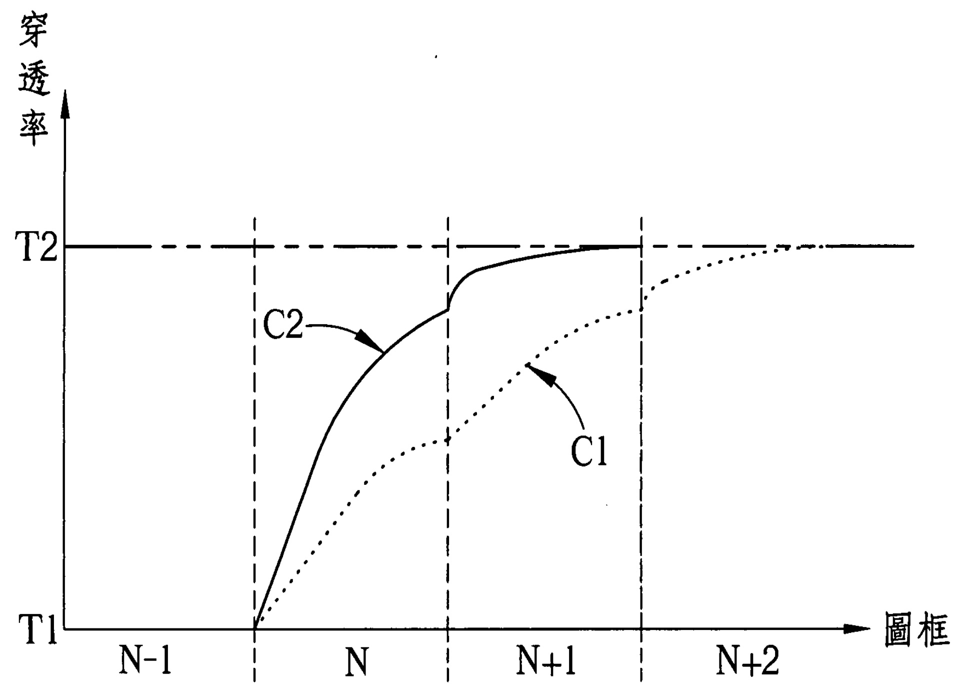
一記憶體控制器，用來依據該倍頻訊號，來控制該第二影像記憶體以及該第三影像記憶體之操作；

一處理電路，用來依據經該第二影像記憶體以及該第三影像記憶體延遲後所輸出的該等像素資料，來產生複數

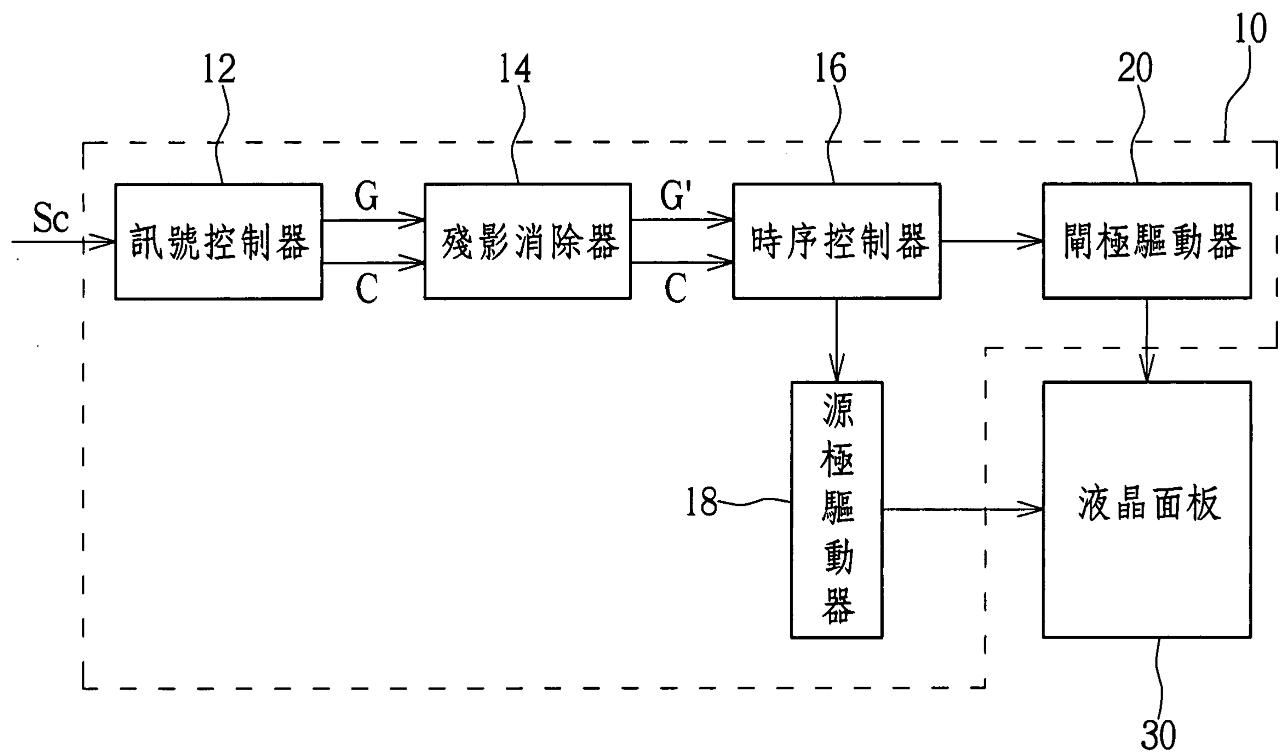
筆過激驅動像素資料；以及
一比較電路，用來比較該第二影像記憶體所延遲的該等像素資料以及該第三影像記憶體所延遲的該等像素資料，以決定該處理電路所產生的該等過激驅動像素資料之資料值。



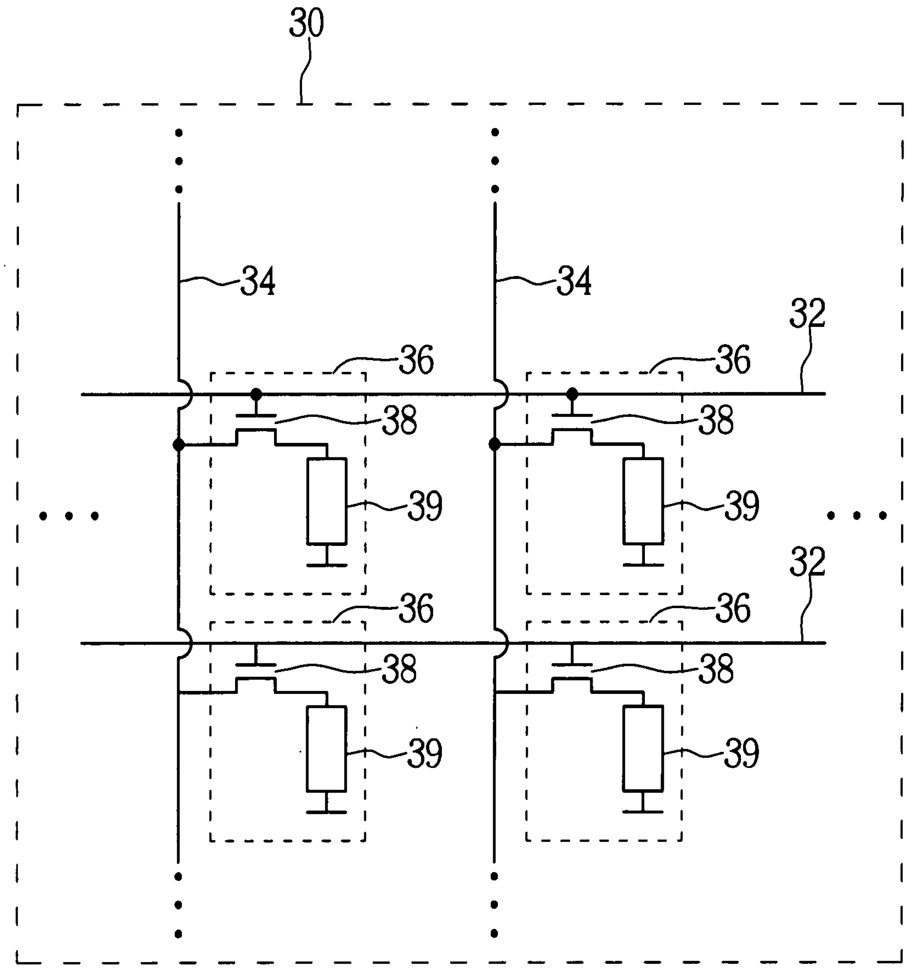
圖一



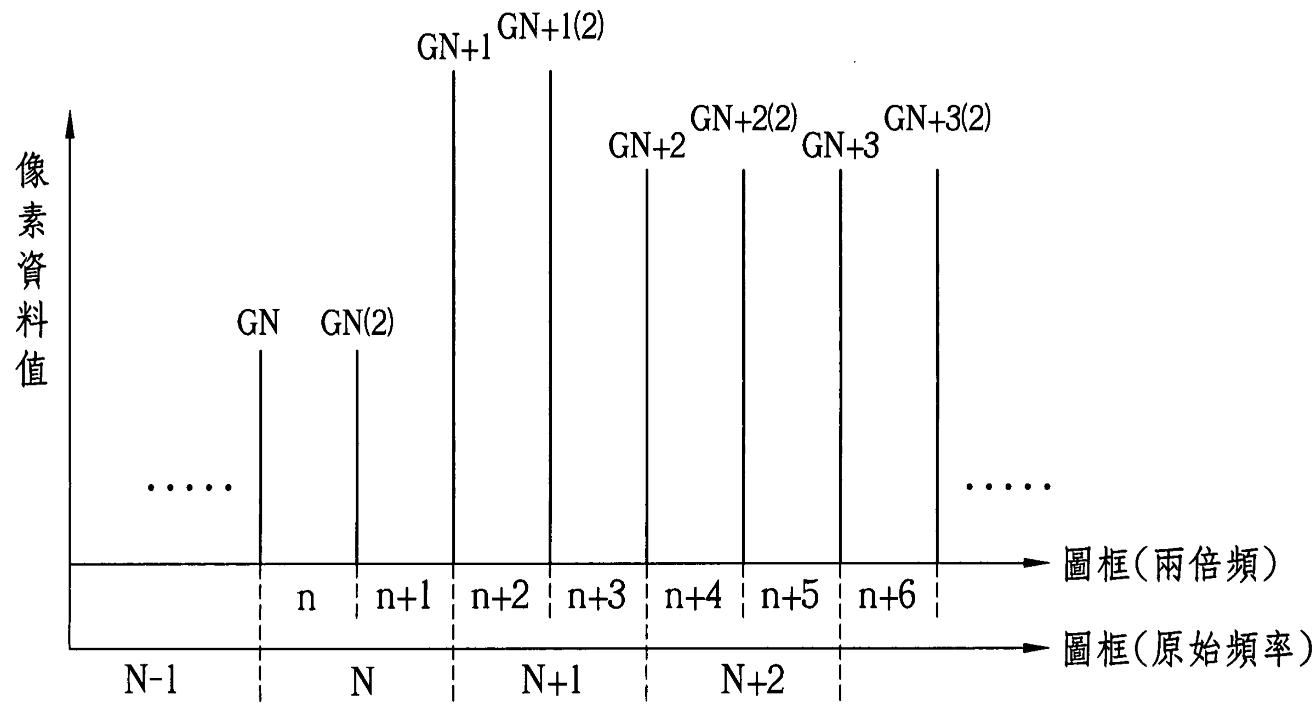
圖二



圖三

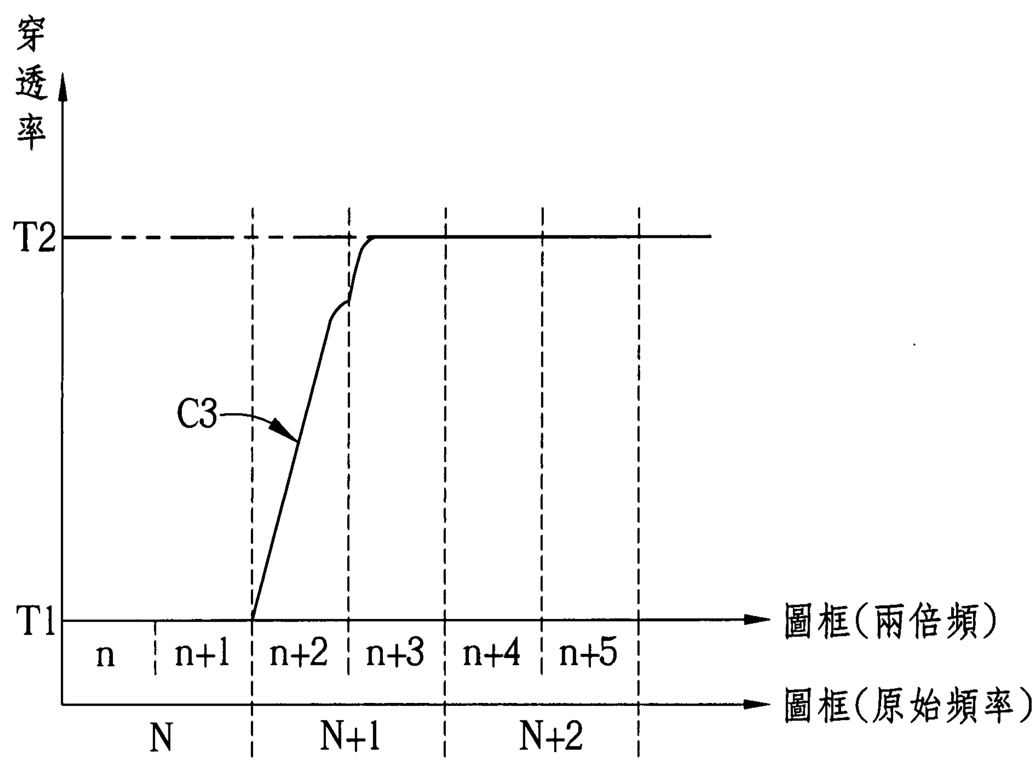


圖四

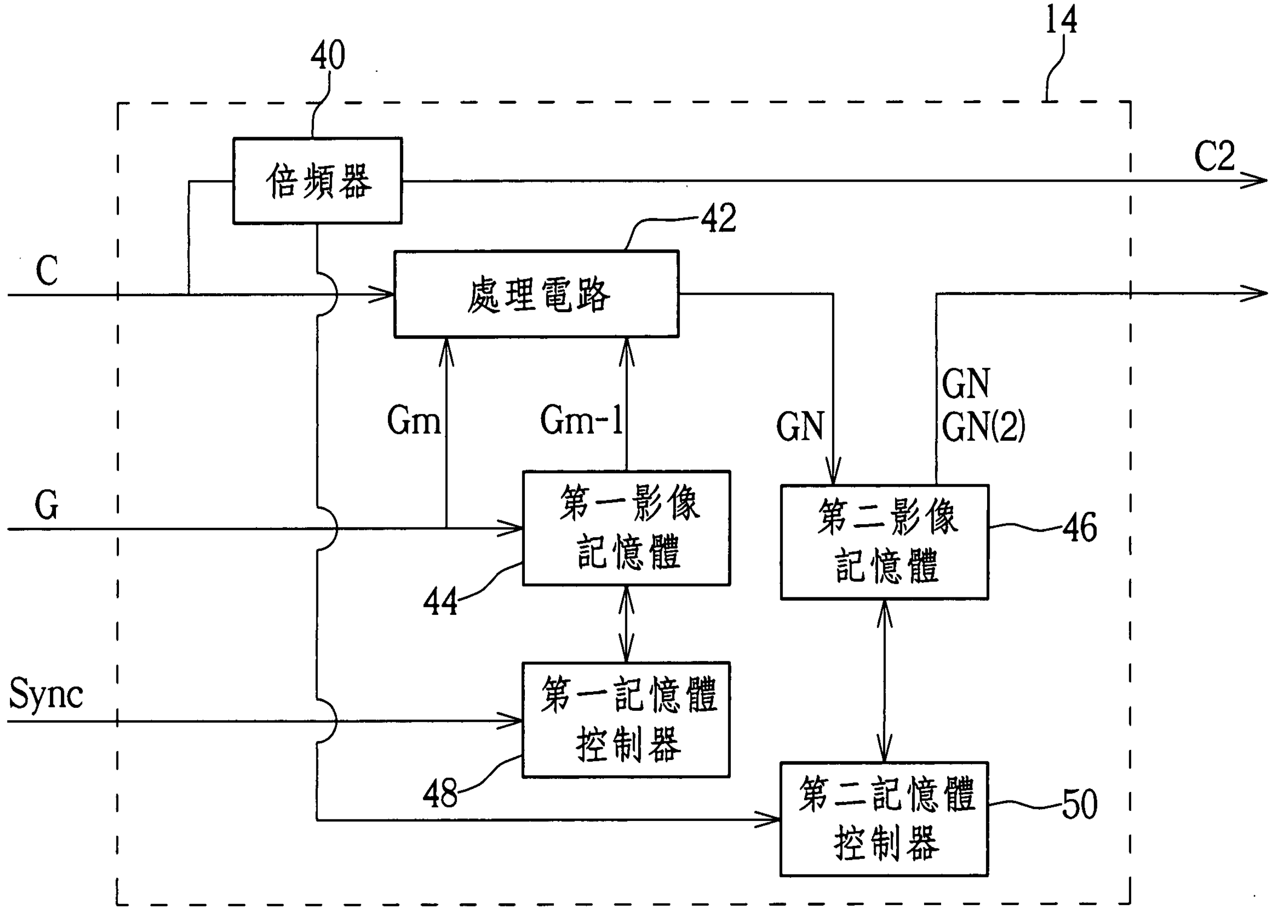


圖五

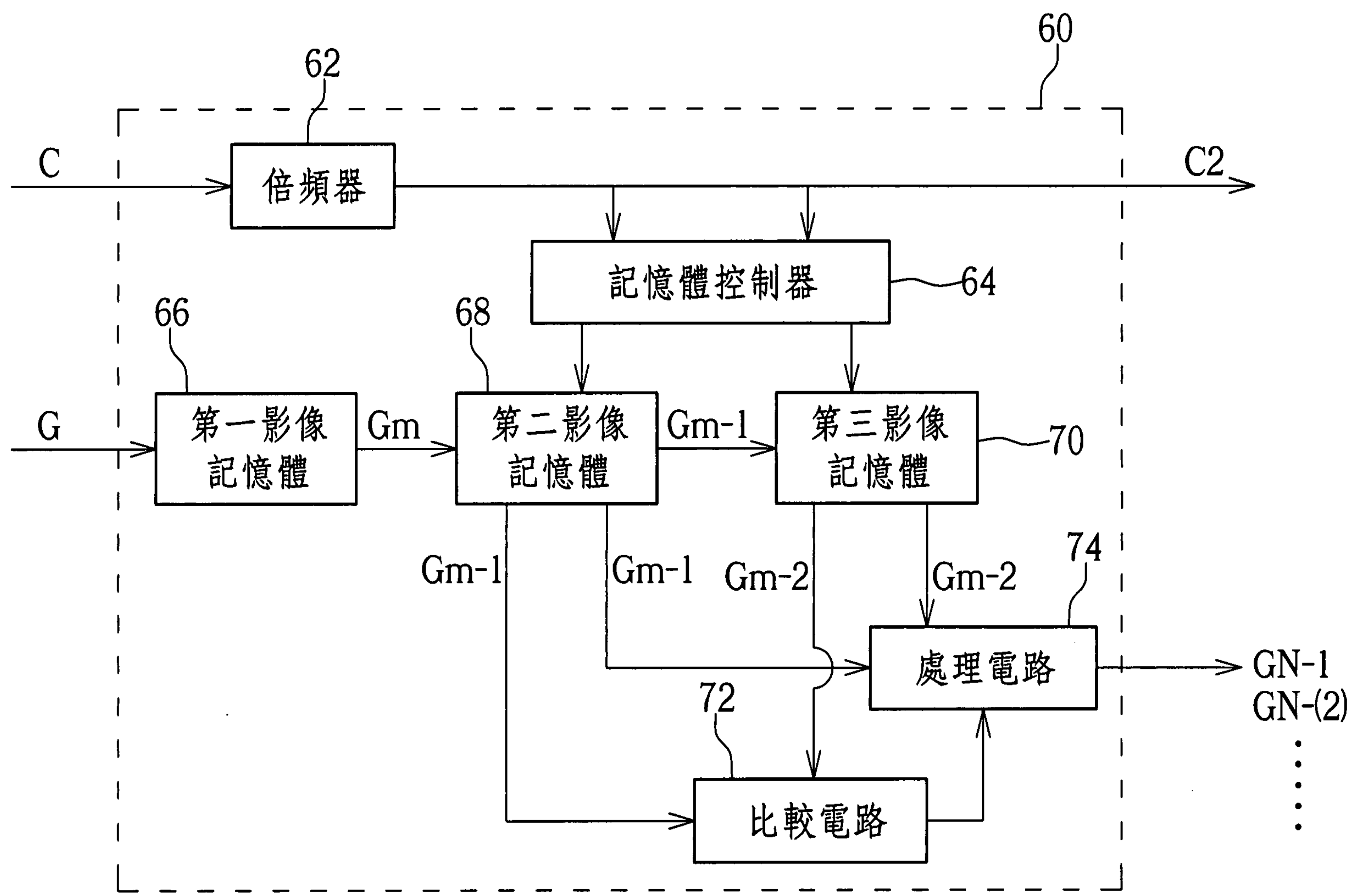
LGD_000301



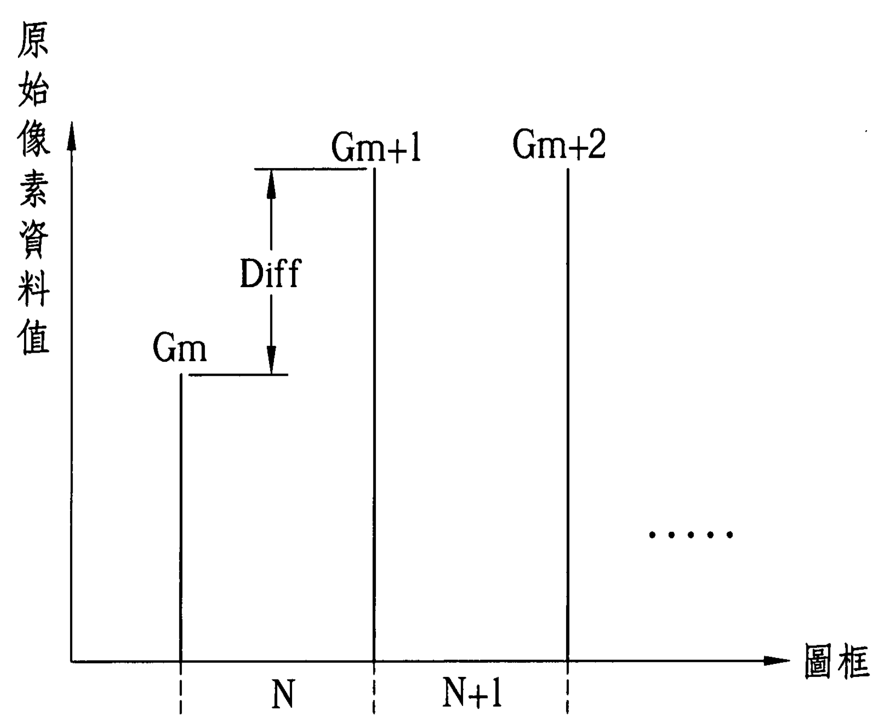
圖六


14
40
倍頻器
C2
42
處理電路
C
Gm
Gm-1
GN
GN
GN(2)
G
第一影像記憶體
第二影像記憶體
46
44
Sync
第一記憶體控制器
48
第二記憶體控制器
50

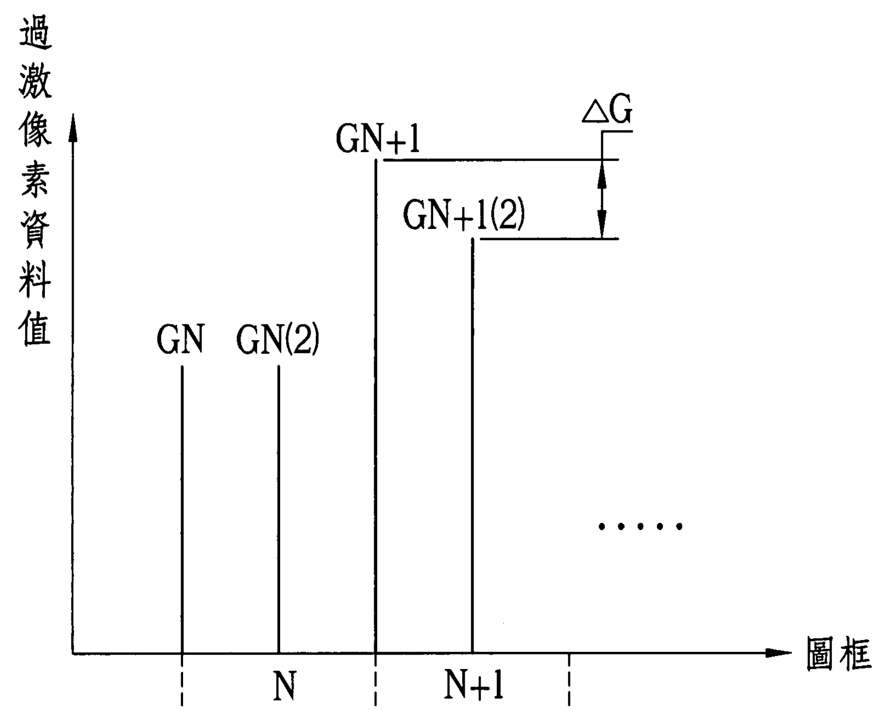
圖七


60
62
C
倍頻器
C2
記憶體控制器
64
66
68
G
第一影像記憶體
Gm
第二影像記憶體
Gm-1
第三影像記憶體
70
Gm-1
Gm-1
Gm-2
Gm-2
74
處理電路
GN-1
GN-(2)
72
比較電路

圖八



圖九



圖十

(4.6版)申請案件名稱:用來驅動一液晶顯示面板之驅動電路及其驅動方法

第 1/27 頁

第 1/27 頁

第 2/27 頁

第 3/27 頁

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第 10/27 頁

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第 11/27 頁

第 11/27 頁

第 12/27 頁

第 12/27 頁

第 13/27 頁

第 13/27 頁

第 14/27 頁

第 14/27 頁

第 15/27 頁

第 15/27 頁

第 16/27 頁

第 16/27 頁

第 17/27 頁

第 17/27 頁

第 18/27 頁

第 18/27 頁

第 19/27 頁

第 19/27 頁

第 20/27 頁

第 21/27 頁

第 22/27 頁

第 23/27 頁

第 24/27 頁

第 25/27 頁

第 25/27 頁

第 26/27 頁

第 27/27 頁

APPLICATION DATA SHEET

Electronic Version v14

Stylesheet Version v14.0

Title of Invention	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD

Application Type : regular, utility

Attorney Docket Number : VASP0001USA

Correspondence address:

Customer Number: 027765

Priority Data:

Doc.No: 092132122; Country -TW ; Date: 2003-11-17 us-priority-claimed

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E-mail:	

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Postal Code of Mailing Address:	
Country of Mailing Address:	TW
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Fax:	
E-mail:	

Attorney Information:

practitioner(s) at Customer Number:

027765

as our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

TRANSMITTAL

Electronic Version v1.1

Stylesheet Version v1.1.0

Title of Invention	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD

Application Number :	
Date :	
First Named Applicant:	Yung-Hung Shen
Confirmation Number:	
Attorney Docket Number:	VASP0001USA

I hereby certify that the use of this system is for OFFICIAL correspondence between patent applicants or their representatives and the USPTO. Fraudulent or other use besides the filing of official correspondence by authorized parties is strictly prohibited, and subject to a fine and/or imprisonment under applicable law.

I , the undersigned, certify that I have viewed a display of document(s) being electronically submitted to the United States Patent and Trademark Office, using either the USPTO provided style sheet or software, and that this is the document(s) I intend for initiation or further prosecution of a patent application noted in the submission. This document(s) will become part of the official electronic record at the USPTO.

Submitted By:	Elec. Sign.
Winston Hsu Registered Number: 41,526	Winston Hsu

Documents being submitted:	Files
us-assignment	VASP0001-usassn.xml
	us-assignment.xsl
	us-assignment.dtd
	VASP0001ASS1.tif
	VASP0001ASS2.tif
us-request	VASP0001-usrequ.xml
	us-request.dtd
	us-request.xsl
us-fee-sheet	VASP0001-usfees.xml
	us-fee-sheet.xsl
	us-fee-sheet.dtd
us-declaration	VASP0001-usdecl.xml
	us-declaration.dtd
	us-declaration.xsl
us-power-of-attorney-grant	VASP0001-uspoat.xml
	us-power-of-attorney-grant.dtd
	us-power-of-attorney-grant.xsl
us-declaration	VASP0001DEC1.tif
us-declaration	VASP0001DEC2.tif
application-body	VASP0001-trans.xml
	us-application-body.xsl
	application-body.dtd
	wipo.ent
	mathml2.dtd
	mathml2-qname-1.mod
	isoamsa.ent
	isoamsb.ent
	isoamsc.ent
	isoamsn.ent
	isoamso.ent
	isoamsr.ent
	isogrk3.ent
	isomfrk.ent
	isomopf.ent
	isomscr.ent
	isotech.ent
	isobox.ent
	isocyr1.ent
	isocyr2.ent
	isodia.ent
	isolat1.ent
	isolat2.ent
	isonum.ent
	isopub.ent
	mmlextra.ent
	mmlalias.ent
	soextblx.dtd
	vasp0001usa-01.tif
	vasp0001usa-02.tif

	vasp0001usa-03.tif vasp0001usa-04.tif vasp0001usa-05.tif vasp0001usa-06.tif vasp0001usa-07.tif vasp0001usa-08.tif vasp0001usa-09.tif vasp0001usa-10.tif
Comments	

FEE TRANSMITTAL

Electronic Version v08

Stylesheet Version v08.0

Title of Invention	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD

Application Number :

Date :

First Named Applicant: Yung-Hung Shen

Attorney Docket Number: VASP0001USA

TOTAL FEE AUTHORIZED $ 425

Patent fees are subject to annual revisions on or about October 1st of each year.

Filing as small entity

BASIC FILING FEE

Fee Description	Fee Code	Amount $	Fee Paid $
Utility Filing Fee	2001	385	385
Subtotal For Basic Filing Fees: $ 385			

EXTRA CLAIM FEES

Fee Description	Extra Claim	Fee Code	Amount $	Fee Paid $
Total Claims : 9	0	2202	9	0
Independent Claims : 2	0	2201	43	0
Subtotal For Extra Claims Fees: $ 0				

ASSIGNMENT FEES

Fee Description	Property Number	Quantity	Fee Code	Amount $	Fee Paid $
Recording Each Patent Assignment Per Property Fee	00000000	1	8021	40	40
Subtotal For Additional Fees: $40					

AUTHORIZED BILLING INFORMATION

The commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit account number: 500801

Access Code ****

Deposit name: NORTH AMERICA INTERNATIONAL PATENT OFFICE

Deposit authorized name: WINSTON HSU

LGD_000316

Signature:	VAEB-JMXX-8IIL
Date (YYYYMMDD):	2004-01-07

Charge Assignment Fees Required Under 37 C.F.R. Section 1.21 (h).

Charge Any Additional Fee Required Under 37 C.F.R. Sections 1.16 and 1.17.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Electronic Version v11

Stylesheet Version v10

Title of Invention	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD

As the below named inventors, we declare that:

This declaration is directed to the invention titled: " DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD"

We believe that we are the original and first inventors of the subject matter which is claimed and for which a patent is sought;

We have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

We acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

All statements made herein of own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTORS:

Inventor 1: Yung-Hung Shen	Inventor
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Inventor 2: Shih-Chung Wang	Inventor
Signature :	Citizen of : TW
Inventor 3: Yuh-Ren Shen	Inventor

Signature :	Citizen of : TW
Inventor 4: Cheng-Jung Chen	Inventor
Signature :	Citizen of : TW

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor , I hereby declare that :

I believe I am the sole (if only one name appears below) , or joint (if more than one name appears) , original and first inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled :

"DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD"

__+__ The specification for the above entitled invention is filed herewith.

______ The specification for the above entitled invention was filed previously with application serial number: ________ Filing Date: ________

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of the invention disclosed in this application in accordance with Title 37, Code of Federal Regulations, Section 1.56 (a). I further acknowledge the duty in any continuation-in-part application to disclose to the Patent and Trademark Office all information known to be material to the patentability of the invention disclosed in this application, as defined in 1.56, which became available to me between the filing date of the prior application and the filing date of this application

PRIORITY CLAIM

______ There is no claim of priority

__+__ Claim of priority is based on the following:

Filing No. in Taiwan, R.O.C: 092132122

Filing Date in Taiwan, R.O.C: 11/17/2003

POWER OF ATTORNEY

As a named inventor, I hereby appoint the following attorneies to prosecute this application and to transact all related business in the Patent and Trademark Office:

Winston Hsu Registration# 41,526 WinstonHsu@naipo.com.tw

P.O. Box 506,
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U.S.A
TEL: (02)8923-7350

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued hereon.

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Citizen of: R.O.C.

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Citizen of: R.O.C.

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Citizen of: R.O.C.

Date: ____________ Cheng-Jung Chen

Printed Name: Cheng-Jung Chen
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Citizen of: R.O.C.

POWER OF ATTORNEY OR AUTHORIZATION OF AGENT

Electronic Version v05

Stylesheet Version v05.0

Title of Invention	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD

First Named Applicant :	Yung-Hung Shen
Attorney Docket Number :	VASP0001USA

I hereby appoint the registered practitioner(s) at Customer Number:

027765

as attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

I am the Applicant/Inventor.

Full Name of Applicant of Record:

Winston Hsu	
Signature: Winston Hsu	Date: 2004-01-07

Electronic Version
Stylesheet Version v1.1.1

Description

DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to a driving circuit of a liquid crystal display (LCD) panel and its related driving method, and more particularly, to a driving circuit for applying over two data impulses to a pixel electrode within one frame period, and its related driving method.

[0003] 2. Description of the Prior Art

[0004] A liquid crystal display (LCD) has advantages of lightweight, low power consumption, and low divergence and is applied to various portable equipment such as notebook computers and personal digital assistants (PDAs). In addition, LCD monitors and LCD televisions are gaining in popularity as a substitute for traditional cathode ray tube (CRT) monitors and televisions. However, an LCD does have some disadvantages. Because of the limitations of physical characteristics, the liquid crystal molecules need to be twisted and rearranged when changing input data, which can cause the images to be delayed. For satisfying the rapid switching requirements of multimedia equipment, improving the response speed of liquid crystal is desired.

[0005] Generally when driving an LCD, a driving circuit receives a plurality of frame data and then generates corresponding data impulses, scan voltages, and timing signals, according to the frame data, in order to control pixel operation of the LCD. Each of the frame data includes data for refreshing all of the pixels within a frame period; thus each of the frame data can be regarded as including a plurality of pixel data, and each of the pixel data is for defining the gray level that a pixel is required to reach within a frame period. In the general standard, each pixel can switch among 256 (2^8) gray levels, thus each of the pixel data is 8 bits in length.

[0006] Please refer to Fig.1 showing a timing diagram of pixel data values varying in accordance with the frames. When driving a pixel, the driving circuit receives a plurality of pixel data used for driving the pixel in sequence. As shown in Fig.1, GN, GN+1, GN+2 are the pixel data received in frame periods N, N+1, N+2, and the driving circuit determines the gray level of the pixel in the frame periods N, N+1, N+2 according to the values of the pixel data GN, GN+1, GN+2. In general, the larger the value of the pixel data is, the larger the gray level is. The driving circuit generates a data impulse corresponding to a frame period according to the pixel data GN, GN+1, GN+2, and applies the pulse to a pixel electrode of the corresponding pixel to have the pixel be in the appropriate gray level as required within each frame period.

[0007] Please refer to Fig.2 showing a timing diagram of different transmission rates of a pixel, varying in accordance with the frames. Two curves C1, C2 are measured when the driving circuit changes the transmission rate from T1 to T2 beginning at frame period N. The curve C1 shows the transmission rate of a pixel not overdriven corresponding to the frames, and the curve C2 shows the transmission rate of the pixel overdriven corresponding to the frames. The U.S. published application No. 2002/0050965 is one of the references of the conventional overdriving method. There is a time delay when charging liquid crystal molecules, so that they cannot twist at a predetermined angle at a predetermined transmission rate. As shown by the curve C1, in the case of not being overdriven, the transmission rate cannot reach a predetermined level in the frame period N but has to wait until the frame period N+2. Such a delay causes blurring. In order to improve that, some conventional LCD are overdriven, which means applying a higher or a lower data impulse to the pixel electrode to accelerate the reaction speed of the liquid crystal molecules, so that the pixel can reach the predetermined gray level in a predetermined frame period. As shown by the curve C2, in the case of being overdriven, although the reaction speed of the liquid crystal molecules is faster than in case of not being overdriven, the transmission rate has to wait until frame period N+1 to reach T2. Thus, the requirement of reaching T2 in the frame period N still remains unsatisfied.

SUMMARY OF INVENTION

[0008] It is therefore a primary objective of the claimed invention to provide a driving circuit of an LCD panel and its relating driving method to solve the problem mentioned above.

[0009] Briefly, the present invention provides a method for driving an LCD panel. The LCD panel includes a plurality of scan lines, a plurality of data lines, and a plurality of pixels. Each pixel is connected to a corresponding scan line and a corresponding data line, and each pixel includes a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device. The method includes receiving continuously a plurality of frame data, generating a plurality of data impulses for each pixel in every frame period according to the frame data and applying the data impulses to the liquid crystal device of one of the pixels within one frame period via the data line connected to the pixel in order to control the transmission rate of the liquid crystal device of the pixel.

[0010] The present invention further provides a driving circuit for driving an LCD panel including a blur clear converter for receiving frame data every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel, the blur clear converter delaying current frame data to generate delayed frame data and generating a plurality of overdriven pixel data in every frame period for each pixel; a source driver for generating a plurality of data impulses to each pixel according to the plurality of overdriven pixel data generated by the blur clear converter and applying the data impulses to the liquid crystal device of the pixel via the scan line connected to the pixel in order to control the transmission rate of the liquid crystal device; and a gate driver for applying a scan line voltage to the switch device of the pixel so that the data impulses can be applied to the liquid crystal device of the pixel.

[0011] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0012] Fig.1 is a timing diagram of the pixel data values varying in accordance with the frames according to the prior art.

[0013] Fig.2 is a timing diagram of different transmission rates of the pixel varying in accordance with the frames.

[0014] Fig.3 is a block diagram of a driving circuit and an LCD panel according to the present invention.

[0015] Fig.4 is a circuit diagram of the LCD panel.

[0016] Fig.5 is a timing diagram of pixel data values varying in accordance with frames.

[0017] Fig.6 is a timing diagram of the transmission rate of the pixel varying in accordance with the frames.

[0018] Fig.7 is a block diagram of the blur clear converter according to the first embodiment of the present invention.

[0019] Fig.8 is a block diagram of the blur clear converter according to the second embodiment of the present invention.

[0020] Fig.9 is a timing diagram of original pixel data received by the blur clear converter varying in accordance with the frames.

[0021] Fig.10 is a timing diagram of overdriven pixel data generated by the blur clear converter varying in accordance with the frames.

DETAILED DESCRIPTION

[0022] Please refer to Fig.3 showing a block diagram of a driving circuit 10 and an LCD panel 30 according to the present invention. The driving circuit 10 is for driving the LCD panel 30, which includes a signal controller 12, a blur clear converter 14, a timing controller 16, a source driver 18, and a gate driver 20. The signal controller 12 is for receiving composite video signals Sc, which includes frame data and timing data for driving the LCD panel 30, and processing the composite video signals Sc to separate them into frame signals G and control signals C. Subsequently, the blur clear converter 14 continuously receives the control signals C and the frame data included in the frame signals G and generates processed frame signals G including a plurality of overdriven data according to the frame data. The timing controller 16 controls the source driver 18 and the gate driver 20 according to the frame signals G and the control signals C so that the source driver 18 and the gate driver 20 generate corresponding data line voltages and scan line voltages according to the plurality of overdriven data included in the frame signals G in order to drive the LCD panel 30 to generate images corresponding to the composite video signals Sc.

[0023] Please refer to Fig.4 showing a circuit diagram of the LCD panel 30. The LCD panel 30 includes a plurality of scan lines 32, a plurality of data lines 34, and a plurality of pixels 36. Each pixel 36 is connected to a corresponding scan line 32 and a corresponding data line 34, and each pixel 36 has a switching device 38 and a liquid crystal device 39 a.k.a. a pixel electrode. The switching device 38 is connected to the corresponding scan line 32 and the corresponding data line 34, and the source driver 18 and the gate driver 20 control the operation of each pixel 36 via the scan line 32 and the data line 34. To drive the LCD 30, scan voltages are applied to the scan lines 32 to turn on the switching devices 38, and data voltages are applied to the data lines 34 and transmitted to the pixel electrodes 30 through the switching devices 38. Therefore, when the scan voltages are applied to the scan lines 32 to turn on the switching devices 38, the data voltages on the data lines 34 will charge the pixel electrodes 39 through the switch devices 38, thereby twisting the liquid crystal molecules. When the scan voltages on the scan lines 32 are removed to turn off the switching devices 38, the data lines 34 and the pixels 36 will disconnect, and the pixel electrodes 39 will remain charged. The scan lines 32 turn the switching devices 38 on and off repeatedly so that the pixel electrodes 39 can be repeatedly charged. Different data voltages cause different twisting angles and show different transmission rates. Hence, the LCD 30 displays various images.

[0024] Please refer to Fig.5 showing a timing diagram of pixel data values varying in accordance with frames. According to the present invention, when driving any pixel 36 of the LCD panel 30, the driving circuit 10 generates a plurality of pixel data used for driving the pixel in sequence. As shown in Fig.5, GN, GN(2), GN+1, GN+1(2), GN+2, GN+2(2), GN+3, GN+3(2) are the pixel data generated in frame periods N, N+1, N+2, N+3. The driving circuit 10 generates two pieces of pixel data for each pixel 36 in every frame period. The driving circuit 10 drives the pixel to reach gray levels in the frame periods N, N+1, N+2, N+3 according to the values of the pixel data GN - GN+2(2). For instance, when the pixel data GN, GN(2) are generated, the source driver of the driving circuit 10 converts the pixel data GN, GN(2) into two corresponding data impulses and then applies them to the liquid crystal device 39 via the data line 32 in the frame period N in order to control the transmission rate of the liquid crystal device 39. Similarly, data impulses corresponding to the pixel data GN+1 - GN+3(2) are applied respectively to corresponding pixel electrodes 39 every half a frame period. Same as the prior art, the larger the value of the pixel data is, the higher the voltage of the corresponding data impulse is, and the larger the gray level value is.

[0025] Please refer to Fig.6 showing a timing diagram of the transmission rate of the pixel 36 varying in accordance with the frames. As described above, the driving circuit 10 generates two pieces of pixel data in each frame period, and then the source driver 18 generates two corresponding data impulses according to the two pieces of pixel data and applies them to the pixel electrode 39 of the corresponding pixel 36 in order to control the transmission rate and gray level of the pixel electrode 39. As shown in Fig.6, the driving circuit 10 changes the transmission rate of the pixel electrode 39 of a pixel 36 from T1 to T2 in the frame period N+1. The pixel electrode 39 is applied with two data impulses corresponding to the pixel data GN+1, GN+1(2) in the frame period N+1 at a time interval of half a frame period. As shown in Fig.6, although the transmission rate of the pixel electrode 39 cannot reach T2 in the first half period n+2 of the frame period N+1, in the later half period n+3 of the frame period N+1, the pixel electrode 39 is applied with another data impulse, so that the transmission rate can reach T2 in the frame period N+1 as required. Therefore, blurring will not occur.

[0026] In the present embodiment, the two pieces of pixel data of each pixel in every frame period are generated by the blur clear converter 14. Please refer to Fig.7 showing a block diagram of the blur clear converter 14. The blur clear converter 14 includes a multiplier 40, a processing circuit 42, a first image memory 44, a second image memory 46, a first memory controller 48, and a second memory controller 50. The multiplier 40 is for doubling the frequency of the control signal C to generate a multiplied signal C2. The first image memory 44 is controlled by the first memory controller 48 to delay current pixel data Gm for a frame period to generate delayed pixel data Gm-1 according to the control signal C. The processing circuit 42 generates a plurality of overdriven pixel data GN according to the current pixel data Gm and the delayed pixel data Gm-1. The second image memory 46 stores the overdriven pixel data GN, and the second memory controller 50 controls the second image memory 46 to output two overdriven pixel data GN, GN(2) to each pixel 36 within a frame period according to the multiplied signal C2 in order to have the source driver 18 apply two data impulses to a specific pixel 36 within a frame period according to the two overdriven pixel data GN, GN(2).

[0027] Please refer to Fig.8 showing a block diagram of the blur clear converter 60 according to the second embodiment of the present invention. The blur clear converter 60 functions the same as the blur clear converter 14, which includes a multiplier 62, a first image memory 66, a second image memory 68, a third image memory 70, a memory controller 64, a processing circuit 74, and a comparing circuit 72. The multiplier 62 is for doubling the frequency of the control signal C to generate a multiplied signal C2. The first image memory 66 is for receiving and temporarily storing a plurality of pixel data G. The second image memory 68 delays the plurality of pixel data G for a frame period to generate delayed pixel data Gm-1. The third image memory 70 delays the pixel data Gm-1 for a frame period to generate delayed pixel data Gm-2. Thus the pixel data Gm-2 lags the pixel data Gm-1 for a frame period, and so does the pixel data Gm-1 with respect to the pixel data Gm. The memory controller 64 controls the second image memory 68 and the third image memory 70 to output two overdriven pixel data in each frame period according to the multiplied signal C2. The processing circuit 74 generates two pieces of overdriven pixel data GN-1, GN-1(2) for each pixel 36 in every frame period according to the pixel data Gm-1, Gm-2. The comparing circuit 72 compares the pixel data Gm-1 with the pixel data Gm-2 to determine the values of the overdriven pixel data GN-1, GN-1(2).

[0028] Please refer to Fig.9 showing a timing diagram of original pixel data received by the blur clear converter 60 varying in accordance with the frames, and Fig.10 showing a timing diagram of overdriven pixel data generated by the blur clear converter 60 varying in accordance with the frames. As shown in Fig.9, the original pixel data received by the blur clear converter 60 in the frame periods N and N+1 are respectively Gm and Gm+1, with a difference Diff between each other. The blur clear converter 60 generates the two overdriven pixel data GN+1, GN+1(2) with a difference ΔG between each other according to the original pixel data Gm, Gm+1. The difference ΔG is determined by the comparing circuit 72 in Fig.8 for driving the pixels 36 according to difference conditions. The difference ΔG is determined according to the difference Diff between the original pixel data Gm and Gm+1. For instance, when the difference Diff is less than a specific value, the comparing circuit 72 determines the difference ΔG as 0, that is equating the overdriven pixel data GN+1 to the overdriven pixel data GN+1(2). Or when the difference Diff is larger than a specific value, the comparing circuit 72 modulates the difference ΔG to drive the LCD panel 30 properly.

[0029] In contrast to the prior art, the present invention discloses a driving circuit and relating driving method to generate two pieces of pixel data in each frame period for every pixel on an LCD panel and then to generate two data impulses according to the two pieces of pixel data and to apply them to each pixel within a frame period in order to change the transmission rate of a pixel electrode. Thus, each of the pixels of the LCD panel is applied of a plurality of data impulses within a frame period, so that liquid crystal molecules of the pixels can twist to reach a predetermined gray level within a frame period, and blurring will not occur.

[0030] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Claims

[c1] 1.A method for driving a liquid crystal display (LCD) panel, the LCD panel comprising:
a plurality of scan lines;
a plurality of data lines; and
a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device, and
the method comprising:
receiving continuously a plurality of frame data;
generating a plurality of data impulses for each pixel within every frame period according to the frame data; and
applying the data impulses to the liquid crystal device of one of the pixels within one frame period via the data line connected to the pixel in order to control a transmission rate of the liquid crystal device of the pixel.

[c2] 2. The method of claim 1 further comprising:
delaying the frame data to generate a plurality of corre-

sponding delayed frame data; and
comparing current frame data and corresponding delayed data to determine voltage values of the data impulses when generating the data impulses.

[c3] 3.The method of claim 2 wherein the data impulses are a first data impulse and a second data impulse applied to the liquid crystal device of the pixel in sequence within the frame period.

[c4] 4. The method of claim 3 further comprising:
determining a difference between the first data impulse and the second data impulse according to the current frame data and the corresponding delayed frame data.

[c5] 5. The method of claim 1 further comprising:
applying a scan line voltage to the switch device of the pixel via the scan line connected to the pixel in order to have the data impulses be applied to the liquid crystal device of the pixel.

[c6] 6. The method of claim 1 wherein each frame data comprises a plurality of pixel data, and each pixel data corresponds to a pixel.

[c7] 7. A driving circuit for driving an LCD panel, the LCD panel comprising:
a plurality of scan lines;

a plurality of data lines; and

a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device,

the driving circuit comprising:

a blur clear converter for receiving frame data every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel, the blur clear converter delaying current frame data to generate delayed frame data and generating a plurality of overdriven pixel data within every frame period for each pixel;

a source driver for generating a plurality of data impulses to each pixel according to the plurality of overdriven pixel data generated by the blur clear converter and applying the data impulses to the liquid crystal device of the pixel via the scan line connected to the pixel within one frame period in order to control transmission rate of the liquid crystal device; and

a gate driver for applying a scan line voltage to the switch device of the pixel so that the data impulses can be applied to the liquid crystal device of the pixel.

[c8] 8. The driving circuit of claim 7 wherein the blur clear converter further comprises:
a multiplier for multiplying a frequency of a control signal to generate a multiplied signal;
a first image memory for delaying the pixel data for a frame period;
a processing circuit for generating the plurality of overdriven pixel data according to the pixel data and the pixel data delayed by the first image memory;
a second image memory for storing the overdriven pixel data;
a memory controller for controlling the second image memory according to the multiplied signal to output the plurality of overdriven pixel data to any pixel so that the source driver generates the data impulses to each pixel within one frame period according to the overdriven pixel data output by the second image memory.

[c9] 9. The driving circuit of claim 7 wherein the blur clear converter further comprises:
a multiplier for multiplying a frequency of a control signal to generate a multiplied signal;
a first image memory for receiving and temporarily storing the pixel data;
a second image memory for delaying the pixel data stored and output by the first image memory for a frame

period;

a third image memory for delaying the pixel data stored and output by the second image memory for a frame period;

a memory controller for controlling the second image memory and the third image memory according to the multiplied signal;

a processing circuit for generating the plurality of overdriven pixel data according to the pixel data delayed and output by the second image memory and the third image memory; and

a comparing circuit for comparing the pixel data delayed by the second image memory with the pixel data delayed by the third image memory in order to determine data values of the overdriven pixel data generated by the processing circuit.

Electronic Version

Stylesheet Version v1.1.1

DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD

Abstract

A method for driving a liquid crystal display (LCD) panel includes receiving continuously a plurality of frame data, generating a plurality of data impulses for each pixel every frame period according to the frame data, and applying the data impulses to a liquid crystal device of a pixel within a frame period via the data line connected to the pixel in order to control a transmission rate of the liquid crystal device.

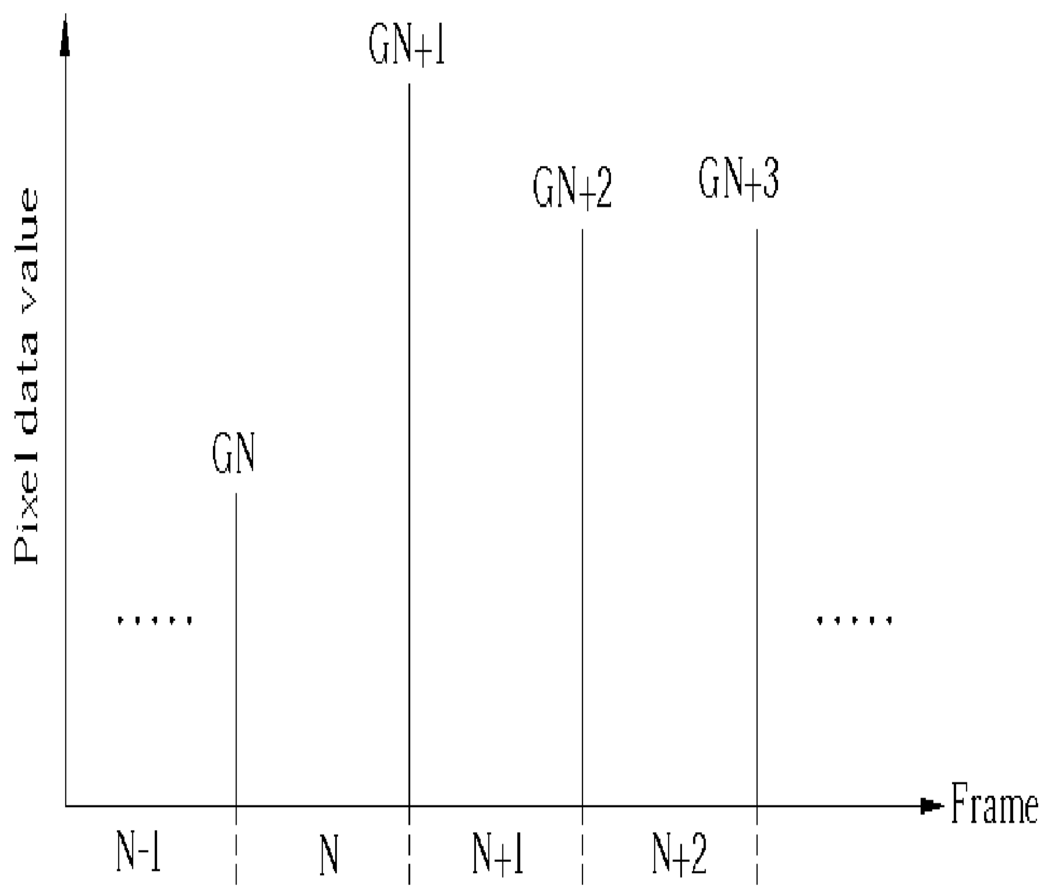


Fig. 1 Prior art

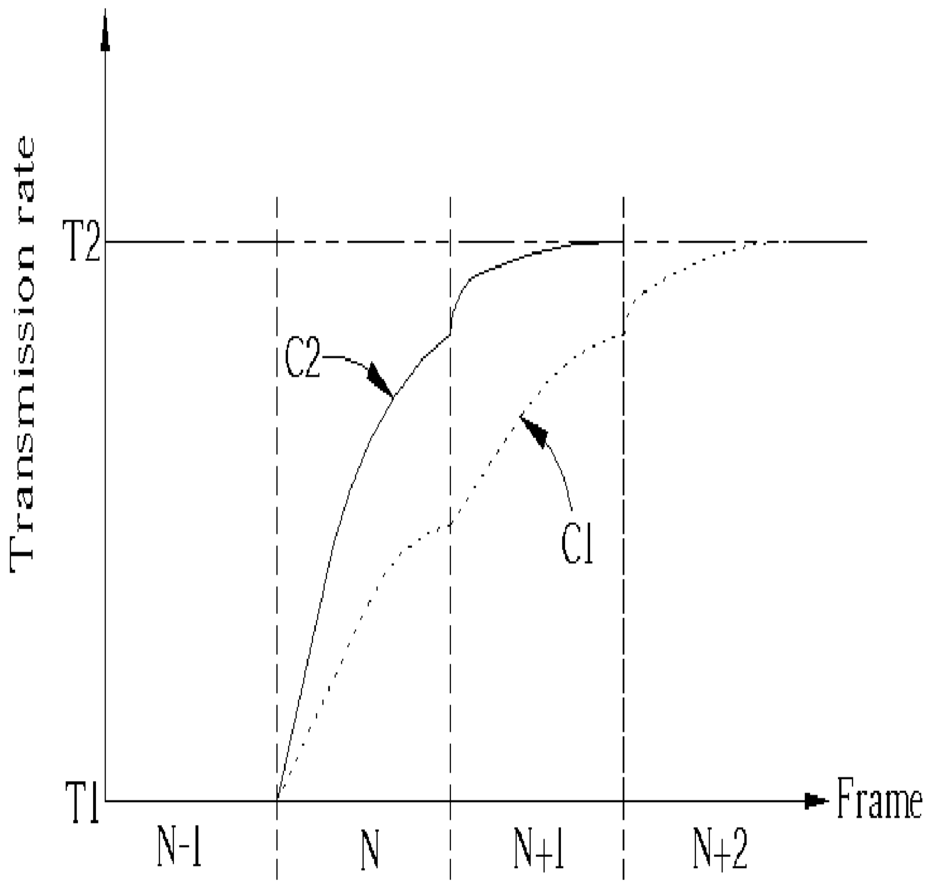


Fig. 2 Prior art

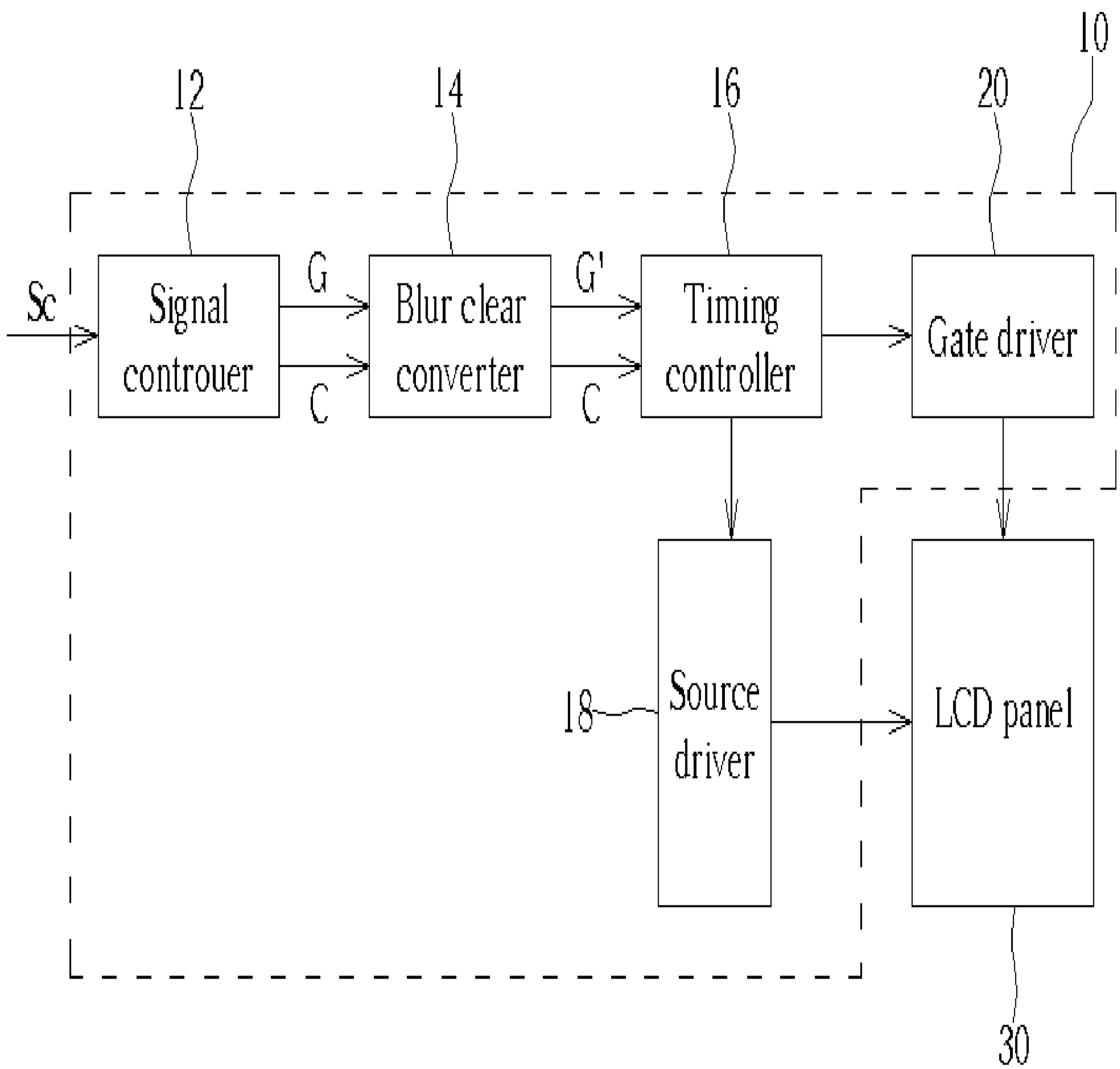

10
12
14
16
20
Sc
Signal
controuer
G
C
Blur clear
converter
G'
C
Timing
controller
Gate driver
18
Source
driver
LCD panel
30

Fig. 3

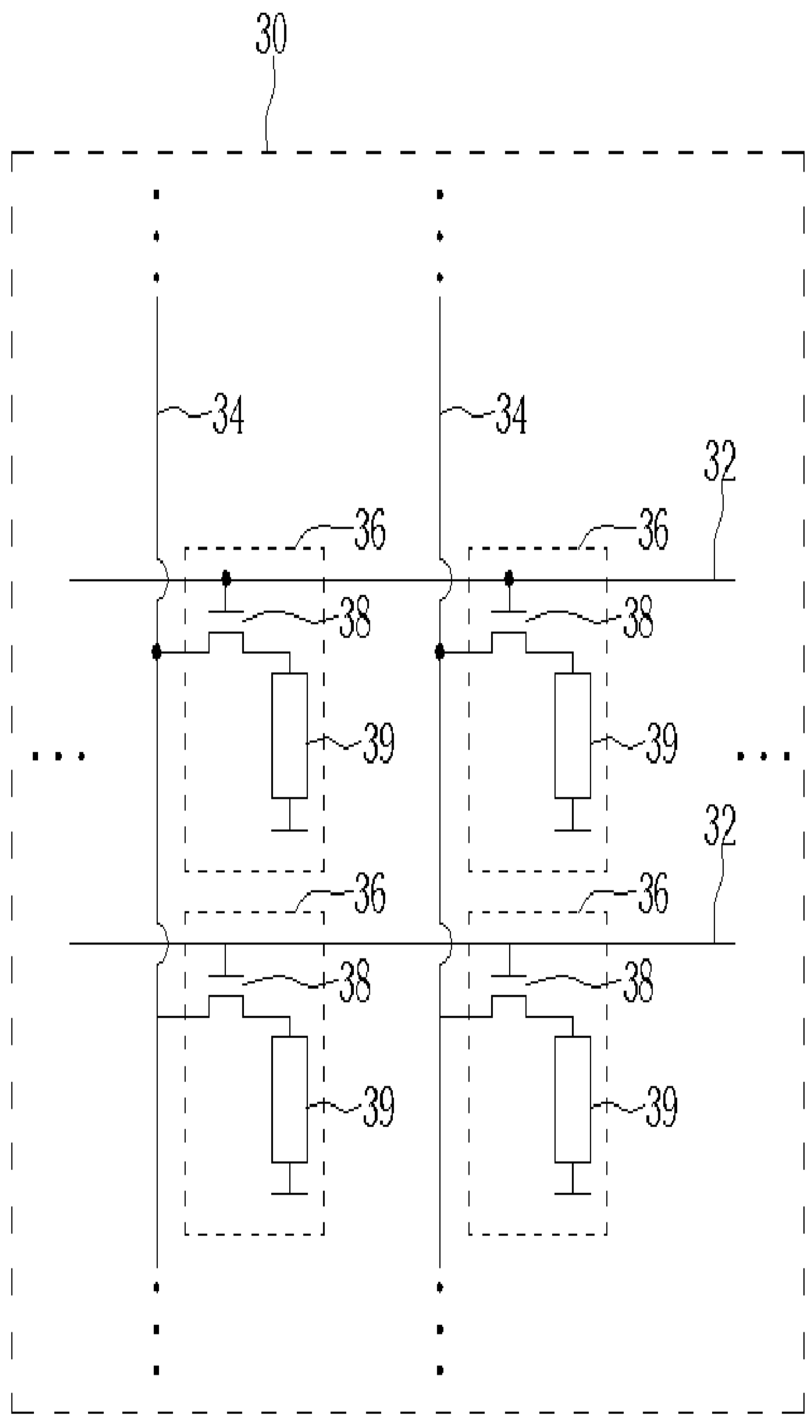
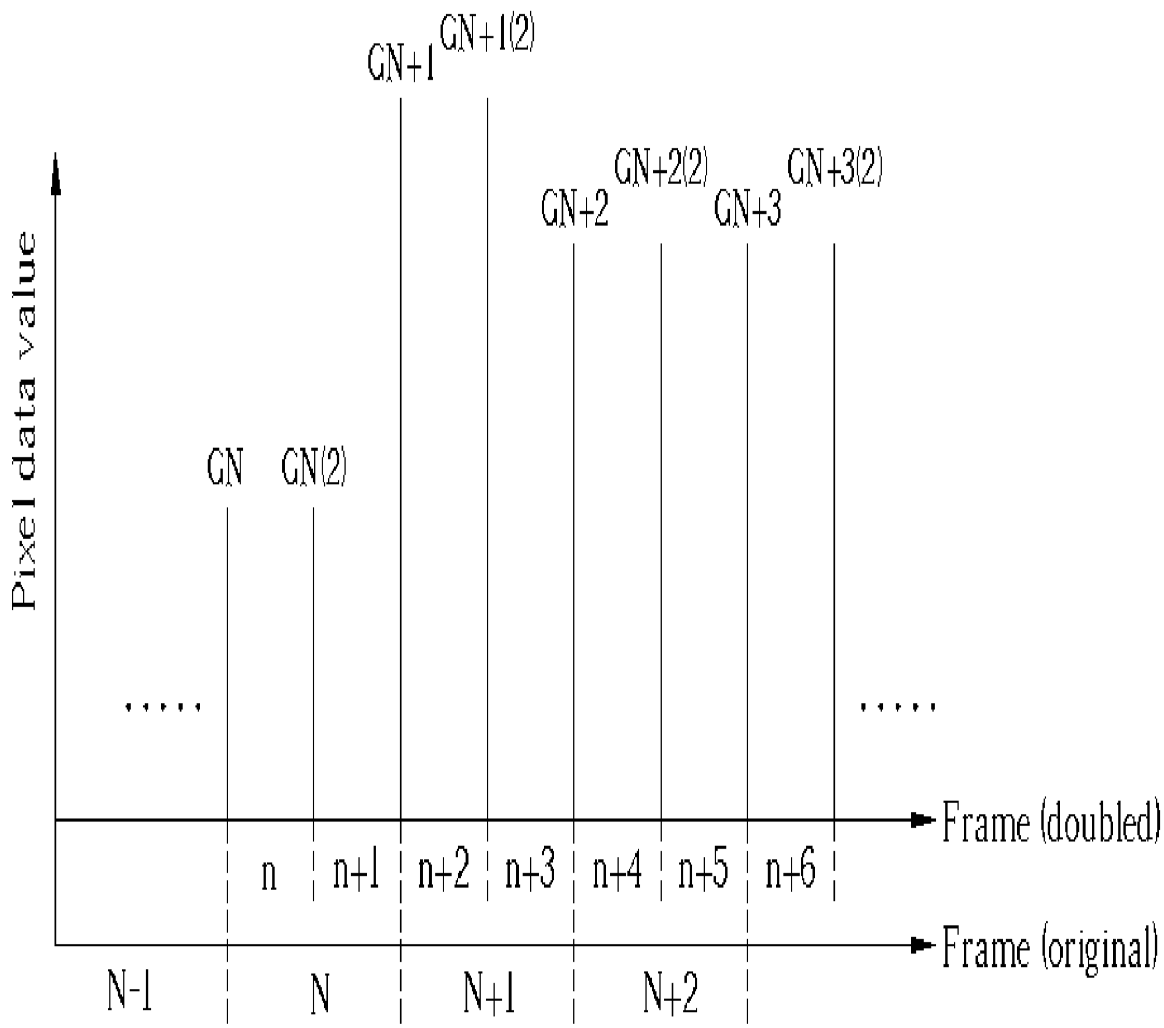


Fig. 4



GN+1
GN+1(2)
GN+2
GN+2(2)
GN+3
GN+3(2)
Pixel data value
GN
GN(2)
Frame (doubled)
n
n+1
n+2
n+3
n+4
n+5
n+6
Frame (original)
N-1
N
N+1
N+2

Fig. 5

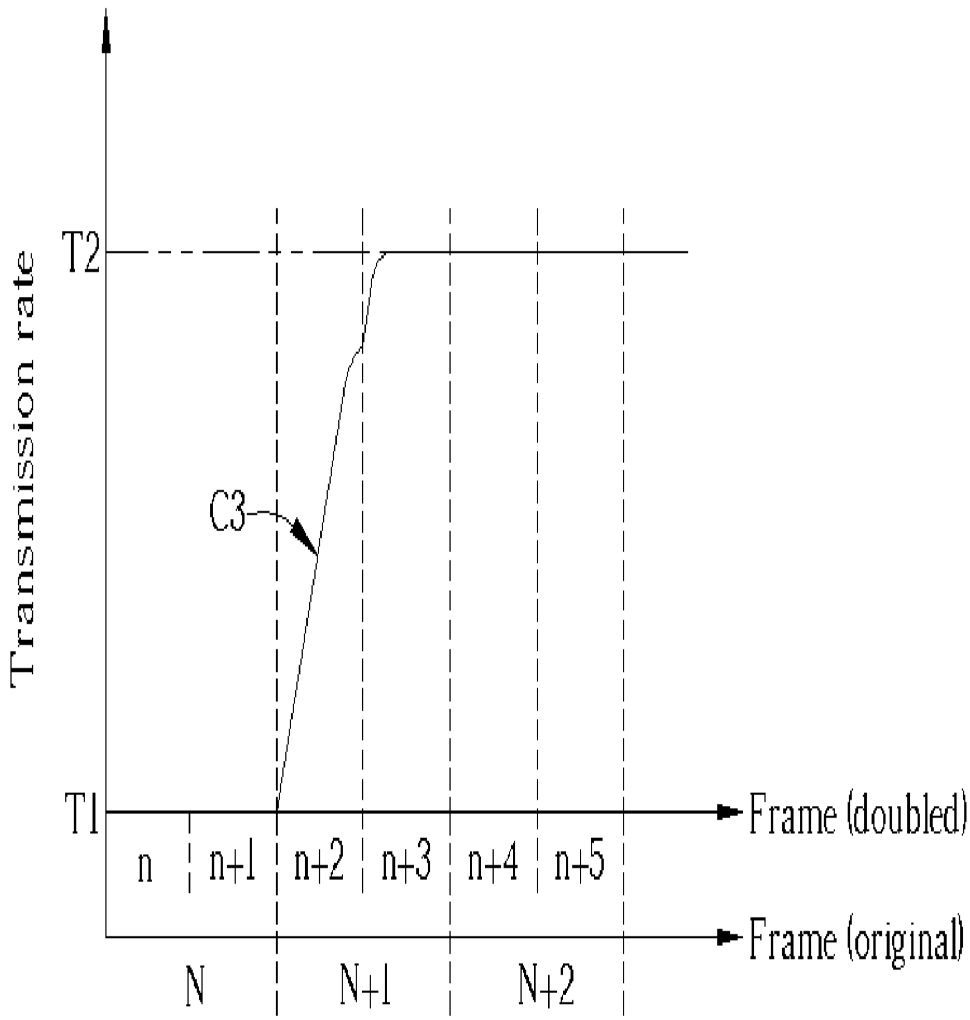

Transmission rate
T2
T1
C3
n
n+1
n+2
n+3
n+4
n+5
Frame (doubled)
Frame (original)
N
N+1
N+2

Fig. 6

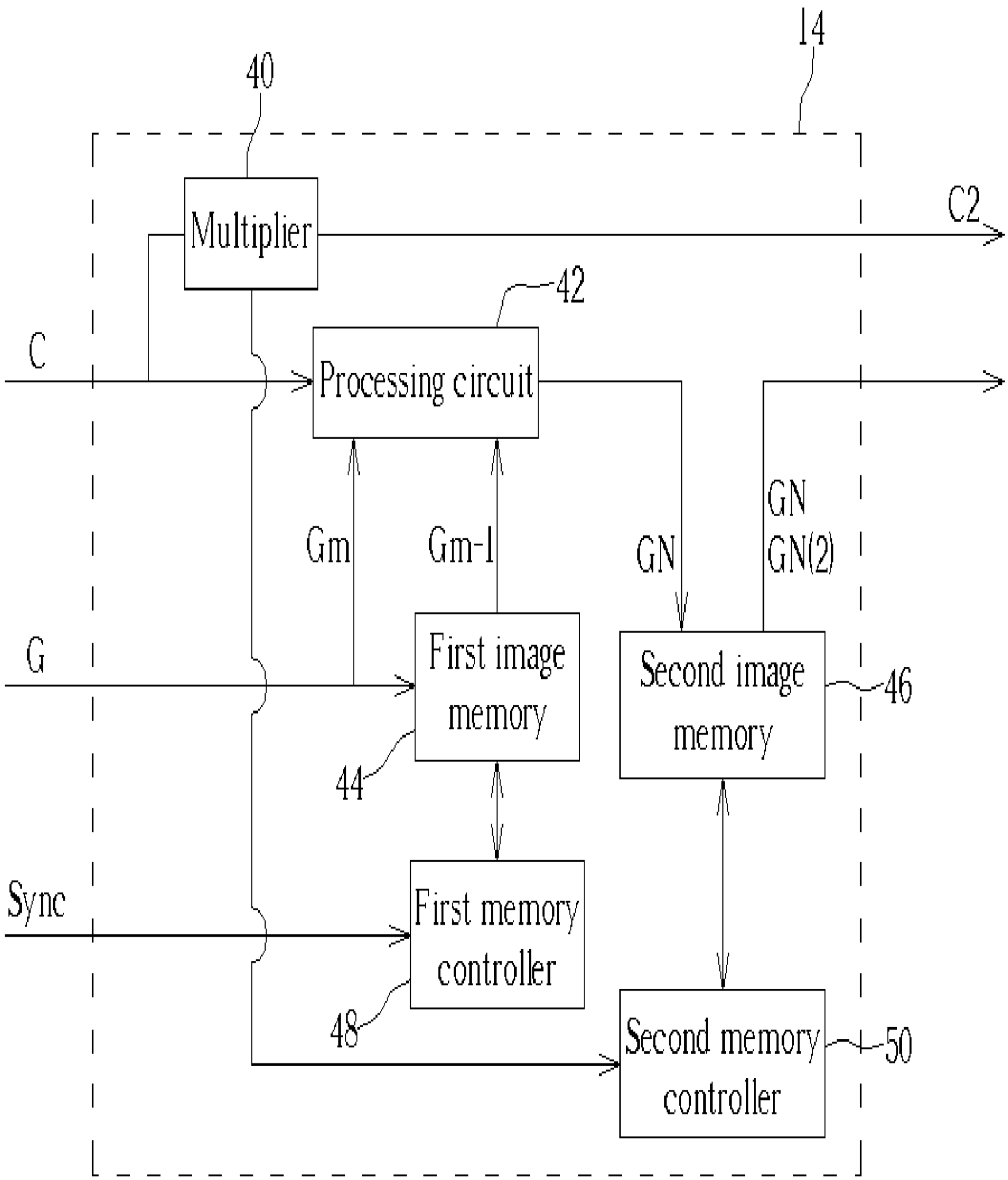

14
40
Multiplier
C2
42
C
Processing circuit
Gm
Gm-1
GN
GN
GN(2)
G
First image memory
Second image memory
46
44
Sync
First memory controller
48
Second memory controller
50

Fig. 7

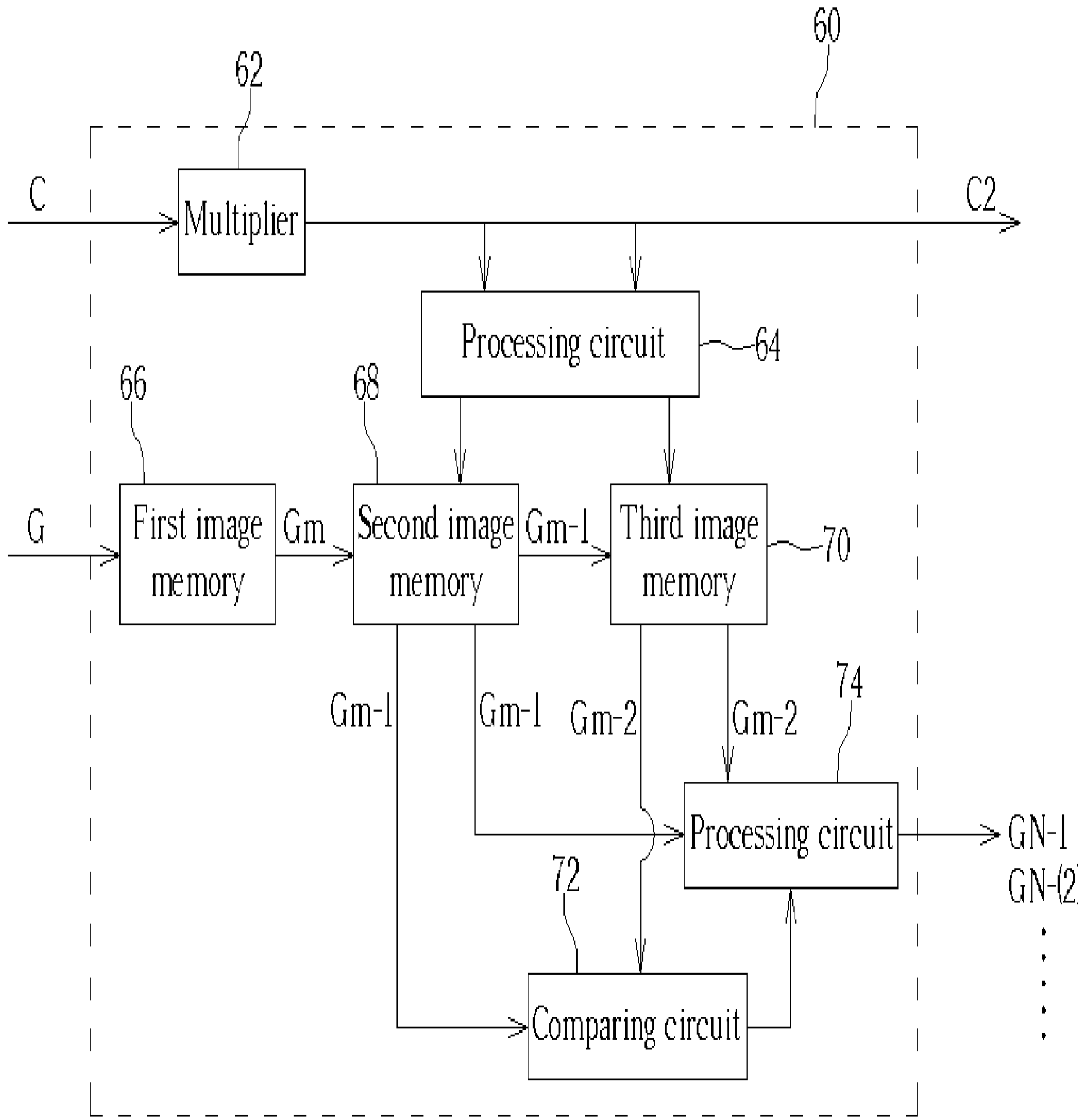
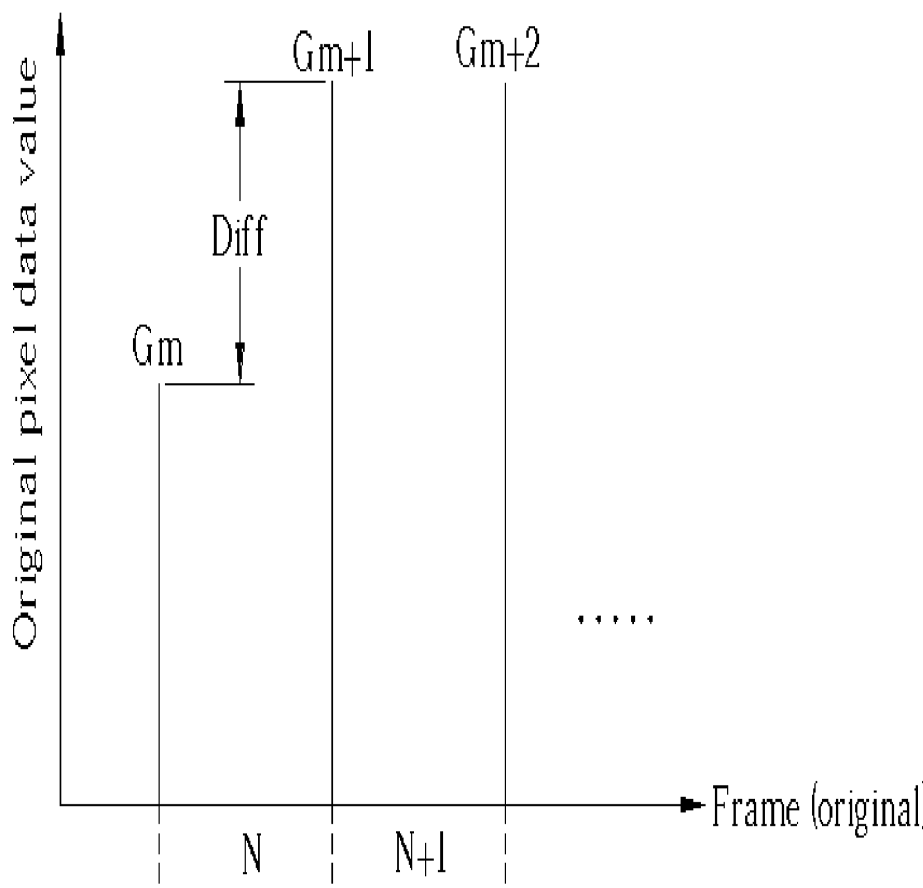
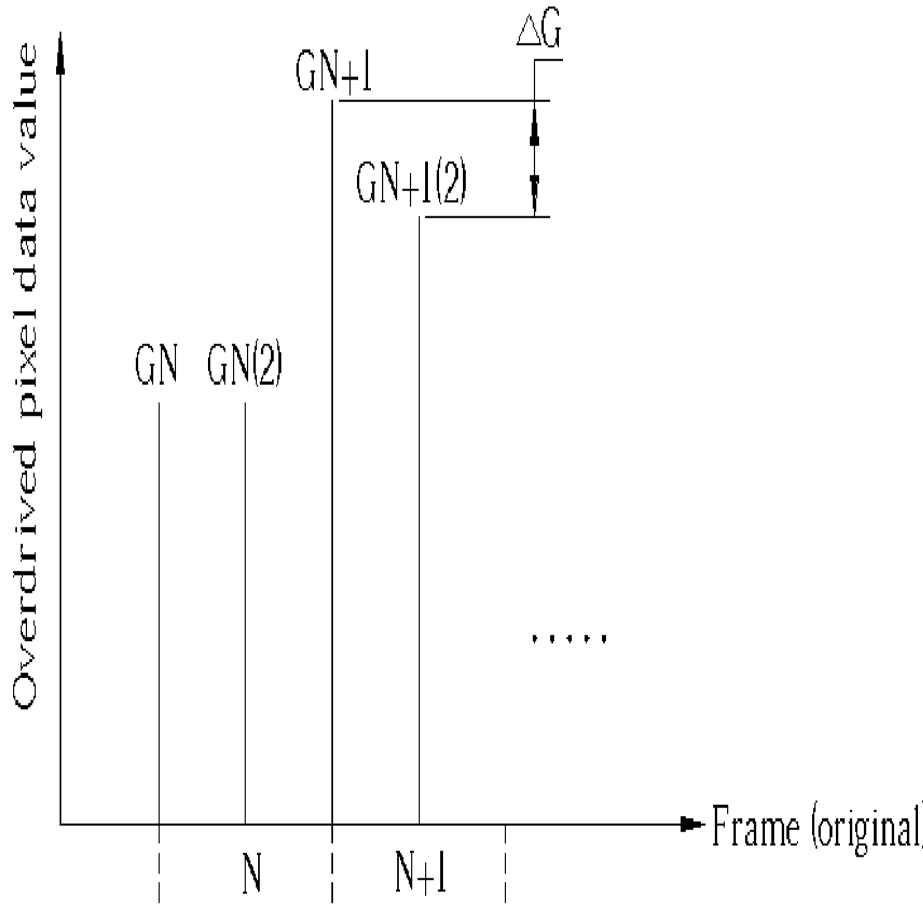

60
62
C
Multiplier
C2
Processing circuit
64
66
68
G
First image memory
Gm
Second image memory
Gm-1
Third image memory
70
Gm-1
Gm-1
Gm-2
Gm-2
74
Processing circuit
GN-1
GN-(2)
72
Comparing circuit

Fig. 8



Original pixel data value
Gm+1
Gm+2
Diff
Gm
.....
Frame (original)
N
N+1

Fig. 9



ΔG
GN+1
GN+1(2)
Overdrived pixel data value
GN
GN(2)
.....
Frame (original)
N
N+1

Fig. 10

ACKNOWLEDGEMENT RECEIPT

Electronic Version

Stylesheet Version v01

Title of Invention	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD

Submision Type : Utility Patent Filing

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First Named Applicant: Yung-Hung Shen

Attorney Docket Number: VASP0001USA

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From: us

File Listing:

Doc. Name	File Name	Size (Bytes)	Date Produced (yyyymmdd)
us-assignment	VASP0001-usassn.xml	2293	2004-01-08
us-assignment	us-assignment.xsl	8983	2004-01-08
us-assignment	us-assignment.dtd	10898	2004-01-08
us-assignment	VASP0001ASS1.tif	42484	2004-01-08
us-assignment	VASP0001ASS2.tif	31724	2004-01-08
us-request	VASP0001-usrequ.xml	3477	2004-01-08
us-request	us-request.dtd	19064	2004-01-08
us-request	us-request.xsl	33300	2004-01-08
us-fee-sheet	VASP0001-usfees.xml	2011	2004-01-08
us-fee-sheet	us-fee-sheet.xsl	24912	2004-01-08
us-fee-sheet	us-fee-sheet.dtd	11069	2004-01-08
us-declaration	VASP0001-usdecl.xml	1282	2004-01-08
us-declaration	us-declaration.dtd	3833	2004-01-08
us-declaration	us-declaration.xsl	10015	2004-01-08
us-power-of-attorney-grant	VASP0001-uspoat.xml	982	2004-01-08
us-power-of-attorney-grant	us-power-of-attorney-grant.dtd	4923	2004-01-08
us-power-of-attorney-grant	us-power-of-attorney-grant.xsl	12448	2004-01-08
us-declaration	VASP0001DEC1.tif	38466	2004-01-08
us-declaration	VASP0001DEC2.tif	32114	2004-01-08
application-body	VASP0001-trans.xml	28337	2004-01-08
application-body	us-application-body.xsl	83497	2004-01-08
application-body	application-body.dtd	49498	2004-01-08
application-body	wipo.ent	4956	2004-01-08
application-body	mathml2.dtd	54588	2004-01-08
application-body	mathml2-qname-1.mod	13225	2004-01-08
application-body	isoamsa.ent	5191	2004-01-08
application-body	isoamsb.ent	3988	2004-01-08
application-body	isoamsc.ent	1460	2004-01-08
application-body	isoamsn.ent	5620	2004-01-08
application-body	isoamso.ent	1934	2004-01-08

Doc. Name	File Name	Size (Bytes)	Date Produced (yyyymmdd)
application-body	isoamsr.ent	7073	2004-01-08
application-body	isogrk3.ent	3559	2004-01-08
application-body	isomfrk.ent	4553	2004-01-08
application-body	isomopf.ent	2571	2004-01-08
application-body	isomscr.ent	4628	2004-01-08
application-body	isotech.ent	5268	2004-01-08
application-body	isobox.ent	3568	2004-01-08
application-body	isocyr1.ent	5345	2004-01-08
application-body	isocyr2.ent	2504	2004-01-08
application-body	isodia.ent	1508	2004-01-08
application-body	isolat1.ent	5282	2004-01-08
application-body	isolat2.ent	9007	2004-01-08
application-body	isonum.ent	5913	2004-01-08
application-body	isopub.ent	6621	2004-01-08
application-body	mmlextra.ent	7901	2004-01-08
application-body	mmlalias.ent	38209	2004-01-08
application-body	soextblx.dtd	12870	2004-01-08
application-body	vasp0001usa-01.tif	3010	2004-01-08
application-body	vasp0001usa-02.tif	3494	2004-01-08
application-body	vasp0001usa-03.tif	5060	2004-01-08
application-body	vasp0001usa-04.tif	4928	2004-01-08
application-body	vasp0001usa-05.tif	5202	2004-01-08
application-body	vasp0001usa-06.tif	4128	2004-01-08
application-body	vasp0001usa-07.tif	6812	2004-01-08
application-body	vasp0001usa-08.tif	7326	2004-01-08
application-body	vasp0001usa-09.tif	2942	2004-01-08
application-body	vasp0001usa-10.tif	3314	2004-01-08
package-data	VASP0001-pkda.xml	10237	2004-01-08
package-data	package-data.dtd	27025	2004-01-08
package-data	us-package-data.xsl	19263	2004-01-08
	Total files size	775693	

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