Ernst Lueder

LIQUID CRYSTAL DISPLAYS

ADDRESSING SCHEMES AND ELECTRO-OPTICAL EFFECTS

WILEY SID Series in Display Technology

SID

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LIQUID CRYSTAL DISPLAYS

Page 2

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Liquid Crystal Materials and Liquid Crystal Cells

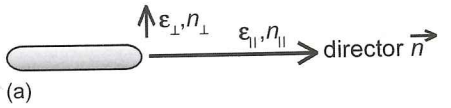
2.1 Properties of Liquid Crystals

2.1.1 Shape and phases of liquid crystals

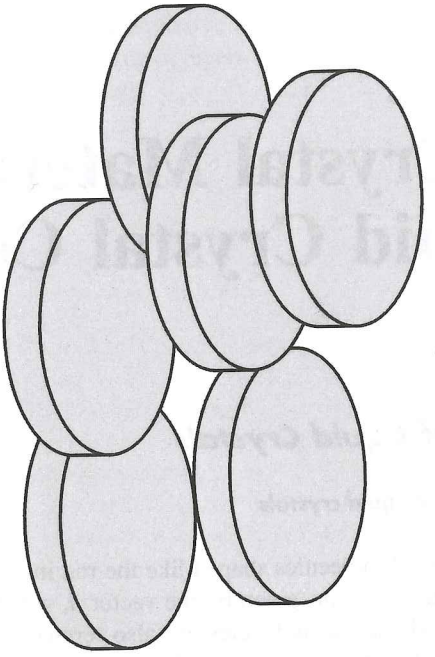
Most liquid crystals consist of molecules shaped like the rod in Figure 2.1(a). The direction of the long axis is called the *director*, given by the vector $\vec{n}$, which is an apolar vector as $\vec{n}$ and $-\vec{n}$ are equivalent. Rod-shaped molecules are also termed *calamitic*. Other shapes of molecules are disc-like or discotic, as in Figure 2.1(b), and lath-like.

We focus on calamitic (Bahadur, 1990; Demus *et al.*, 1998a,b) liquid crystals as they are the most important for applications. Below the melting point T_m they are solid, crystalline and anisotropic, whereas above the clearing point with temperature $T_c > T_m$ they are a clear isotropic liquid. In the mesophase in Figure 2.2 in between T_m and T_c, the material has the appearance of a milky liquid, but still exhibits the ordered phases shown in Figure 2.2. These phases are now described in the sequence given by increasing temperature. The first phase above T_m is the smectic C phase (smectic is derived from the Greek word for soap). As all smectic phases, it is ordered in two dimensions. The molecules are arranged with random deviations tilted to the plane of the layer. In the smectic A phase the directors of the molecules are again with random deviations perpendicular to the plane of the layer. Next to the clearing point, the nematic phase appears with only a one-dimensional order (nematic in Greek means a thread, indicating the thread-like defects in the material). All members of the mesophase are anisotropic, as is the solid phase.

Some more phases of minor importance for display applications are below the smectic C phase, the smectic B_{hex} phase (hexatic B phase), with the same layers as smectic C but a short range close packed hexagonal structure, in Figure 2.3(a) seen against the director $\vec{n}$; in this direction, the smectic C phase exhibits the irregular structure in Figure 2.3(b). The phases J, G, E, K and H are located above T_m, and are smectic-like soft crystals with a long range order.



(a)



(b)

Figure 2.1 (a) Road-like or calamitic liquid crystal molecule with director n; (b) disclike or discotic liquid crystal molecules

The smectic C^* phase (chiral smectic C phase) in Figure 2.4 possesses a layered smectic structure in which the parallel directors of the molecules are rotated from layer to layer on the surface of a cone, resulting in a helix.

If chiral compounds such as cholesterol esters are added, the nematic phase changes to the cholesteric phase in Figure 2.5, which exhibits a helical structure in which, again, the director is rotated from layer to layer.

An as yet poorly understood peculiarity are the blue phases which occur in a small temperature range between the cholesteric and solid anisotropic phase.

More than 20 000 calamitic compounds are known.

Liquid crystals, the phases of which change with temperature, are called *thermotropic*. Those which change with the concentration of solvents and temperature are *lyotropic*. Calamitic and thermotropic liquid crystals are important for LCDs. Their nematic phase is the basis for both the most widely used Twisted Nematic (TN) cell with active matrix addressing, and for the SuperTwist Nematic (STN) cell with passive matrix addressing. Further LCDs based on calamitic and thermotropic nematic phases are Polymer Dispersed

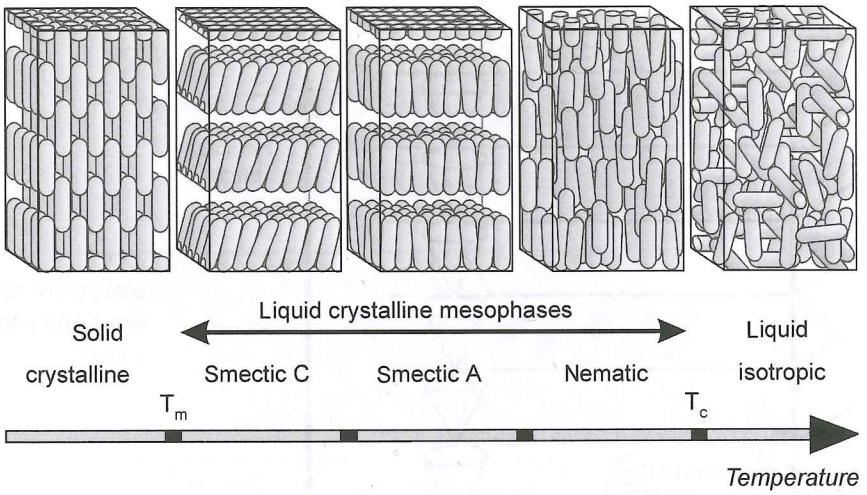


Figure 2.2 Phases of LC materials versus temperature

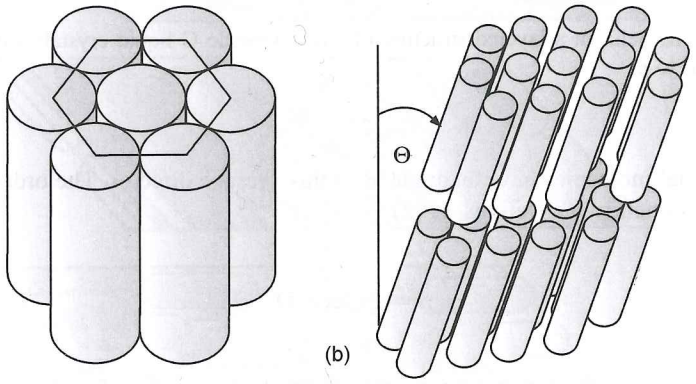


Figure 2.3 Top view of (a) the close packed hexagonal structure of the smectic B_{hex} phase, and (b) of the smectic C phase

Liquid Crystals (PDLC) and guest-host-LCDs. The smectic A and smectic C* phases provide bistable ferro-electric LCDs with passive matrix addressing. The cholesteric phase gave rise to the Stabilized Cholesteric Texture (SCT) with bistability at zero field. LCDs based on these phases will be discussed later.

To better understand electro-optical effects and electronic addressing, some materials properties have to be presented (Bahadur, 1990; Demus *et al.*, 1998a,b).

2.1.2 *Material properties of anisotropic liquid crystals*

The rod-like molecules have a head and a tail, which is, however, not taken into account by the direction of $\vec{n}$. Molecules in an unordered alignment exhibit an average director.

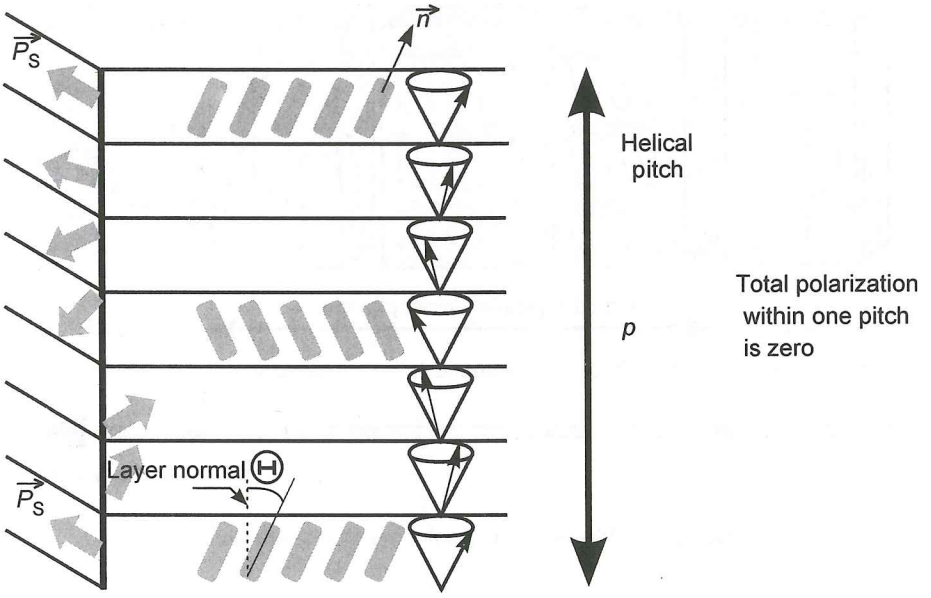


Figure 2.4 The helix in a layered structure of chiral smectic C liquid crystals with polarization $\vec{P}_s$ perpendicular to $\vec{n}$

The individual molecules have an angle Θ to this average director. The order parameter S of a phase is defined by (Tsvetkov, 1942)

$$S = \frac{1}{2}\langle 3\cos^2\Theta - 1\rangle, \tag{2.1}$$

where the bracket indicates that the average over a large number of molecules with angles Θ is taken. In a perfectly ordered state, $\Theta = 0$, and hence $S = 1$. A completely unordered phase has $S = 0$. In typical nematic phases, S lies in the region of 0.4 to 0.7, indicating that the molecules are rather disordered.

The energy needed for a phase transition, e.g., from smectic A to smectic C, is characterized by a transition enthalpy in kJ/mol. Extensive investigations of phase transitions have revealed the temperature dependance of physical parameters such as the helical pitch, the viscosity or the elastic coefficients.

Due to the ordered structure, all phases between T_m and T_c are anisotropic, meaning that all dielectric, optical and mechanical properties depend upon the direction.

The dielectric constant is $\varepsilon = \varepsilon_r \varepsilon_0$, where $\varepsilon_0 = 8.854 \cdot 10^{-14}$ F/m stands for the permittivity in vacuum and ε_r for the relative dielectric constant. This means, as shown in Figure 2.1, $\varepsilon_r = \varepsilon_\parallel$ in the direction parallel to the director and $\varepsilon_r = \varepsilon_\perp$ perpendicular to the director, leading to the dielectric anisotropy

$$\Delta\varepsilon = \varepsilon_\parallel - \varepsilon_\perp. \tag{2.2}$$

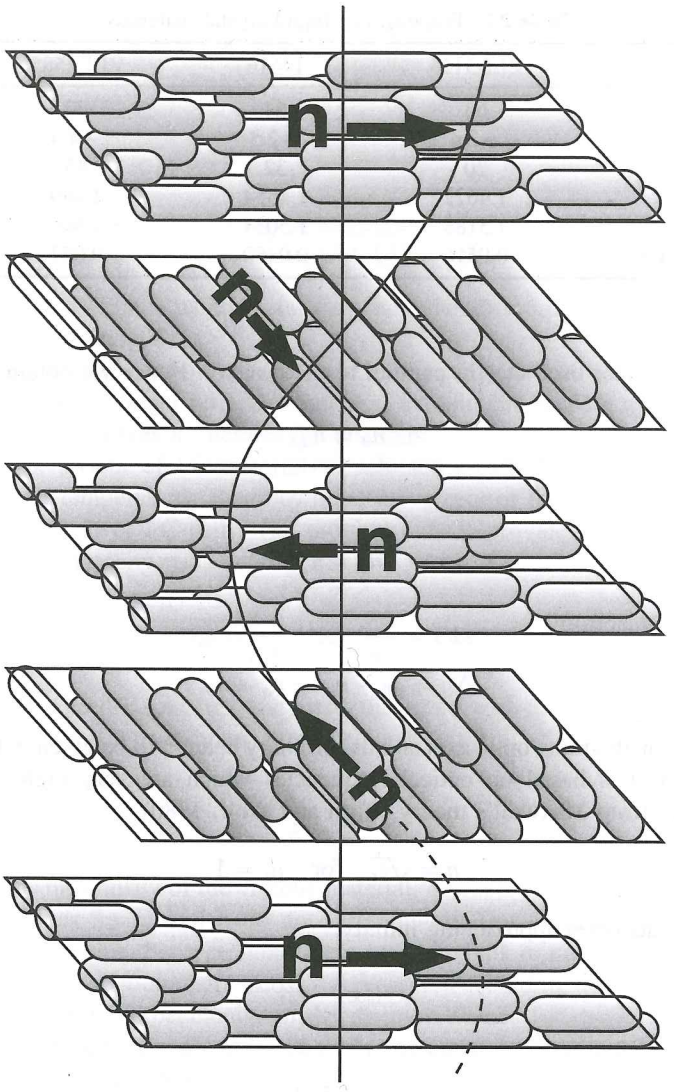


Figure 2.5 Helix of the cholesteric phase

Materials with $\Delta\varepsilon > 0$ are called p-type; their molecules align with the director parallel to the electric field, whereas in n-type materials with $\Delta\varepsilon < 0$, they align perpendicular to the field. This holds independent of the direction of the field vector. Values for $\Delta\varepsilon$ are found in the range from -0.8 to -6 and from 2 to 20. The addition of cyanogroups enlarges $\Delta\varepsilon$, whereas fluorine atoms in materials with $\Delta\varepsilon < 0$ lower $\Delta\varepsilon$ even further. Values for four materials are listed in Table 2.1.

The optical anisotropy Δn concerns the refractive indices n_0 for the ordinary beam of light, where the vector of the electrical field oscillates perpendicular to the optical axis that is perpendicular to the director and the refractive index n_e for the extraordinary beam of light,

Table 2.1 Properties of liquid crystal materials

	ZLI-3125	14616	ZLI-2585	14627
T_C[°C]	63	54	70	48
$\Delta\varepsilon$ (1kHz, 20°C)	+2.4	+2.3	−4.4	−3.5
η [mm^2/s] (20°C)	20	32	45	45
$n_0 = n_\perp$	1.4672	1.4554	1.469	1.4551
$n_e = n_\parallel$	1.5188	1.5034	1.506	1.4893
Δn (589 nm, 20°C)	0.0516	0.0480	0.037	0.0342

where the field vector oscillates in parallel to the director. Hence we obtain

$$n_0 = n_\perp, \tag{2.3}$$

and

$$n_e = n_\parallel, \tag{2.4}$$

and the optical anisotropy

$$\Delta n = n_\parallel - n_\perp = n_e - n_0. \tag{2.5}$$

More explanation about the optic axis and the ordinary beam will be given in Chapter 6. The refractive index n is based on optical frequencies which are very high. Therefore, the equation known from Maxwell's theory (Born and Wolf, 1980)

$$n = \sqrt{\varepsilon_r} \quad \text{for} \quad \mu_r = 1 \tag{2.6}$$

provides for frequencies approaching infinity:

$$\varepsilon_{r\parallel\infty} = n_\parallel^2, \tag{2.7}$$

$$\varepsilon_{r\perp\infty} = n_\perp^2 \tag{2.8}$$

and

$$\Delta\varepsilon_{r\infty} = n_\parallel^2 - n_\perp^2. \tag{2.9}$$

The refractive indices depend upon the wavelength λ. Values for Δn lie in the range $\Delta n \in [0.04, 0.45]$; some values are listed in Table 2.1. As a rule, materials with a high Δn are not stable to UV light. Due to the optical anisotropy, the material is birefringent. The speed of light is (Born and Wolf, 1980)

$$v = \frac{c}{\sqrt{n(\lambda)}}, \tag{2.10}$$

where c is the speed of light in vacuum. The speeds of light

$$v_{\parallel} = \frac{c}{\sqrt{n_{\parallel}(\lambda)}}, \tag{2.11}$$

and

$$v_{\perp} = \frac{c}{\sqrt{n_{\perp}(\lambda)}}, \tag{2.12}$$

where the E-vector oscillates parallel and perpendicular to the director, are different and dependent on the wavelength.

This is the key for the electro-optical effects in liquid crystal cells.

The direction with the larger refraction index $n_{\parallel}$ exhibits the smaller speed, and hence is called the slow axis, whereas $n_{\perp}$ defines the fast axis.

The dynamic behaviour of LC materials is affected greatly by the viscosity. Too high viscosities at lower temperatures slow down the movement of the molecules and yield the lower temperature limit of LC cells. The proximity to T_c provides the upper temperature limit. The dynamic viscosity η_d is defined as

$$\eta_d = \frac{F}{A}\frac{d}{v} \quad \text{in} \quad \frac{Ns}{m^2} = \text{Pa s}, \tag{2.13}$$

where F is the force needed to shift a body with the area A with the velocity v over a viscous layer with a thickness d. For displays, the kinematic viscosity

$$\eta = \frac{\eta_d}{\delta} \quad \text{in} \quad \frac{mm^2}{s} \tag{2.14}$$

is used, where δ is the density of the viscous material. As for most LC materials, δ is around $1Ns^2/mm^4$; the values for η_d and η do not differ much. The viscosity depends upon the orientation of the directors. For a random orientation, the bulk or turbid kinematic viscosity is given in Table 2.1. The rotational viscosity is measured according to Figure 2.6, where the vector of the rotation is perpendicular to the director. Values for dynamic rotational viscosities of LCs are 0.02 Pa s to about 0.5 Pa s. This viscosity is important for the movement of the director in an electric field.

The elastic constants belong to restoring torques if the field of directors is deformed. The three deformations from the equilibrium are splay, twist and bend, with the elastic constants K_{11}, K_{22} and K_{33}, as shown in Figure 2.7. The dimension is a force. The values are very small in the range of $10 \cdot 10^{-2} N$. These elastic forces determine the equilibrium in the presence of electric and magnetic fields.

A large variety of chemical compounds exhibit the properties of liquid crystals. The basic structure with rings, linking groups and terminal groups is shown in Figure 2.8. Rings can be cyclohexyl, pyridine, dioxane, phenylcyclohexane or phenyldioxane. Fluorinated compounds have a high specific resistance $\rho = 5 \cdot 10^{15}\ \Omega$ cm. The characteristic temperatures of LC compounds can be shifted by additive ingredients. By this means, Merck's nematic compounds reached the wide temperature range of operation, from $-40°C$ to $120°C$, which is very suitable for automotive application. In Table 2.2 properties of LC materials with this wide temperature range are listed.

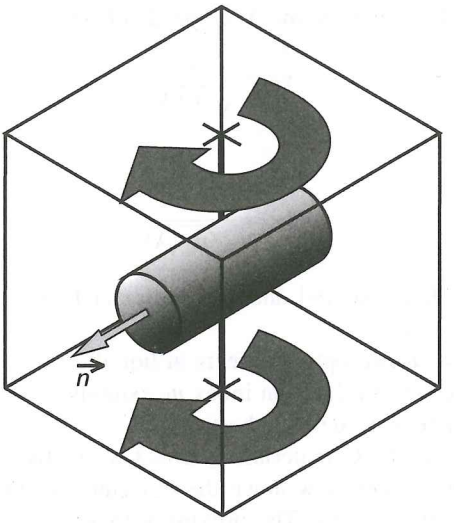


Figure 2.6 The rotational viscosity for rotation of a molecule perpendicular to the director

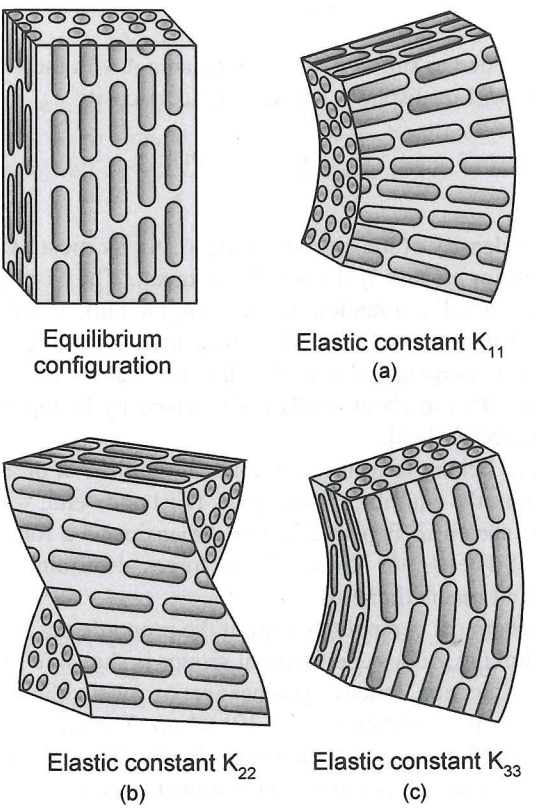


Figure 2.7 Equilibrium configuration; the elastic deformations splay (a), twist (b) and bend (c)

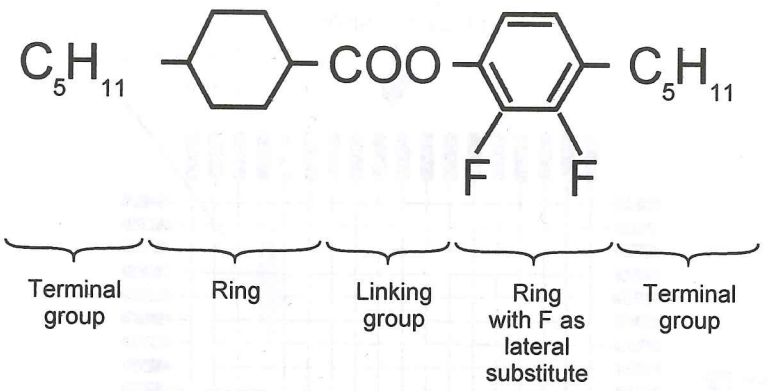


Figure 2.8 The basic structure of a calamitic LC molecule

Table 2.2 Properties of nematic LC materials with a wide temperature range

	MLC-1380000	MLC-13800100	MLC-1390000	MLC-13900100
Transition temp. smectic-nematic	$< -40°C$	$< -40°C$	$< -40°C$	$< -40°C$
Clearing pt T_c	110°C	111°C	110.5°C	110.5°C
Rotational viscosity, 20°C	228 mPas	151 mPas	235 mPas	167 mPas
$\Delta\varepsilon$ 1 kHz, 20°C	+8.9	+5.0	+8.3	+5.2
$n_0 = n_\perp$	1.4720	1.4832	1.4816	1.4906
$n_e = n_\parallel$	1.5622	1.5735	1.5888	1.5987
Δn	+0.0902	+0.0903	+0.1073	+0.1081

2.2 The Operation of a Twisted Nematic LCD

The liquid crystals used are calamitic and thermotropic in the nematic phase. The operation of this most widely applied LCD will be phenomenologically described in order to give an overview over the entire flat panel display system, including the addressing scheme (Demus *et al.*, 1998a; Kaneko, 1987; Lueder, 1998a). This alleviates the more analytical and detailed treatments which follow.

2.2.1 The electro-optical effects in transmissive twisted nematic LC-cells

Figure 2.9 depicts the top view of a display panel with the conducting rows and columns terminating in the contact pads. The rectangular pixels can only be electrically addressed from those contact pads.

A colour VGA display, as used in laptops, has 480 rows and 3×320 columns forming triple dots for the three colours red, green and blue. An NTSC TV display has 484 rows and 3×450 columns corresponding to 653 400 pixels, whereas an HDTV display has

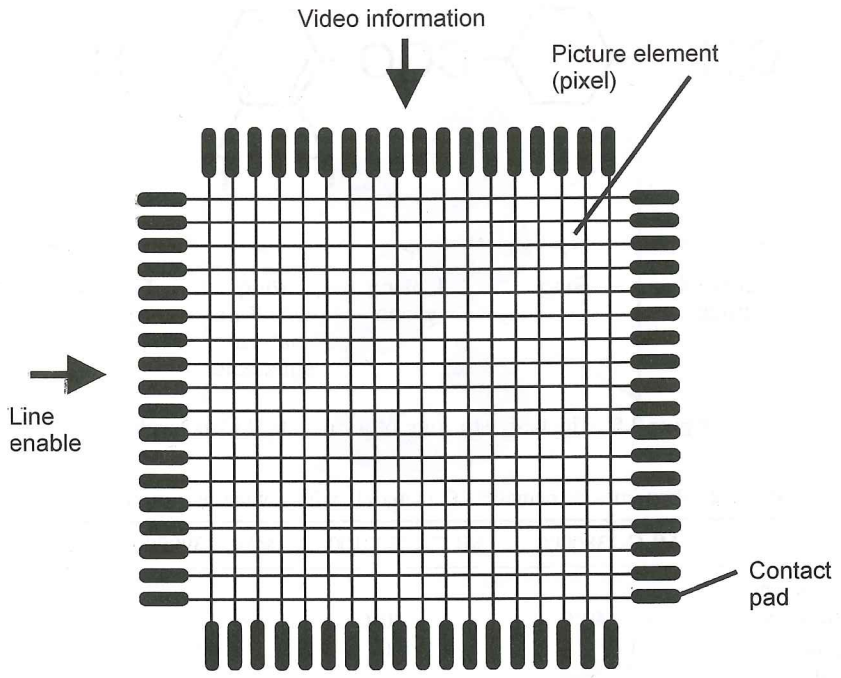


Figure 2.9 Top view of the rows, columns, pixels and contact pads of a display panel

$1080 \cdot 3 \cdot 1920 = 7\,320\,800$ pixels. For more standardized formats, see the table in Appendix 1.

Figure 2.10 shows a pixel of a transmissive twisted nematic LC-cell with no voltage applied. The white back light *f* passes the polarizer *a*. The light leaves it linearly polarized in the direction of the lines in the polarizer, and passes the glass substrate *b*, the transparent electrode *c* out of Indium-Tin-Oxide (ITO) and the transparent orientation layer *g*. This layer, made of an organic material such as polyimide, 100 nm thick, is rubbed to generate grooves in the direction of the plane of the polarized light. In these grooves the rod-like LC molecules are all anchored in parallel, but, as shown in Figure 2.11, with a pretilt angle α_0 to the surface of the orientation layer. The sequence of layers is the same on the second glass plate. A typical thickness of the cell in Figure 2.10 is $d = 3.5\,\mu$ to $4.5\,\mu$. The grooves on the second plate are perpendicular to those on the first plate. This forces the liquid crystal molecules to twist on a helix by $\beta = 90°$ from one plate to the other without the addition of chiral compounds. All twist angles are called β.

Due to the birefringence, the components of the electric field vector of the light in parallel and perpendicular to the directors travel with different speeds, which depend up-on the wavelength. They superimpose along their path between the two glass plates first to elliptically polarized light, in the distance $d/2$ from the input to circularly polarized light, then again to an elliptic polarization, and if

$$d = \frac{\sqrt{3}}{2} \frac{\lambda}{\Delta n} \tag{2.15}$$

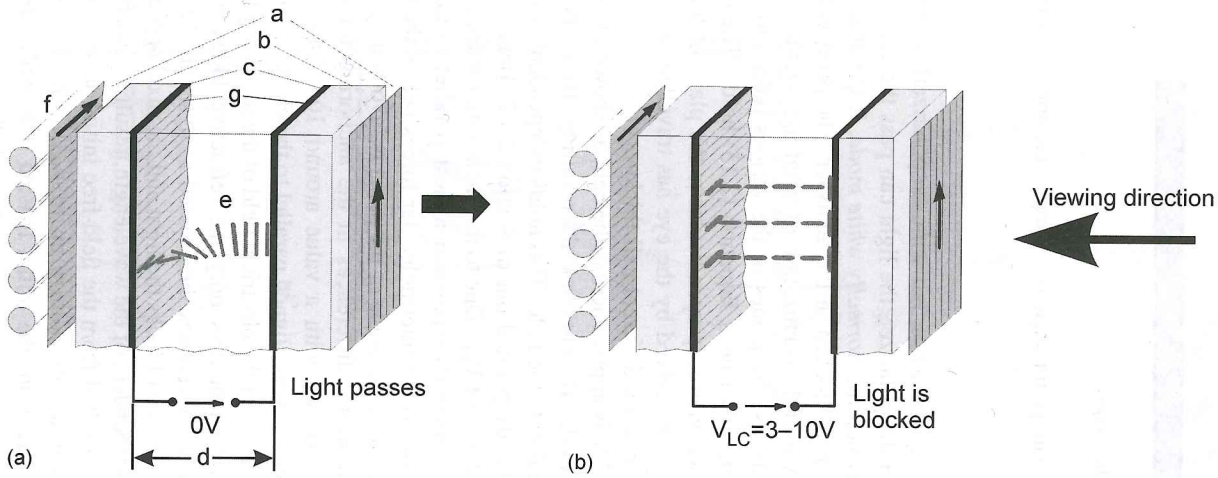


Figure 2.10 The structure of a TN-LCD (a) while light is passing, and (b) while light is blocked. a: polarizer; b: glass substrate; c: transparent electrode; g: orientation layer; e: liquid crystal; f: illumination

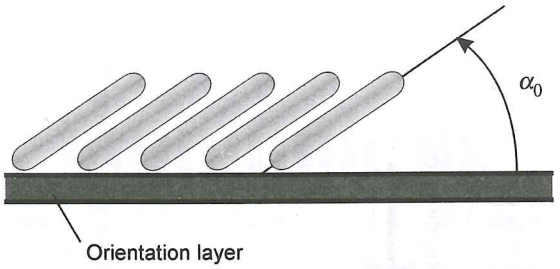


Figure 2.11 LC molecules with pretilt angle α_0 on top of the orientation layer

they reach the analyser again linearly polarized, but with the polarization plane rotated by 90°. If the analyser is crossed with the polarizer, the light can pass the analyser. The pixel appears white. This operation is termed the *normally white mode*. If the analyser is rotated by 90°, a parallel analyser, the light is blocked in the analyser. The pixel is black. This is called the *normally black mode*. A useful visualization of what happens to the light while travelling through the cell is as follows: the planes of the various polarizations follow the twist of the helix. This is, however, only true if Equation (2.15) holds. The explanation is also only true for light travelling and viewed perpendicular to the plane of the substrate. If viewed under a different angle, light perceived by the eye has travelled in a different path with different angles to the director and a different cell thickness d.

If a voltage V_{LC} of the order of 2 V is applied across the cell, as shown in Figure 2.10(b), using the two transparent ITO-electrodes 100 nm thick, the resulting electric field attempts to align the molecules for $\Delta\varepsilon > 0$ parallel to the field. This holds independent of the sign of the vector of the electrical field, as already pointed out in Section 2.1.2. Hence, the following effects are not dependent on the polarity of V_{LC}. Due to the anchoring forces, a thin LC layer on top of the orientation layers maintains its position almost parallel to the surfaces. A threshold voltage V_{th} is needed to overcome intermolecular forces before the twisted molecules start to rotate. A uniform start over the plane of the panel is favoured by a pretilt angle around 3°, which seems to avoid strong differences in the anchoring forces. Only at a saturation voltage V_{max} several times V_{th} with a value around 10 V have all molecules besides those on top of the orientation layers aligned parallel to the electric field, as depicted in Figure 2.10(b). In this state the vector of the electrical field of the incoming light oscillates perpendicular to the directors, and encounters only the refractive index $n_\perp$. Hence, no bi-refringence takes place and the wave reaches the crossed analyser in the same linearly polarized form as at the input. The analyser blocks the light and the pixel appears black. This is an excellent black state as it is independent of the wavelength, resulting in a blocking of the light. This black state is gradually reached from the field-free initial state by increasing the voltage V_{LC} from OV over an intermediate voltage up to V_{max}, which is also gradually rotating the molecules in Figure 2.12 from the initial twisted state with directors parallel to the surfaces (Figure 2.10(a)) over an intermediate state with the director already tilted down with tilt angle α (Figure 2.12(b)) to the final state with directors parallel ($\alpha = 90°$) to the electric field. The transmitted luminance, also termed *transmittance*, of the light is shown in Figure 2.13 for the normally white mode discussed so far. In the normally black mode, the analyser is parallel to the polarizer and allows the light to pass at the voltage

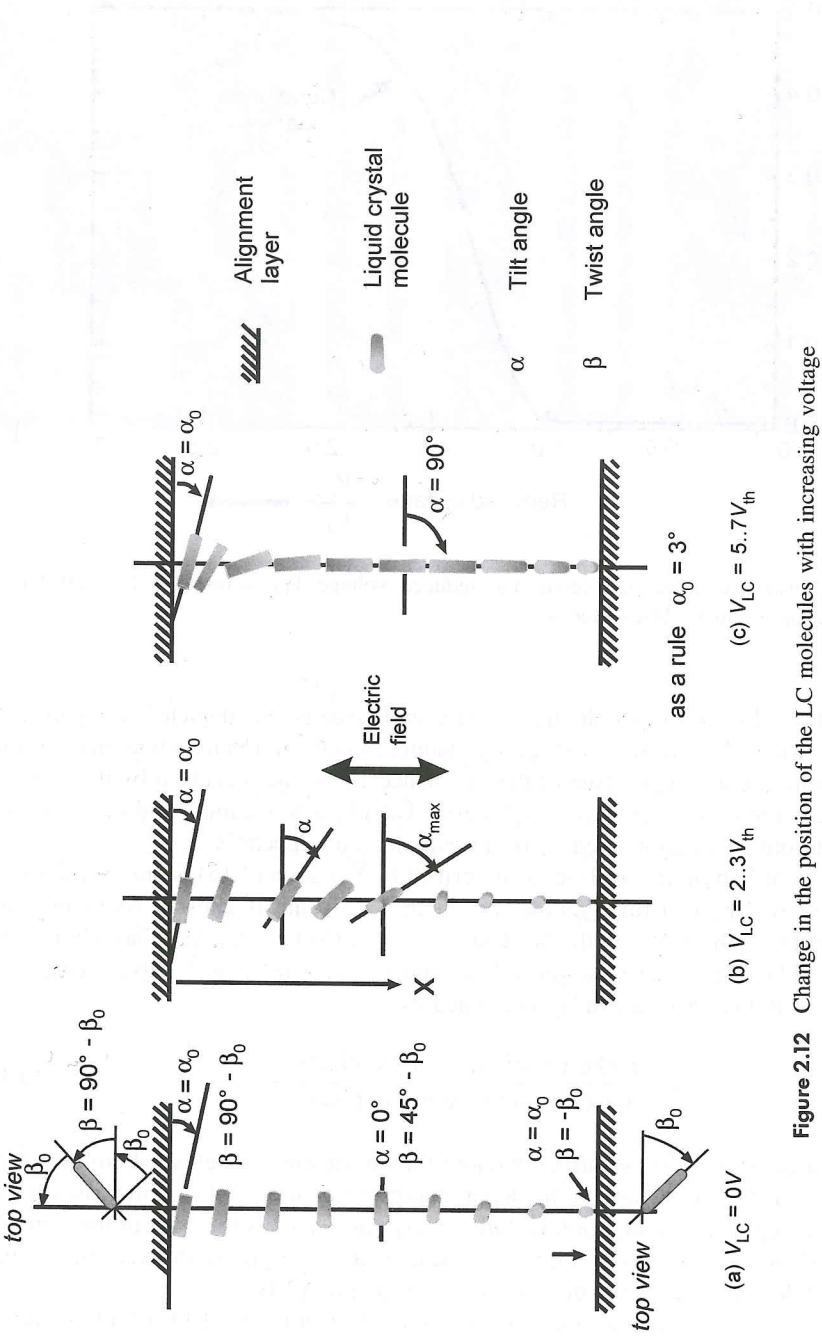


Figure 2.12 Change in the position of the LC molecules with increasing voltage

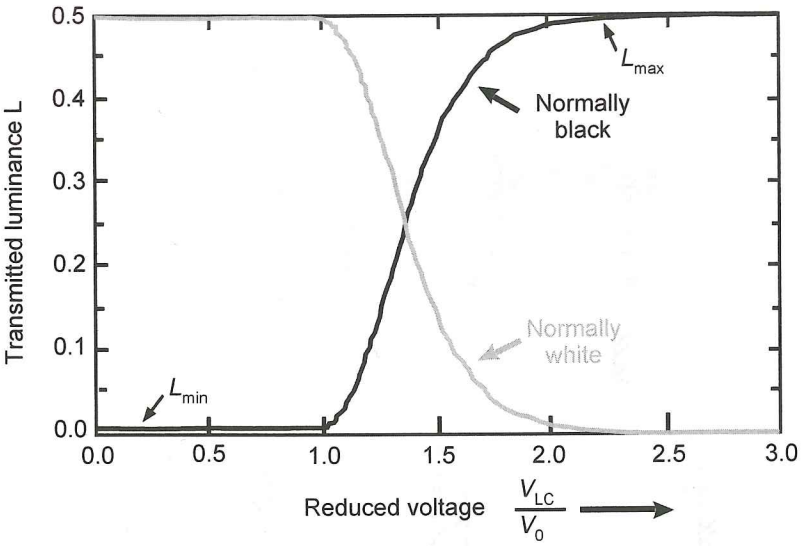


Figure 2.13 Transmitted luminance versus the reduced voltage V_{LC} across the LC cell for the normally white and normally black modes

$V_{th} \leq V_{LC} \leq V_{max}$. For this mode the transmitted luminance is also depicted in Figure 2.13. Only in this mode is the threshold voltage V_{th} visible, as in the normally white mode a small change in luminance at a high value of the luminance cannot be perceived by the eye.

Luminance is the correct term for 'brightness'. The physical meaning and dimensions of luminance and other display-related units are explained in Appendix 2.

The blocking of light in the analyser as described by Equation (2.15) is only valid for one wavelength for which, as a rule, yellow light with $\lambda = 505\,\text{nm}$ is chosen. As other wavelengths can still pass the analyser, the black state is not perfect. As a rule, it has a bluish tint. The imperfect black state can be improved by compensation foils, as discussed later.

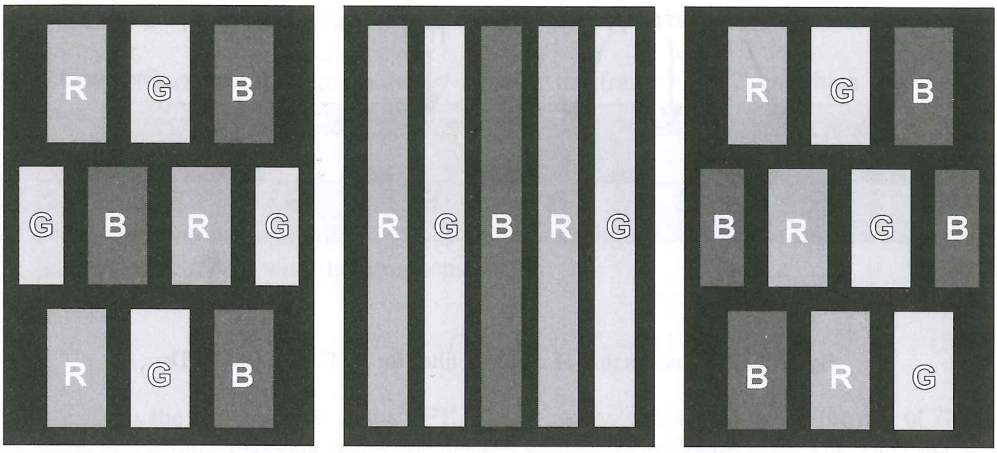
The Contrast Ratio CR of a display is defined by

$$CR = \frac{\text{highest luminance in the pixels}, L_{max}}{\text{lowest luminance in the pixels}, L_{min}}. \tag{2.16}$$

The measurement should be performed without the interference of reflected ambient light, i.e. in darkness. If the black state in the denominator of Equation (2.16) is increased by the imperfect blocking of the light, contrast falls in any case. This is the case in the normally black state, whereas the normally white state described above yields an excellent contrast due to a much lower value of the denominator in Equation (2.16).

Grey shades of a pixel are controlled by the voltage V_{LC} in Figure 2.13, which modulates the luminance from a full but imperfect black up to a full white. Luminance differs when the display is viewed under angles different from perpendicular to the glass plates. Contrast decreases the more oblique the angles become.

The TFT addressing circuit will be placed on the glass next to the backlight in Figure 2.10. In a colour display, the glass plate facing the viewer carries the pixellized colour filter,



(a) (b) (c)

Figure 2.14 The geometrical arrangement of colour pixels for red R, green G, and blue B (a) in triangles, (b) in stripes and (c) in diagonal form

shown in Figure 2.14. The pixels for red, green and blue are covered with a compound which absorbs all wavelengths originating from the white backlight besides red, green and blue, respectively. The saturation of the colours is individually controlled for each pixel by the voltage V_{LC} in the same way as for grey shades.

The geometrical arrangement of the colour pixels in triangles in Figure 2.14(a) and along diagonals in Figure 2.14(c) are recommended for moving TV pictures, whereas the colour stripes in Figure 2.14(b) are preferred for computer displays often presenting rectangular graphs.

The cross-section of a colour filter in Figure 2.15 contains the colour materials for R, G and B, an absorptive layer with a low reflection in between the pixels, a so-called black matrix, an overcoat layer and, in the case of TFT addressing, an unpixellized ITO electrode over the entire display area. For other addressing schemes, the ITO layer is no longer unstructured. The ITO electrode on the TFT-carrying plate is pixellized. The black matrix prevents light between the pixels, which is neither controlled by the voltage V_{LC} at the ITO electrodes nor exhibits the desired colour, from seeping through the cell. This light would lighten up the black state, and would thus degrade contrast and the saturation of colour. A suitable material for a black matrix is an organic material with carbon particles exhibiting a reflectivity of only 4 percent, whereas the previously used Cr-oxide has a reflectivity of 40 percent. The overcoat layer (e.g. out of a methacrylate resin solution) equalizes the different heights of the colour pixels and protects them.

2.2.2 *The addressing of LCDs by TFTs*

So far we know that we have to control the grey shade individually in each pixel by applying the appropriate pixel voltage V_{LC}, but by only using the external contact pads in Figure 2.9.

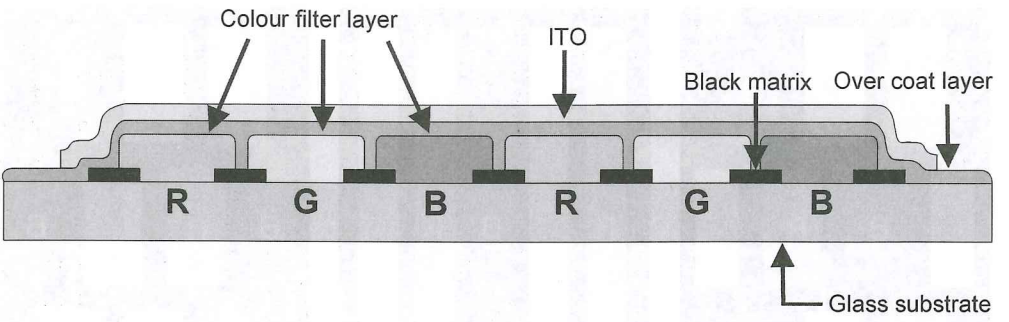


Figure 2.15 Cross-section of a colour filter for TFT addressed LCDs

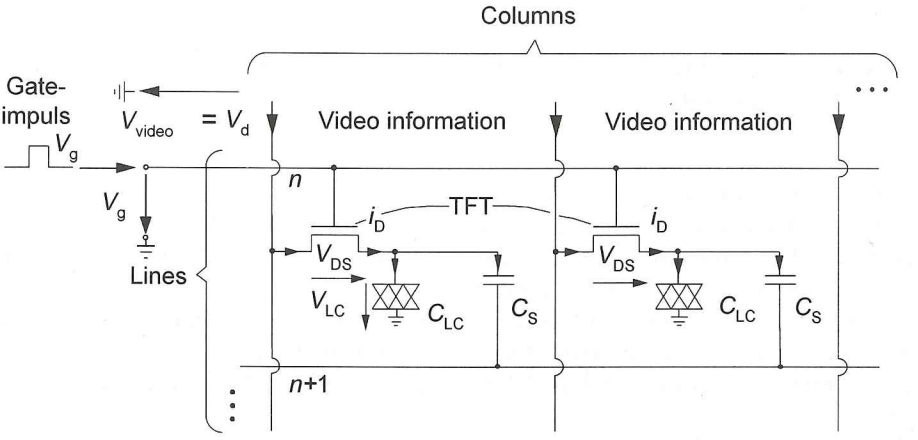


Figure 2.16 TFT addressing of the pixels in a row

The TFT-addressed LCD, usually called an Active Matrix LCD (AMLCD), solves this task as depicted in Figure 2.16. It shows two pixels of a row of pixels, with the row- and column-conductors and ground represented by the unstructured ITO electrode on the colour plate in Figure 2.15. The TFTs are *n*-channel Field Effect Transistors (FETs) fabricated with thin film technology. They operate as switches in the pixels. All TFTs in a row are rendered conductive by a positive gate impulse V_g. TFTs in other rows are blocked by grounding the rows. The video information is fed in through the columns and the conducting TFTs into all the pixels of a row simultaneously. More specifically, the video voltage V_d corresponding to a desired grey shade charges the LC-capacitor C_{LC} and an additional thin-film storage capacitor C_s up to the voltage V_d. This constitutes an amplitude modulation. The operation addresses one line at a time, as opposed to one pixel at a time, of the e-beam in CRTs. During the charging time, the storage capacitor connected to the succeeding line $n+1$ is grounded, and hence connected in parallel to C_{LC}. As this is no more true during other

phases of the operation, degradations of the addressing waveform are introduced, as discussed later.

The pixel switches have to charge N rows in the frame time T_f in which a picture is written. Hence, the row-address time is

$$T_r = T_f/N. \tag{2.17}$$

The waveform of the pixel-voltage V_{LC} is depicted in Figure 2.17. In the time T_r, the storage capacitors are charged with the time constant

$$T_{on} = (C_{LC} + C_s)R_{on} \leq 0.1T_r = 0.1\frac{T_f}{N}, \tag{2.18}$$

where R_{on} is the on-resistance of the TFT. The inequality guarantees that at the end of T_r, the voltage V_{LC} is only 1 percent below the desired voltage V_d in Figure 2.16. The TFTs need to be fast enough to make sure that even if their properties fluctuate, as indicated by dashed lines in Figure 2.17, they still charge the capacitors to the voltage V_d. After the time T_r, the transistor is blocked, but still has a finite off-resistance R_{off}. After T_f the row is addressed again and, the new picture information is fed in. During this time, the discharge of the capacitors should be small to provide a luminance as constant as possible. This yields an almost flicker-free picture, again as opposed to the CRT, where in the absence of storage the luminance of the phosphor decays after having shortly been hit by the e-beam. The constraint for the time constant T_{off} of the discharge is

$$T_{off} = (C_{LC} + C_s)R_{off} \geq 200\,T_f, \tag{2.19}$$

which ensures a voltage drop of only 1 percent at T_f. From Equations (2.18) and (2.19), we obtain

$$\frac{R_{off}}{R_{on}} = \frac{I_{on}}{I_{off}} \geq 2000\,N. \tag{2.20}$$

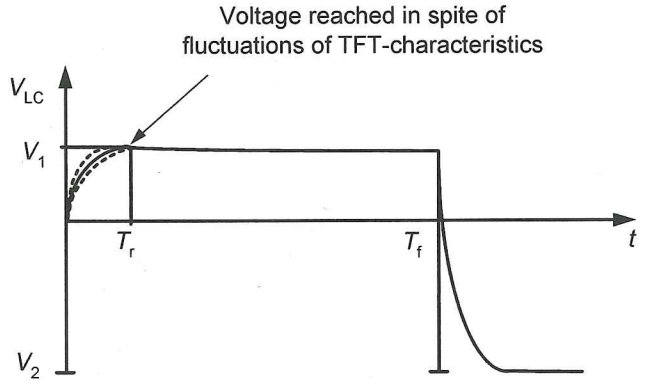


Figure 2.17 Waveform of the voltage across a pixel during charging and discharge of the storage capacitor

For an NTSC display with $N=484$, we require $R_{off}/R_{on} \geq 968 \cdot 10^3$. With the practically achievable value for the off-current $I_{off}=1$ pA, the value for the on-current $I_{on} \geq 1$ μA meets the constraint in inequality (2.20).

The voltage across the pixels has to be free of dc in order to avoid dissociation of the ingredients in the LC material. Therefore, the voltage V_{LC} applied in the next frame time has the alternate sign as indicated in Figure 2.17. As we have observed in Section 2.2.1, the operation of the TN cell is independent of the sign of the electrical field vector. The alteration in sign from frame to frame is mandatory for a sufficient life of the LC cell. The transmitted luminance of an LC cell in Figure 2.13 exhibits a linear dependence on V_{LC} in a range of about 3 V. For 256 grey shades, this results in steps of 11.7 mV/grey shade. Special care will be taken to ensure the accuracy of these steps, as the voltages are altered by parasitic capacitive couplings. Remedies against this damage will be the alternating signs of V_{LC} from row to row, column to columns, frame to frame, and combinations of these measures.

TFT-addressed LCDs offer an appealing picture quality, mainly due to the absence of flicker. TFTs are fabricated together with the storage capacitors, ITO electrodes and conductors in thin film technology on glass or plastics as substrates. Glass substrates used to be 1.2 mm thick, and are presently down to 0.7 mm, whereas plastic materials excel in a thickness of only 100 μ to 200 μ. As monocrystalline layers are unfeasible in thin film technology, the semiconductor in the TFTs is either amorphous or polycrystalline. Materials are a-Si, poly-Si and, more seldom, CdSe. Alternative pixel switches are MIMs or thin film diodes.

A more economical method of addressing does not require the above-mentioned pixel switches, and generates the voltages across the pixels by a superposition of voltages at the contact pads. This is called Passive Matrix (PM) addressing which, however, exhibits shortcomings.

A more detailed discussion of all addressing schemes starts with Chapter 10.

14

Addressing of Liquid Crystal Displays with a-Si Thin Film Transistors (a-Si-TFTs)

An introduction to TFT addressed LCDs has been given in Chapter 2. In this and the following three chapters, we build on the introduction by first looking at the TFT as a component with a-Si and poly-Si semiconductors, its operation and properties, before we turn to the active matrix addressing of LCDs with TFTs. Then, we describe the manufacture of TFTs together with the other layers of an LC cell. Finally, two more AMLCDs with MIMs and diodes will be discussed afterwards.

14.1 Properties of a-Si Thin Film Transistors

TFTs with the voltages and currents in Figure 14.1(a) are Metal-Insulator-Semiconductor Field Effect Transistors (MIS-FETs) which are used most often as bottom-gate, and more seldom as top-gate, transistors with the schematic cross-sections in Figures 14.1(b) and 14.1(c). On a substrate, as a rule usually of glass or more recently plastic foil, the metallic bottom gate in Figure 14.1(b) is deposited and structured, followed by the gate-dielectric, the amorphous-Si semiconductor, the metallic drain and source electrodes, and a protection layer covering the semiconductor channel. The materials used are given in Figure 14.1(b). The top gate TFT in Figure 14.1(c) has an inverted sequence of layers. The main difference to a monocrystalline MIS-FET is the amorphous nature of the semiconductor. This is unavoidable, since thin film deposition processes are unable to provide crystalline layers. The most one can achieve is to induce crystal growth either thermally or by laser annealing, resulting in crystallized regions separated by grain boundaries. These poly-crystalline Si layers can be used for poly-Si-TFTs.

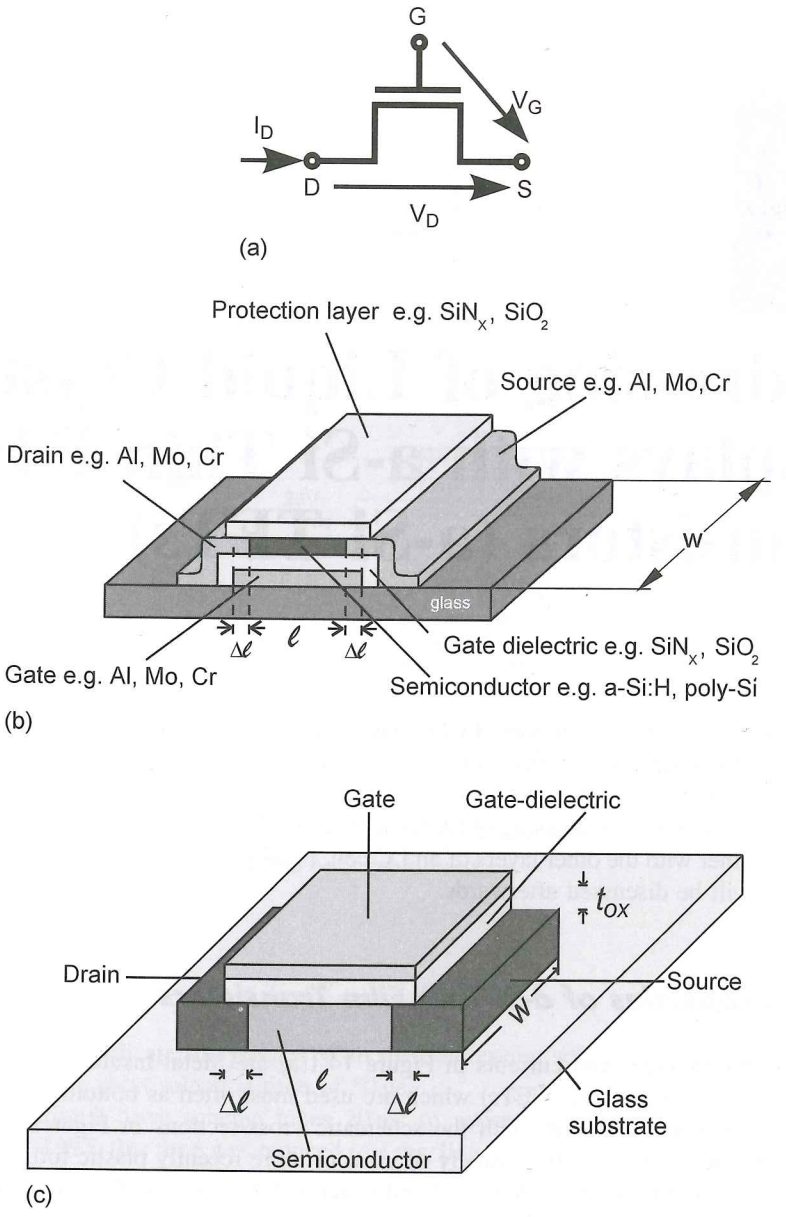


Figure 14.1 (a) The symbol for a TFT; (b) cross-section of a bottom gate TFT; (c) cross-section of a top gate TFT

The operation of an a-Si-TFT starts with a separation of charge in the capacitor between the gate electrode and the electrode formed by the drain and source, and the distribution of the potential along the upper surface of the semiconductor channel. The charge separation is induced by the gate-source voltage V_G. The voltage V_D between drain and source causes an electric field parallel to the surface of the n-channel of the a-Si, which transports the negative

charge to the drain. The drain current I_D in Figure 14.1(a) follows approximately the same well known law as for FETs (Sze, 1981; Borkon and Weimer, 1963; Khakzar, 1991). It is

$$I_D = 0 \quad \text{for} \quad V_G \leq V_{th} \tag{14.1}$$

$$I_D = \mu C_G \frac{w}{2l}((V_G - V_{th})^2 - (V_D - (V_G - V_{th}))^2) \quad \text{for} \quad V_D \leq V_G - V_{th},\ V_G > V_{th} \tag{14.2}$$

and

$$I_D = \mu C_G \frac{w}{2l}(V_G - V_{th})^2 \quad \text{for} \quad V_D > V_G - V_{th},\ V_G > V_{th}. \tag{14.3}$$

For discussion, an alternative version of the same equations will be helpful, where the sequence of the last two equations is inverted and the inequalities are rewritten:

$$I_D = 0 \quad \text{for} \quad V_G \leq V_{th} \tag{14.4}$$

$$I_D = \mu C_G \frac{w}{2l}(V_G - V_{th})^2 \quad \text{for} \quad V_G - V_{th} < V_D,\ V_G > V_{th} \tag{14.5}$$

and

$$I_D = \mu C_G \frac{w}{l}\left((V_G - V_{th})V_D - \frac{V_D^2}{2}\right) \quad \text{for} \quad V_G - V_{th} \geq V_D,\ V_G > V_{th}, \tag{14.6}$$

where μ stands for the electron mobility, and w and, respectively, for the width and length of the channel respectively.

$$C_G = \frac{\varepsilon_0 \varepsilon_r}{d} \tag{14.7}$$

is the gate capacitance, where d is the thickness of the gate dielectric, and

$$V_{th} = -e\, n_0\, d_{HL}/C_G \tag{14.8}$$

represents the threshold voltage, where e is the charge of an electron, n_0 the charge density in the semiconductor channel and at the interface to the dielectric before voltages are applied, and d_{HL} the thickness of this channel.

Equations (14.1) and (14.4) describe the ideally blocked TFT. In reality, the channel exhibits a finite sheet resistance R_{CH}, resulting in an off-current

$$I_{off} = V_D w/R_{CH}\, l \tag{14.9}$$

The transition region is governed by Equations (14.2) and (14.6), and the saturation region by Equations (14.3) and (14.5). The basis for the derivation of the equations is Shokley's gradual channel approximation (Sze, 1981), which assumes that the electric field in the channel

directed from drain to source is much larger than the field perpendicular to it. For a-Si-TFTs the equations, however, imply further approximations as effects such as localized states in the band gaps and traps at the dielectric and in the a-Si channel are not considered. As a consequence of these traps in which the electrons are caught, only about 1 percent to 5 percent of the induced charge contributes a-Si interface to the current I_D. This reflects in a low electron mobility of a-Si in the range of $0.2\,cm^2/Vs$ to $1.5\,cm^2/Vs$, whereas monocrystalline Si has more than $1800\,cm^2/Vs$. Due to these localized states, the power of 2 in Equations (14.2), (14.3), (14.5) and (14.6) is changed into an exponent in the range 2.1 to 2.3.

The reduced output characteristics derived from Equations (14.2) and (14.3), $I_{D0}=I_D/\mu C_G(w/l)=f(V_D)$ with V_G as a parameter, are plotted in Figure 14.2(a). The transition region represents parabolas opened downwards and with the vertex at

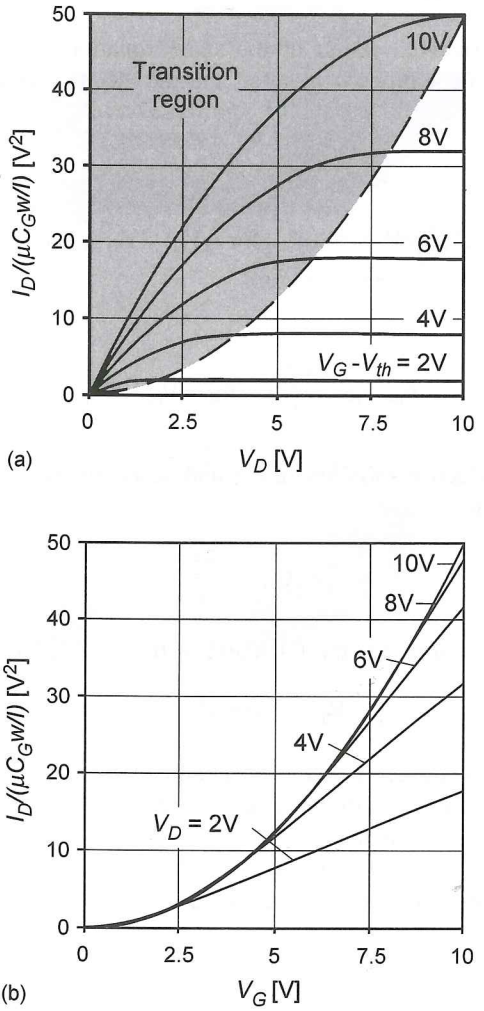


Figure 14.2 (a) Output characteristics of a TFT; (b) input characteristics of a TFT; (c) input characteristics of a TFT with $\sqrt{I_D}$ as the ordinate

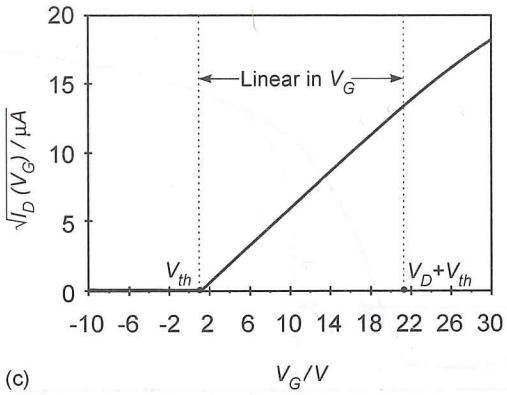


Figure 14.2 (continued)

$V_D=(V_G-V_{th})$ and $I_{D0}=(1/2)(V_G-V_{th})^2$. In the saturation region, I_{D0} is a constant. The border between the transition region and the saturation occurs for $V_D=V_G-V_{th}$. Substituting this into Equation (14.2) or (14.3) yields

$$I_{D0}=\frac{1}{2}V_D^2. \tag{14.10}$$

This border is shown as a dashed line in Figure 14.2(a).

The reduced input characteristics derived from Equations (14.5) and (14.6), $I_{D0}=I_D/\mu C_G(w/l)=f(V_G)$ with V_D as a parameter, are plotted in Figure 14.2(b). For $V_G<V_D+V_{th}$, Equation (14.5) provides the parabola

$$I_{D0}=\frac{1}{2}(V_G-V_{th})^2 \tag{14.11}$$

independent of V_D for the saturation region. In the transition region with Equation (14.6) and $V_G\geq V_D+V_{th}$, the curve for I_{D0} is linear in V_G with a steepness proportional to V_D, as shown in Figure 14.2(b).

In Figure 14.2(c) $\sqrt{I_D}=f(V_G)$ derived from Equations (14.5) and (14.6) is plotted. For $V_G<V_D+V_{th}$ in Equation (14.5), we obtain the straight line

$$\sqrt{I_D}=M(V_G-V_{th}) \tag{4.12}$$

with

$$M^2=\mu C_G\frac{w}{2l}. \tag{14.13}$$

A measurement of points on the straight line for $\sqrt{I_D}$ provides V_{th} as the intersection of this line with the abscissa and the inclination M, from which we obtain the mobility

$$\mu=M^2/C_G\frac{w}{2l}=\frac{M^2 2ld}{\varepsilon_0\varepsilon_r w}, \tag{14.14}$$

where C_G in Equation (14.7) was used.

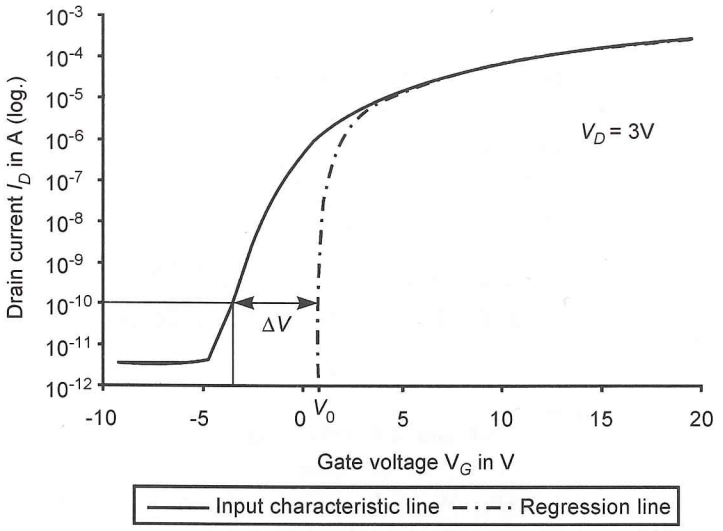


Figure 14.3 Measured (full line) and ideal (dashed line) input characteristics of a TFT with logarithmic ordinate

To determine the property of the a-Si-TFT at small currents we plot the measured data $I_D = f(V_G)$ as the logarithmic curve $\log I_D = f_0(V_G)$ in Figure 14.3. Further, we plot the curve derived from the saturation region in Equation (14.5) as the log I_D of the parabola in Equation (14.5), shown as a dashed line in Figure 14.3. We define the voltage ΔV in Figure 14.3 as the difference between the saturation curve and the measured curve at an off-current of 10^{-10} A. The smaller is ΔV, the better are the blocking properties of the TFT. As a substitute for ΔV, the off-current in Equation (14.9) also describes the blocking performance.

The three quantities μ, V_{th} and ΔV or I_{off} define an a-Si-TFT well enough for our applications, where μ is derived from the saturation region and ΔV or I_{off} from the low current region. Typical values are $\mu = 0.8\,\text{cm}^2/\text{Vs}$, $V_{th} = 1\text{V}$, $\Delta V = 2.5\,\text{V}$ and $I_{off} = 10^{-12}\,\text{A}$ at $-3.5\,\text{V}$.

14.2 Static Operation of TFTs in an LCD

The operation of TFTs as switches at the pixels allowing the video voltage at the columns to charge the storage capacitors has been outlined in Chapter 2. The circuit is depicted in Figure 2.16. The charging of the storage capacitors $C_{LC} + C_s$ in a pixel must occur with a small enough time constant T_{on} in Equation (2.18) from which the limit for the on-resistance R_{on} of the TFT follows as

$$R_{on} \leq \frac{0,1T_f}{N(C_{LC} + C_s)}. \tag{14.15}$$

On the other hand, this resistance can be expressed by a basic equation for current transport in a medium with mobility μ, and the areal charge density σ, that is the density in a unit area

with the thickness d_{HL} of the channel with width w and length l, as (Sze, 1981)

$$R_{on} = \frac{l}{\mu\sigma w}. \tag{41.16}$$

The charge on $C_{LC}+C_s$ defines the grey shade, and hence imposes the constraint in Equation (2.19) on the time constant T_{off} of the discharge. This results in the constraint for R_{off} of the TFT

$$R_{off} \geq \frac{200T_f}{C_{LC}+C_s}. \tag{14.17}$$

The constraints for R_{on} and R_{off} will be required for the discussion of the performance of a TFT in the environment of a pixel in Figure 14.4. The TFT is embedded in its own voltage dependent parasitic capacitance C_{GS}, C_{GD} and C_{DS}; C_{LC} is the capacitance and R_{LC} the resistance of the LC layer, with the lower electrode being at ground; C_s is an additional thin film storage capacitance enhancing the value of C_{LC}. However, C_s is not connected to ground as is C_{LC}, but to the next gate line, saving a ground line. From the two columns the parasitics C_{c1e} and C_{c2e} shown in Fig. 14.7 couple onto V_p, which is equal to V_{LC}. The voltage V_{FP} at the front-plate will be explained later. The rows r_1 and r_2 are gate lines, and carry the gate pulses V_{r1} and V_{r2} in Figures 14.4 and 14.5, which render the appropriate TFTs conductive during row address time T_r with voltage V_g, and block it with voltage V_0 in Figure 14.5 during the remainder of T_f. The video signal V_{c1} on column 1 is positive during one frame time T_f and, in order to provide an almost dc-free pixel voltage, V_{c1} is negative during the following frame time. Capacitive voltage dividers transmit the steps of the gate voltage onto V_{LC}, where they cause visible changes in the grey shade. Assuming that 256 grey shades are generated by a voltage swing of 8 V, then 31 mV define one grey shade. This demonstrates how precisely V_{LC} has to be maintained.

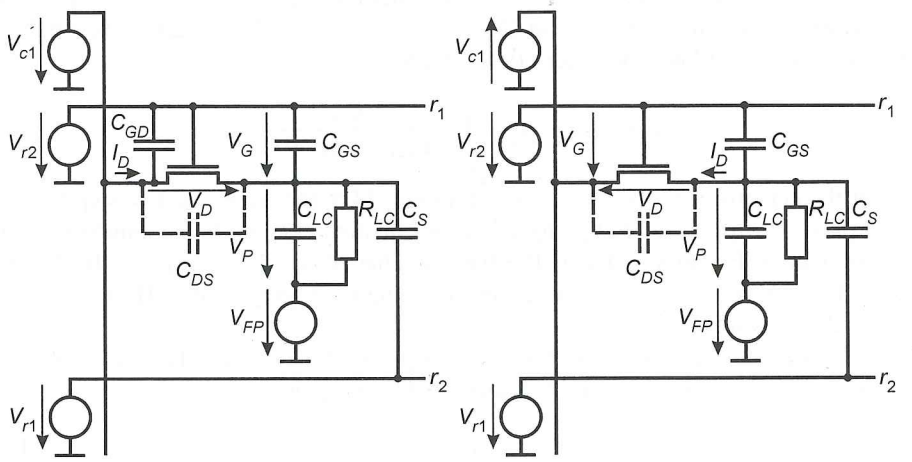


Figure 14.4 The TFT and its environment in a pixel (a) for charging of C_{LC} to a positive voltage and (b) to a negative voltage

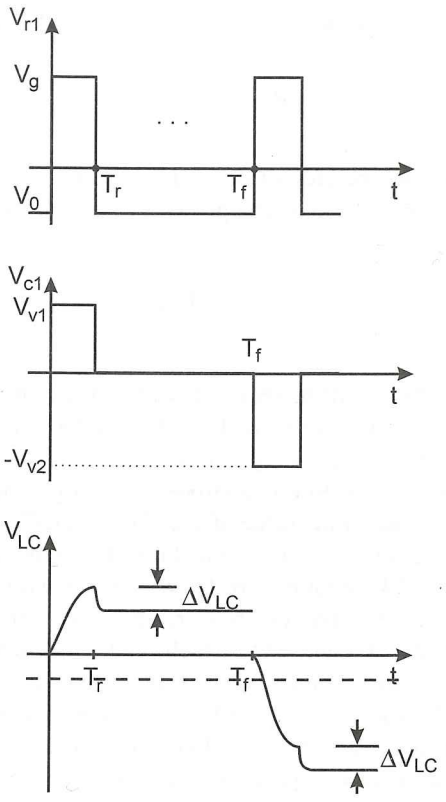


Figure 14.5 The gate impulses and their effect on the pixel voltage V_p

V_{LC} in Figure 14.5 reaches the desired value V_{v1} within T_r. Then the negative step $-(V_g - V_0)$ of the row pulse, that is the falling edge of V_{r1} at $t = T_r$, reaches V_{LC} through the capacitive voltage devider C_{GS} and $C_{LC} + C_s$ as a stepwise change ΔV_{LC}, first published by Suzuki (1987) and later by Lauer (1996), with

$$\Delta V_{LC} = -(V_g - V_0)\frac{C_{GS}}{C_{GS} + C_{LC} + C_s}. \tag{14.18}$$

Also, for the negative video-voltage $-V_{v2}$ in Figure 14.5, the same negative step $V_g - V_0$ of the row pulse V_{r1} again lowers V_{LC} by ΔV_{LC} in Equation (14.18). Some numbers illustrate the importance of Equation (14.18). The typical values $C_{GS} = 20\,\text{fF}$, $C_{LC} = 80\,\text{fF}$, $C_s = 60\,\text{fF}$ and $V_g - V_0 = 8\,\text{V}$ result in $\Delta V_{LC} = 1\,\text{V}$, corresponding to 30 grey shades. Hence, a compensation of ΔV_{LC} is required.

Another derivation of ΔV_{LC} reveals other aspects of its nature (Howard, 1995). The charge Q in the channel during the presence of the gate pulse is

$$Q = \sigma w(l + 2\Delta l) < 0, \tag{14.19}$$

where σ is the electron charge used in Equation (14.16) and Δl is the length of the overlap between drain or source with the gate in Figure 14.1(a). After the drop to zero of the gate

impulse, a part k of this negative charge is distributed mainly onto the larger capacitances C_{LC} and C_s, causing the voltage drop

$$\Delta V_{LC} = \frac{kQ}{C_{LC} + C_s} = \frac{k\sigma w(l + 2\Delta l)}{C_{LC} + C_s} < 0. \tag{14.20}$$

Substituting $C_{LC}+C_s$ in Equation (14.20) by $C_{LC}+C_s$ in Equation (14.15), and eliminating R_{on} by Equation (14.16), yields

$$\Delta V_{LC} \leq \frac{Nl(l + 2\Delta l)k}{2 \cdot 0.1 T_f \mu}. \tag{14.21}$$

This equation demonstrates that $|V_{LC}|$ can be decreased by a large mobility and a small channel length, as well as a small overlap Δl. The technology for TFTs has to take note of these requirements. A further means to decrease $|\Delta V_{LC}|$ is to choose a large C_s in Equation (14.18), which is limited, however, by the constraint in Equation (14.15) and the area needed in the pixel. Finally, a small C_{GS} in Equation (14.18) is also helpful. It is achieved by a large thickness of the gate dielectric which, however, reduces C_G and I_D in Equation (14.2).

The shift of V_{LC} by ΔV_{LC} not only causes changes in the grey shades, but also generates a damaging dc voltage. A remedy for both is to lower the potential of the back plate by $|\Delta V_{LC}|$ to the dashed line in Figure 14.5, which requires a voltage source V_{FP} in Figures 14.4(a) and 14.4(b) with

$$V_{FP} = \Delta V_{LC} < 0. \tag{14.22}$$

As C_{GS} and C_{LC} are voltage dependent, in this case they depend upon the video voltage, an average value for ΔV_{LC} has to be chosen.

A further, more costly, remedy is to introduce the compensation impulse V_{com} in Figure 14.6 (Khakzar, 1991). The lines are now addressed starting with the lowermost one, that is

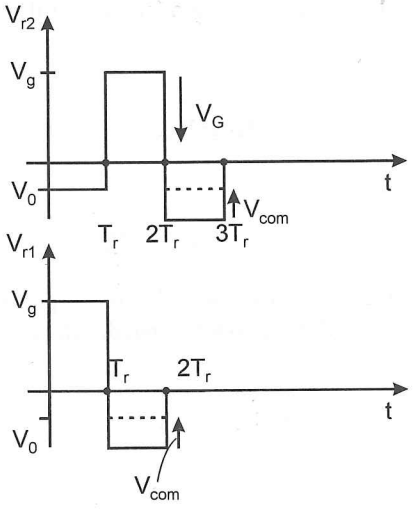


Figure 14.6 The TFT addressing with a compensation impulse

with the row voltage V_{r1}. Then row two is addressed. The falling edge of V_{r2} has increased by V_{com} to $V_g - V_0 + V_{com}$, $V_0 < 0$ resulting in a ΔV_{LC} as

$$\Delta V_{LC} = -(V_g - V_0 + V_{com}) \frac{C_{GS}}{C_{GS} + C_{LC} + C_S}. \tag{14.23}$$

A step V_{com} in the compensation impulse of the previously addressed line r_1 feeds through the capacitive voltage divider C_s and $C_{GS} + C_{LC}$ the voltage

$$\Delta V_{com} = V_{com} \frac{C_s}{C_s + C_{LC} + C_{GS}} \tag{14.24}$$

onto V_{LC} of row r_2, as is shown in Figure 14.6. For compensation of ΔV_{LC} we require

$$\Delta V_{LC} + \Delta V_{com} = -(V_g - V_0 + V_{com}) \frac{C_{GS}}{C_{GS} + C_{LC} + C_s} + V_{com} \frac{C_s}{C_{GS} + C_{LC} + C_s} = 0,$$

providing

$$V_{com} = (V_g - V_0) \frac{C_{GS}}{C_s - C_{GS}}. \tag{14.25}$$

With $V_g - V_0 = 8\,V$, $C_{GS} = 20f\,F$ and $C_s = 60f\,F$, we obtain $V_{com} = 4\,V$.

Now we are ready to derive the requirements for the values of the row voltages V_g in the on state (Schwarz, 1990; Lauer, 1996) and V_0 in the off state (Schwarz, 1990) in Figure 14.5. We perform this with one of the two corrections of the voltage shift ΔV_{LC}, namely by shifting the potential V_{FP} of the back plate by ΔV_{LC} in Equation (14.18), or by the compensation impulse V_{com} in Equation (14.25). The effect of V_{com} on V_{LC} is the same as the lowering of the front plate potential by ΔV_{LC}. Therefore, introducing the voltage source $V_{FP} = \Delta V_{LC}$ in Equation (14.18) describes both correction methods, and is used in the calculation of V_g and V_0. For the further calculations, we recall that V_g is the row voltage in Figures 14.4 and 14.5 and V_G is the gate-source voltage of the TFT in Figures 14.1(a) and 14.4.

In the on state, we require

$$V_G \geq V_{th}. \tag{14.26}$$

From Figure 14.4(a), we obtain

$$V_g = V_G + V_{LC} + V_{FP} \tag{14.27}$$

for a positive voltage V_{LC}. Figure 14.4(b) provides for negative voltages V_{LC}, where the transistor operates with source and drain interchanged, which is possible due to the symmetry of the TFT,

$$V_g = V_G + V_{c1}. \tag{14.28}$$

The video-voltage V_{c1} is

$$V_{min} \leq V_{c1} \leq V_{max} \tag{14.29}$$

for positive V_{c1}, and

$$-V_{max} \leq V_{c1} \leq -V_{min} \tag{14.30}$$

for negative V_{c1} in Equation (14.28). The voltage across the pixel is, according to Figures 14.4(a) and 14.4(b), with $V_D=0$ in the conductive state

$$V_{LC} = V_{c1} - V_{FP}. \tag{14.31}$$

V_{min} and V_{max} are chosen such that V_{LC} in Equation (14.31) covers the entire linear interval of the luminance-voltage curve of the LC cell.

From Equation (14.27), we obtain, with Equation (14.26), for the worst case

$$V_g \geq V_{th} + V_{LC\,max} + V_{FP}. \tag{14.32}$$

With $V_{LCmax}=V_{c1max}-F_{FP}=V_{max}-F_{FP}$, where Equations (14.31) and (14.29) were used, we finally obtain from Equation (14.32)

$$V_g \geq V_{th} + V_{max} \tag{14.33}$$

for positive voltages V_{LC}. For negative voltages, Equtions (14.28), (14.30) and (14.31) yield similarly

$$V_g \geq V_{th} - V_{min} \tag{14.34}$$

The stronger condition (14.34) has to be used for the design of the electronics.

For the derivation of V_0 in Figure 14.5 (Takahashi *et al.*, 1990), where the pixel is not selected, we require

$$V_G < V_{th}, \tag{14.35}$$

and similarly to Equation (14.32) for the worst case,

$$V_0 \leq V_{th} + V_{LC\,min\,a} + V_{FP}. \tag{14.36}$$

For holding the stored charge, Equation (14.36) has to be considered after the steps of all voltages have exercised their effect ΔV_{LCmax}, in all the conditions where V_{LCmin} occurs. This voltage is

$$V_{LC\,min\,a} = V_{LC\,min\,b} + \Delta V_{LC\,max} \tag{14.37}$$

with

$$V_{LC\,min\,b} = V_{c1} - V_{FB}, \tag{14.38}$$

which is the voltage across C_{LC} before the drop caused by the row voltage. In Equation (14.37),

$$\Delta V_{LC\,max} = -(V_g - V_0)\frac{C_{GS}}{C_{GS} + C_{LC\,min} + C_s} \tag{14.39}$$

is the largest drop derived from Equation (14.18).

Inserting Equations (14.37), (14.38), (14.39) and V_g from constraint (14.33) into Equation (14.36) with $V_{c1} = V_{max}$ yields, for the worst case,

$$V_0 \leq V_{th} - V_{max} \frac{2C_{GS} + C_{LC\,min} + C_s}{C_{LC\,min} + C_s}. \tag{14.40}$$

The row voltage V_g in Equation (14.37) in the on-stage and V_0 in Equation (14.40) in the off-stage, as well as the shift of the potential of the front-plate by V_{FP} in Equation (14.22) or the compensation impulse V_{com} in Equation (14.25) determine the row address signals. In the performance of both solutions, the shifted back-plate potential or the compensation impulse are equivalent. The shifted front-plate potential is more often used, because one can use gate line drivers independent of the TFT-specific and pixel design-specific compensation impulse in Equation (14.25).

Not only the falling flanks of the row address signals in Figure 14.5, but also the rising flanks couple a voltage onto V_{LC}. Although it is transitory as the last flank, the falling edge determines the steady state, the effects may be visible as jitter. This adverse influence can be eliminated by introducing a second line to ground, to which C_s is connected, as shown in Figure 14.7. This additional line does not, of course, remove the effect on V_{LC} stemming from the falling flank of the gate impulse. However, it removes the possibility of feeding in the compensation impulse. Hence, the only correction left is the shift of the potential of the back plate.

In addition, the currents for charging and reverse charging the storage capacitors flow in the gate line, changing the potential of the line where charging takes place. This is especially noticeable in large displays with a higher resistance of the lines. It can be significantly reduced by alternating the sign of neighbouring column signals.

Further capacitive couplings in Figure 14.7 feed the video signals V_{c1} and V_{c2} of the two columns bordering a pixel through the parasitic capacitances $C_{c1e} + C_{SD}$ and C_{c2e} onto $C_{LC} + C_S$, causing the pixel voltage to change by

$$\Delta V_{LC} = V_{c1} \frac{C_{c1e} + C_{SD}}{C_{c1e} + C_{SD} + C_{LC} + C_S} + V_{c2} \frac{C_{c2e}}{C_{c2e} + C_{LC} + C_S}. \tag{14.41}$$

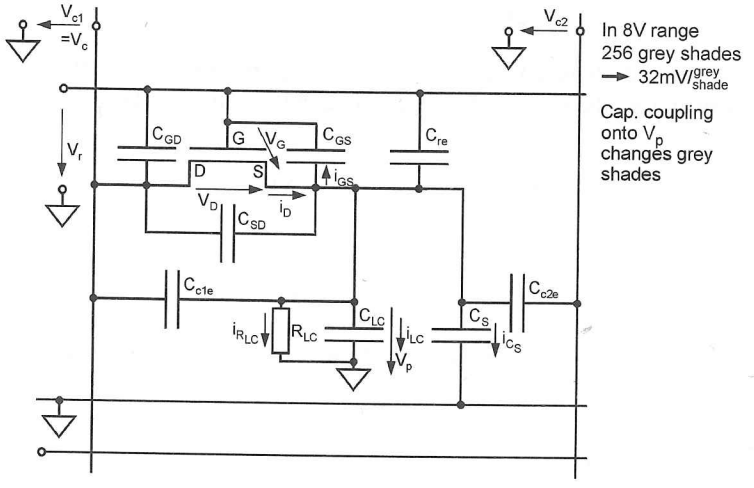


Figure 14.7 The TFT in a pixel with voltages, currents and parasitic capacitances

An exact compensation to $\Delta V_{LC}=0$ is impossible as V_{c1}, V_{c2}, $C_{SD}(V)$ and $C_{LC}(V)$ are dependent on the video voltages. A substantial decrease of ΔV_{LC} is achieved by alternating the signs of V_{c1} and V_{c2} either after each frame or line by line, or even better, from column to column, or as the ultimate, framewise, linewise and columnwise combined.

The capacitive coupling is noticeably reduced by replacing the steep falling edge of the row impulse by the gradual decline in Figure 14.8(a). As this increases the addressing time, an overlap of the two consecutive gate pulses in Figure 14.8 restores the previous speed. Rounding-off the upper portion of the flank in Figure 14.8(b) and then staying with the steep drop has the same beneficial effect. The gate line represents an RC-line, including the crossover capacitances of rows and columns. The step response of a homogeneous RC-line at the end of the line is

$$V_s(t) = V_g\left(1+\frac{2}{\pi}\sum_{i=1}^{\infty}\frac{(-1)^i}{i-(1/2)}\exp\frac{-\pi^2(i-(1/2))^2}{R_{tot}C_{tot}}t\right), \tag{14.42}$$

where R_{tot} and C_{tot} are the total resistance and capacitance of the line. The step response exhibits a delay and a decrease of the rise time T_0 from 10 percent to 90 percent of the final values to $T_0 \approx 0.9\, R_{tot}C_{tot}$ (Lauer, 1996). The delay and reduced rise time limit the resolution r for a display with a diagonal D by the relationship (Howard, 1995)

$$r \approx \frac{1}{\varsigma_s D^3(1+\alpha)}, \tag{14.43}$$

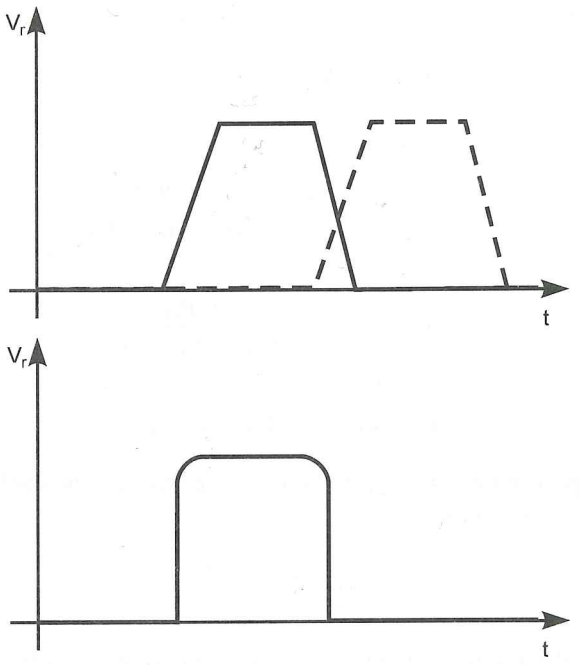


Figure 14.8 Gate pulses for diminished cross talk (a) with trapezoidal and (b) with rounded wave form

where ζ_s is the sheet resistance of the row and $\alpha = f(C_s/C_{LC})$, typically $\alpha \approx 1$. The resolution may be enhanced by reducing the gate line (row) resistance by progressively replacing Mo/Ta by Al and Cu for large diagonal displays.

14.3 The Dynamics of Switching by TFTs

The row address voltages derived in the previous section are steady state values reached after an infinite time. In this section, a differential equation will provide the desired voltages at any time, such as the time T_r with more realistic components such as an LC material with the resistance R_{LC} and a nonlinear TFT.

The differential equation for $V_{LC}(t)$ (Stroomer, 1984; Miyata *et al.*, 1998) is formulated for the ac values in Figure 14.7, and starts with the node equation

$$i_{C_{GS}} + i_{C_{LC}} + i_{C_S} + i_{R_{LC}} = i_D, \tag{14.44}$$

or as a differential equation with $i_C = C\dot{V}$

$$(C_{GS} + C_{LC} + C_S)\dot{V}_{LC} + \frac{V_{LC}}{R_{LC}} = i_D = \mu C_G \frac{w}{l}\left(V_r - V_{LC} - V_{th} - \frac{V_C - V_{LC}}{2}\right)(V_c - V_{LC}), \tag{14.45}$$

where Equation (14.6) for the TFT in the transition region and $V_G = V_r - V_{LC}$ and $V_D = V_C - V_{LC}$ have been used. Reordering of Equation (14.45) provides Riccati's nonlinear differential equation

$$\dot{V}_{LC} = k_1 V_{LC}^2 + k_2 V_{LC} + k_3 \tag{14.46}$$

with

$$k_1 = k/2 \quad \text{and} \quad k = \frac{\mu C_G w/l}{C_{GS} + C_{LC} + C_S},$$

$$k_2 = k(V_{th} - V_r) - \frac{1/R_{LC}}{C_{GS} + C_{LC} + C_S},$$

$$k_3 = kV_c(V_r - V_{th} - V_c/2).$$

As a rule, the simplification $|\mu C_G w/l(V_{th} - V_r)| \gg 1/R_{LC}$ can be applied. The nonlinear transformation of Equation (14.44)

$$V_{LC}(t) = V_c + \frac{1}{\overline{V_{LC}}(t)} \tag{14.47}$$

provides the first order linear differential equation with constant coefficients

$$\dot{\overline{V}}_{LC} = -(2k_1 V_c + k_2)\overline{V}_{LC} - k_1, \tag{14.48}$$

To avoid inconsistancies with the dimension V in Equation (14.47), one would have to divide Equation (14.46) by 1V. For simplicity, the ensuring normalized terms are denoted unchanged V_{LC} including the new variable $\overline{V}_{LC}$.

The general solution of Equation (14.48) is

$$\overline{V}_{LC}(t) = \frac{-k_1}{2k_1 V_c + k_2} + ae^{-(2k_1 V_c + k_2)t}, \tag{14.49}$$

where a is the integration constant. The initial condition $V_{LC}(0) \neq 0$ yields, with (14.47),

$$\overline{V_{LC}}(0) = 1/(V_{LC}(0) - V_c),$$

and with Equation (14.48),

$$a = \frac{1}{V_{LC}(0) - V_c} + \frac{k_1}{2k_1 V_c + k_2}. \tag{14.50}$$

Substituting the constant a in Equation (14.49) finally leads to the solution

$$V_{LC}(t) = V_c + \left[\frac{1}{2q} + \left(\frac{1}{V_{LC}(0) - V_c} - \frac{1}{2q}\right)e^{kqt}\right]^{-1}, \tag{14.51}$$

with

$$q = V_r - V_{th} - V_c. \tag{14.52}$$

The time $t = T_{r-}$, the time immediately before the end of the charging period, gives the pixel voltage to which C_{LC} has been charged. The stepwise change ΔV_{LC} in Equation (14.18) due to the falling flank of V_r occurs immediately afterwards reducing $V_{LC}(T_{r-})$ from Equation (14.51).

Charging $C_{LC} + C_S$ to a negative voltage in Figure 14.4(b) is governed by the node equation

$$-i_{GD} - i_{C_{LC}} - i_{C_S} - i_{R_{LC}} = i_D = \mu C_G \frac{w}{l}\left(V_r - V_{LC} - V_{th} - \frac{V_{LC} - V_C}{2}\right)(V_{LC} - V_C). \tag{14.53}$$

With the same considerations as for the charging to a positive voltage, this leads to Riccati's differential equation

$$\dot{V}_{LC} = k_1' V_{LC}^2 + k_2' V_{LC} + k_3' \tag{14.54}$$

with

$$k_1' = \frac{k'}{2} \quad \text{and} \quad k' = \frac{\mu C_G w/l}{C_{GD} + C_{LC} + C_S},$$

and

$$k_3' = k' V_c (V_r V_{th} - V_c/2).$$

After the transformation Equation (14.47), we finally obtain the solution

$$V_{LC}(t) = V_c + \left[\frac{1}{2q} + \left(\frac{1}{V_{LC}(0) - V_c} - \frac{1}{2q}\right) e^{k' q t}\right]^{-1} \tag{14.55}$$

for charging C_{LC} to a negative voltage; k' is given below Equation (14.54), and q in Equation (14.52). The results in Equations (14.51) and (14.55) are now used to determine the voltages V_g for the on state and V_0 for the off state of the TFT.

The main requirement for the voltage V_{LC} is that it reaches within T_r the desired voltage V_c, determining the grey shade, and that it remains constant during the remainder of T_f. Reaching V_c within T_r is equivalent to equal voltages $V_{LC}(t)$ at $t = T_{r-}$, T_{r+} and negative equal ones at $t = T_f + T_{r-}$, $T_f + T_{r+}$. This is expressed by the requirement

$$V_{LC}(T_{r-}) = V_{LC}(T_{r+}) = -V_{LC}(T_f + T_{r-}) = -V_{LC}(T_f + T_{r+}). \tag{14.56}$$

Inserting Equations (14.56) into Equations (14.51) and (14.55) leads to the conditions

$$\left[\frac{1}{2q} - \left(\frac{1}{2V_c} + \frac{1}{2q}\right) e^{kqT_r}\right]^{-1} \to 0 \tag{14.57}$$

and

$$\left[\frac{-1}{2q} - \left(\frac{1}{2V_c} - \frac{1}{2q}\right) e^{k' q T_r}\right]^{-1} \to 0 \tag{14.58}$$

for charging to V_c and to $-V_c$. It is practical to replace 0 by a limit εV_{LC} with $|\varepsilon| \leq 1$, and as close to zero as required by the display performance (Suzuki, 1992). With this constraint, Equations (14.51) and (14.55) yield

$$\left[\frac{-1}{2q} + \left(\frac{1}{2V_c} + \frac{1}{2q}\right) e^{kqT_r}\right]^{-1} \leq \varepsilon V_{LC}, \quad \text{for } V_c > 0 \quad \text{and} \tag{14.59}$$

$$\left[\frac{-1}{2q} - \left(\frac{1}{+2V_c} + \frac{1}{2q}\right) e^{k' q T_r}\right]^{-1} \leq \varepsilon V_{LC}, \quad \text{for } V_c < 0, \tag{14.60}$$

where it was considered that in Equation (14.59) the steady state was reached from below, and in Equation (14.60) from above. Rewriting Equations (14.59) and (14.60) provides

$$kqT_r \geq \ln\left(\frac{1 + 2q/\varepsilon V_{LC}}{1 + q/V_c}\right) \quad \text{for } V_c > 0 \quad \text{and} \quad V_{LC} < 0 \quad \text{and} \tag{14.61}$$

$$k' q T_r \geq \ln\left(\frac{1 + 2q/\varepsilon V_{LC}}{1 + q/V_c}\right) \quad \text{for } V_c < 0 \quad \text{and} \quad V_{LC} < 0. \tag{14.62}$$

According to Equations (14.51) and (14.29) as well as (14.55) and (14.30), the time constants for charging to $+V_c$ and to $-V_c$) are respectively

$$\tau_+ = \frac{1}{\mu C_G w/l} \frac{C_{GS} + C_{LC} + C_S}{V_r - V_{th} - V_c} \quad \text{for } V_{min} \leq V_c \leq V_{max} \tag{14.63}$$

and

$$\tau_- = \frac{1}{\mu C_G w/l} \frac{C_{GD} + C_{LC} + C_S}{V_r - V_{th} - V_c} \quad \text{for } -V_{max} \leq V_c \leq -V_{min}. \tag{14.64}$$

For $C_{GS} = C_{GD}$ and considering $V_c < 0$ in Equation (14.64), we recognize

$$\tau_- < \tau_+.$$

The largest time constant is encountered for $V_c = V_{max}$ in Equation (14.63) reaching the value

$$\tau_+ = \tau_{max} = \frac{1}{k_{max}(V_r - V_{th} - V_{max})}, \tag{14.65}$$

where

$$k_{max} = \frac{\mu C_G w/l}{G_{GS} + C_{LC\,max} + C_S}. \tag{14.66}$$

The constraint in Equation (14.61) is stronger than that in Equation (14.62), because it is associated with the larger time constant τ_+. For the worst case, constraint (14.61) provides

$$k_{max} T_r (V_g - V_{th} - V_c) \geq \ln \frac{1 + 2(V_g - V_{th} - V_c)/\varepsilon V_{LC}}{1 + (V_g - V_{th} - V_c)/V_c}, \tag{14.67}$$

where $V_r = V_g$ for $V_r > 0$ was used.

The voltage-dependent non-linear capacitance $C_{LC}(V_{LC})$ is depicted in Figure 14.9. The minimum value is reached if the electric field is perpendicular to the director with a dielectric constant $n_\perp < n_\parallel$ and the maximum if the field is parallel to the director.

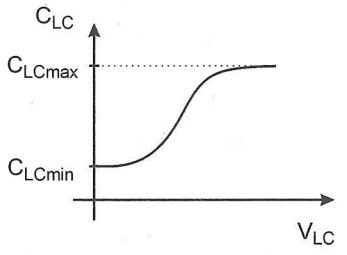


Figure 14.9 The voltage dependent capacitance of liquid crystals

The constraint (14.67) provides, in form of $u = V_g - V_{th} - V_c$, a nonlinear equation for the smallest V_g with given values of V_c, V_{th}, V_{LC}, ε, T_r and k_{max} in Equation (14.66); this equation may be solved by an approximation method such as Newton's. The chosen V_g should be too much above the minimum for V_g, in order to avoid disturbing nonlinearities of the TFT.

For the determination of the blocking voltage V_0, we investigate two cases (Lauer, 1996). First, in the pixel under investigation, $C_{LC} = C_{LC\,min}$ is charged to V_{min}. As a consequence of the linewise sign inversion, the column signals for other pixels travelling down a column are for black pixels in the column $V_c = +V_{min}$ or $V_c = -V_{min}$ in time $T_f - T_r$ during which V_{min} across $C_{LC\,min}$ is maintained. Therefore, the TFT in the pixel with $C_{LC\,min}$ experiences during the time $T_f/2$, that is assuming half the time for a positive and half the time for a negative $V_c = \pm V_{min}$

$$V_{D1} = 0 \tag{14.68}$$

and

$$V_{D2} = 2V_{min}. \tag{14.69}$$

Due to these equations, only during time $T_f/2$ is a current I_D flowing through the TFT.

The ensuing decrease of V_{LC} by dV_{LC1} during the time $T_f - T_r \approx T_f$ degrades the image, because of the parasitic discharge of capacitors by a current I, resulting in

$$dV_{LC1} = \frac{I}{C_{GS} + C_{LC\,min} + C_S} dt \approx \frac{I}{C_{GS} + C_{LC\,min} + C_S} T_f. \tag{14.70}$$

With $I = -(I_D/2) - i_{R_{LC}}$ as the currents in Figure 14.7 discharging $C_{GS} + C_{LC\,min} + C_S$, we obtain from Equation (14.70) in the worst case

$$dV_{LC1} = \frac{T_f}{C_{GS} + C_{LC\,min} + C_S} \left(-\frac{I_D(V_G, V_{D2})}{2} - \frac{V_{min}}{R_{LC}} \right). \tag{14.71}$$

The current $I_D/2$ must be considered because it flows only during time $T_f/2$, and not T_f as in Equation (14.71). Our goal is to minimize the degradation of the image by selecting a low enough V_0 blocking the TFT.

In the second case, $C_{LC} = C_{LC\,max}$ is charged to V_{max}. As a consequence of the linewise sign inversion, the column signal travelling along the column during $T_f - T_r$, in which V_{max} is maintained across $C_{LC\,max}$, is $V_c = \pm V_{max}$. Hence, the voltage V_D at the TFT during the time $T_f/2$ is either

$$V_{D3} = 0 \tag{14.72}$$

or

$$V_{D4} = 2V_{max}. \tag{14.73}$$

The ensuing decrease of V_{LC} is

$$dV_{LC2} = \frac{T_f}{C_{GS} + C_{LCmax} + C_S} \left(-\frac{I_D(V_G, V_{D4})}{2} - \frac{V_{max}}{R_{LC}} \right). \tag{14.74}$$

The value with the largest magnitude

$$dV_{LC} = \max(dV_{LC1}, dV_{LC2}) \tag{14.75}$$

is required to be at least by a factor $\varepsilon > 0$ smaller than for instance, V_{min}, leading to

$$dV_{LC} = \max(|dV_{LC1}|, |dV_{LC2}|) = dV_{LCmax} = \varepsilon V_{min} \tag{14.76}$$

This limits the parasitic discharge of C_{LC} in the most severe case when it is charged to V_{min}. Solving Equations (14.71) and (14.74) for I_D, with the boundary in (14.76), yields

$$|I_D(V_G, V_{D2})| \leq 2\left(\frac{C_{GS} + C_{LC\,min} + C_S}{T_f} dV_{LC\,max} - \frac{V_{min}}{R_{LC}}\right) = I_{D2} \tag{14.77}$$

and

$$|I_D(V_G, V_{D4})| \leq 2\left(\frac{C_{GS} + C_{LC\,max} + C_S}{T_f} dV_{LC\,max} - \frac{V_{max}}{R_{LC}}\right) = I_{D4}, \tag{14.78}$$

where

$V_{D2} = 2V_{min}$ according to Equation (14.69),

$V_{D4} = 2V_{max}$ according to Equation (14.73),

and

$dV_{LC\,max}$ is taken from Equation (14.76).

In both cases, there is only a solution if the conditions

$$\frac{V_{min}}{R_{LC}} \leq \frac{C_{GS} + C_{LC\,min} + C_S}{T_f} dV_{LC\,max} \tag{14.79}$$

and

$$\frac{V_{max}}{R_{LC}} \leq \frac{C_{GS} + C_{LC\,max} + C_s}{T_f} dV_{LC\,max} \tag{14.80}$$

are met. They ensure a positive I_D. If they are not met, V_{min} or V_{max} and ε in Equation (14.76) have to be adjusted accordingly which, however, worsens the performance of the LCD.

The possibility of meeting the conditions in Equations (14.77) and (14.78) are checked by using the measured logarithmic input characteristics in Figure 14.10. The ideal characteristics due to Equations (14.5) and (14.6), shown as a dotted line, do not include the low off-currents caused by the off-resistance of the TFT being finite. We require the measured input characteristics for the drain-source voltages $V_{D2}=2V_{min}$ and $V_{D4}=2V_{max}$ in Equations (14.69) and (14.73) as parameters. The two curves are shown in Figure 14.10.

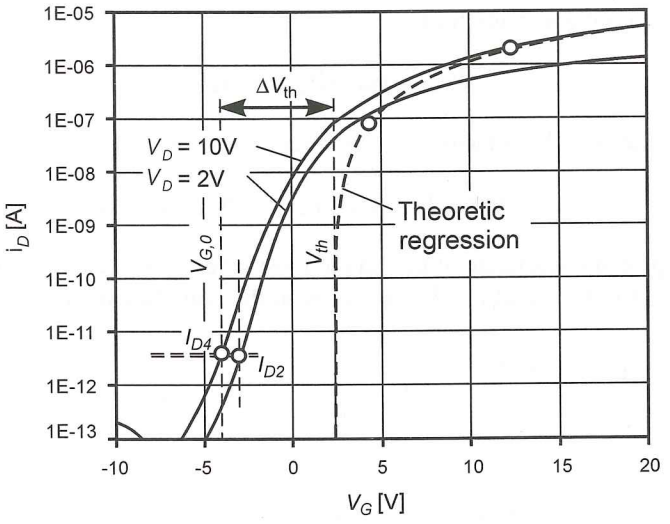


Figure 14.10 The measured logarithmic input characteristics of an a-Si-TFT with the off-currents

The point I_{D2} from Equation (14.76) on the curve with parameter $V_{D2}=2V_{min}$ and the point I_{D4} from Equation (14.78) on the curve with parameter $V_{D4}=2V_{max}$ determine the pertinent gate voltages V_G. The smaller of those two voltages is called V_{G0}, and it represents the more demanding case to be realized in the circuit. This indicates that the real threshold voltage $V_{th0}=V_{G0}$ replaces the ideal threshold V_{th} in Equation (14.40), which now becomes

$$V_0 < V_{G0} - V_{max}. \tag{14.81}$$

V_{G0} is, by $\Delta V_{th}=V_{th}-V_{G0}$, lower than V_{th}, as is indicated in Figure 14.10.

A practical example will demonstrate that the row voltage $V_r=V_0$ obtained in Equation (14.81) by investigating the dynamics of the addressing circuit can be considerably lower than V_0 in Equation (14.40) based on the ideal behaviour of the TFT.

The following data are given: $V_{min}=1\,V$, $V_{max}=5\,V$, $C_{LC\,min}=40\,fF$, $C_{LC\,max}=80\,fF$, $C_S=60\,fF$, $C_{GS}=20\,fF$ and, in Figure 14.10, $V_{th}=2.38\,V$. Equations (14.77) and (14.78) provide $I_D \leq 3.4\cdot 10^{-12}\,A$ for $V_{D2}=2\,V$ and $I_D \leq 3.8\cdot 10^{-12}\,A$ for $V_{D4}=10\,V$. The smaller of the two pertinent gate-source voltages in Figure 14.10 is $V_{G0}=-4\,V$ yielding, with Equation (14.81) $V_0<-9\,V$. V_0 in Equation (14.40) would have yielded $V_0=-4.62\,V$. The substantial change to Equation (14.81) is due to the corrected input characteristics for low off-currents in Figure 14.10.

14.4 Bias-Temperature Stress Test of TFTs

The measurements which determine μ, V_{th} and ΔV characterize the actual performance of a TFT. For stability over time, the shift ΔV_{th} of the threshold voltage is the most important property for addressing of LCDs. The investigations in Sections 14.2 and 14.3 demonstrate that the appropriate grey shade and the blocking property of a TFT are based on V_{th}.

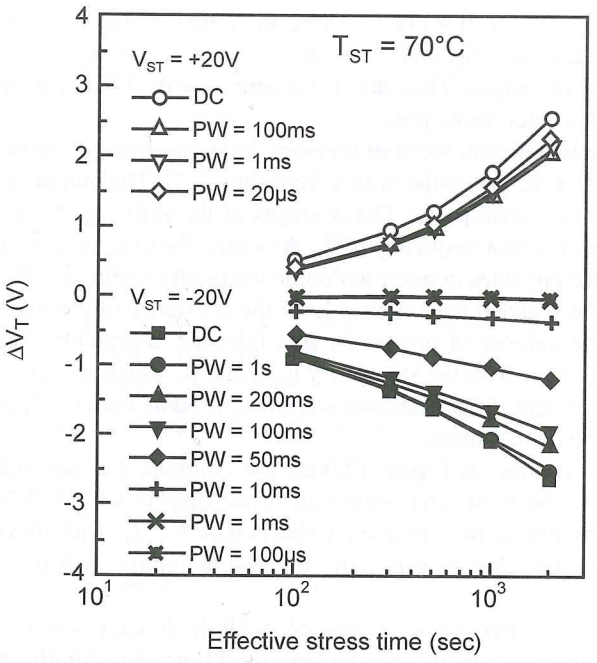


Figure 14.11 The shift of V_{th} during bias temperature stress tests

Equation (14.8) describes how V_{th} depends upon the charge trapped in the semiconductor at the interface to the dielectric and in the dielectric itself.

The Bias Temperature Stress (BTS) test (Chiang and Kaniki, 1996) deals with detrapping and trapping of this charge at an elevated temperature, e.g. at 70°C. A sequence of positive or negative gate-source pulses $\pm V_G$ is applied, with the pulse width as a parameter, while $V_D = 0$ during a given stress time. The measured data in Figure 14.11 shows a larger shift of V_{th} for negative than for positive gate pulses. In each case, the shift increases with the pulse width. A phenomenological explanation is that negative pulses try to empty the traps the more effectively the longer the pulse. The traps are again gradually, but not completely, filled by the intrinsic charge. This results in a lowering of V_{th}. Positive gate pulses fill more of the so far empty traps, resulting in an increase of V_{th}. The gate pulses used for addressing LCDs consist of a sequence of positive and negative pulses with different widths. The superposition of the shifts provides an increase in V_{th}. This increase, measured at an elevated temperature and over a stress time of more than a day, reveals an indication of the life of a TFT under the conditions used in a display.

14.5 Drivers for AMLCDs

The row and column drivers provide the signals (which were discussed in Chapter 13 for PM displays, and in Sections 14.2 and 14.3 for AM displays) to the contact pads. A more detailed discussion will be presented in this section. The next section will be devoted to the processing of the video signal from the picture source to the column drivers.

As a rule, the drivers are ICs placed along the edges of the glass or plastic panel and bonded to the contact pads. Special driver ICs have been developed which require only a narrow stripe along the edges. They are, for example, only 1.8 mm wide, 16 mm long and have 240 pins with a pitch of 64 μm.

The row- or gate-line drivers are shift registers where each stage, as the example in Figure 14.12 shows, provides the gate pulse with a frequency $1/T_f$. The output may include a circuit generating the compensation pulse. The N stages of the shift register generate N pulses in time intervals T_f/N or with a frequency N/T_f. As a rule, the even and odd numbered rows are addressed from different sides in order to double the pitch to more feasible dimensions. Very seldom, the rows are scanned from both sides if the resistance of the line is too high, but the price for double the number of drivers is, as a rule, not acceptable. The video or column driver in Figure 14.13 receives the signals for R, G and B, which are time sequentially stored on capacitors from where the operational amplifiers used as buffer amplifiers drive them as voltage sources into the columns.

In the dual scan driving in Figure 12.9(c), the columns are interrupted in the middle. Hence, we can drive the upper and lower half of the display with $N/2$ lines, each in frame time T_f with half the line address frequency that is with $N/2T_f$. This alleviates the frequency requirements for the line drivers, especially for a large number of N lines and the Pleshko–Alt limits.

A further reduction of frequencies is possible with the block parallel addressing in Figure 14.14. b words (corresponding to b pixels) are stored time-sequentially, at frequency f_1, into shift register A or B, and transferred in parallel to the latch, while the other shift register is filled. The parallel transfer from the latch with frequency $f_2 = f_1/b$ into the b blocks of latches loads the m/b cells of each latch in the time $(m/b)\cdot(1/f_2) = (m/f_1)$, which is the same time as needed for loading m words into the shift register A or B. The number of columns in the display is m; the columns are subdivided into b blocks, with m/b columns each. The storage cells $\nu = 1.2, \ldots, m/b$ in the b blocks feed their content in parallel into the column blocks. While this is happening, a second set of b blocks above the displays, which is not drawn, is being filled with data. The selection of the number b determines by how much the frequency f_1 is decreased. As we shall see later, further processing of the digital

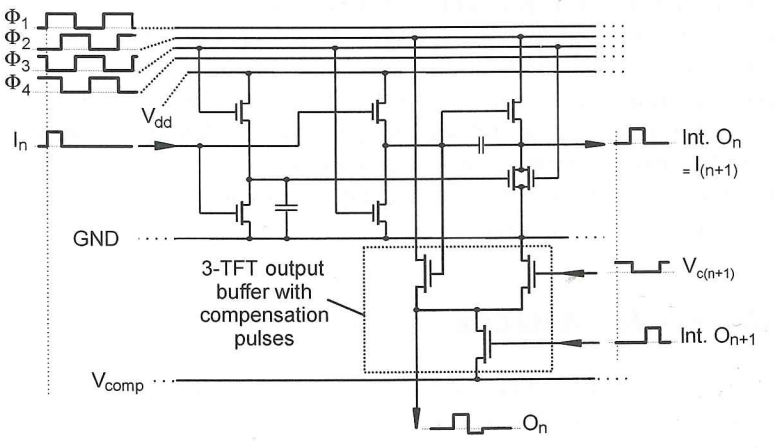


Figure 14.12 Example for one stage of a shift register for the rows of an AMLCD

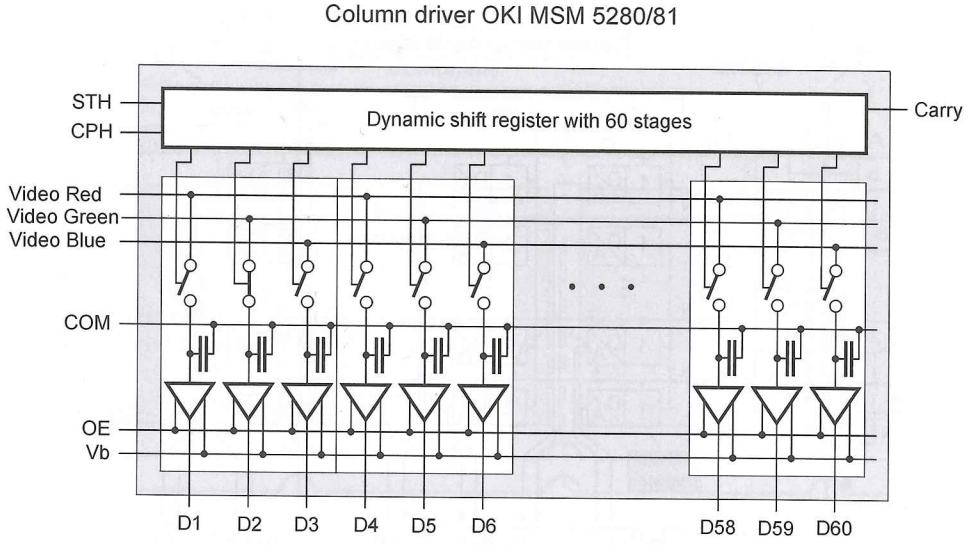


Figure 14.13 A video driver of an AMLCD

words, including D/A-conversion and amplification, can also be performed at the lower frequency f_2.

Since the cost of the addressing circuits is roughly half the cost of an LCD, halving the number of the expensive video drivers in the scheme in Figure 14.15 is most helpful (Sakamoto *et al.*, 1997). The column driver first feeds the video voltage into the pixel of the first column driven in Figure 14.15, and then into those of the second column driven. Only half the number of column lines, but twice the number of rows r_1 and r_2, are necessary. Half the number of column drivers have, time sequentially, to take care of two lines, for which they have to work at double the speed of the conventional approach. Electrically, the pixels became asymmetric because the parasitic capacitive couplings between neighbouring pixels C_R and C_L are unequal. To render them almost equal, a dummy electrode (indicated by a dashed line) has been introduced. This electrode is expected to exhibit the same shielding effect between the pixel as the column line. There are at least two pixel layouts in the panel in Figure 14.15: one with the TFT in the upper portion of the pixel and left of the column, and one with the TFT in the lower portion and right of the column. This results in different gate-source capacitances of the TFTs which, as we know, influence the voltage V_{LC}. The difference in capacitance can be balanced by an additional thin film capacitor C_b in Figure 14.15. With this new driving scheme, power consumption is also decreased by 25 percent, as only half the number of data drivers is used.

A further decrease in power consumption is possible with the power recycling shown in Figure 14.16 (Kim *et al.*, 1997). The largest power consumption occurs for a sign inversion of the voltage from pixel to pixel, because the voltage swing between two adjacent frames is largest. Between two frames the switches between two adjacent columns are closed. This allows the capacitances charged to a negative pixel voltage and those charged to a positive one to discharge, resulting in a common voltage half-way between the previous positive and negative voltages. From there, the capacitances are recharged to the inverted positive and negative voltage of the next frame by the addressing circuit. Hence, power consumption is

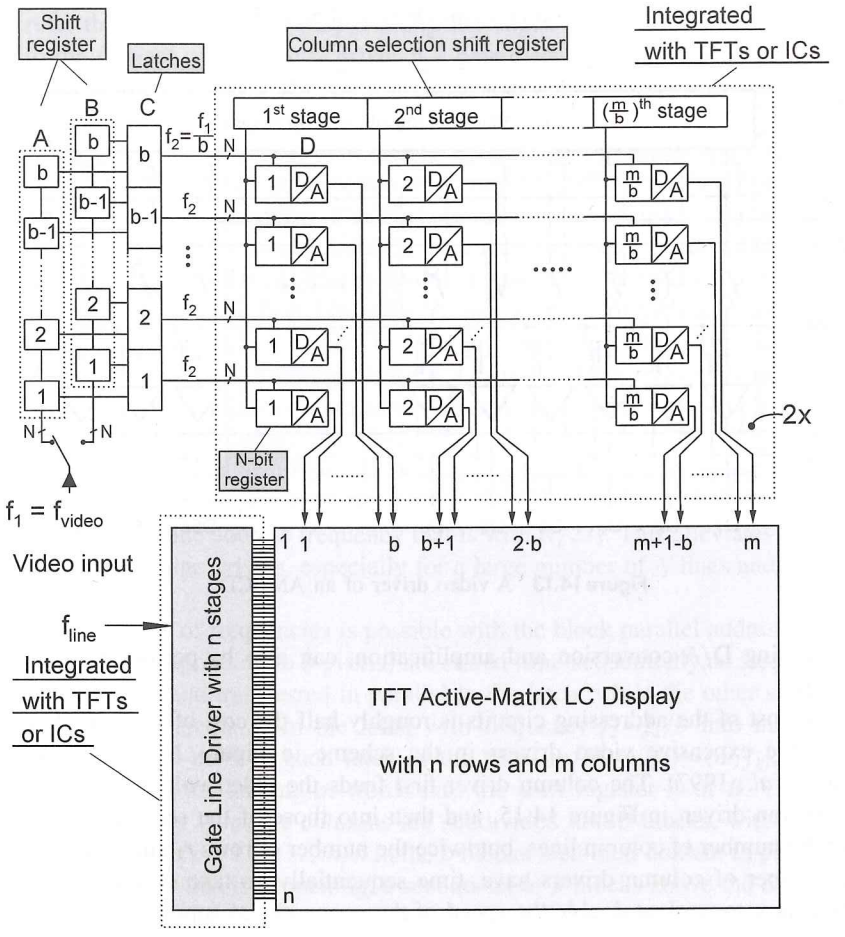


Figure 14.14 Block diagram for block parallel video drivers for an AMLCD

only half of the power consumption encountered if the addressing circuit had to provide the current for the entire recharging of the capacitances.

The maximum voltage swing V_s is with V_{max} in Equation (14.29)

$$V_s = 2\,V_{max}. \tag{14.82}$$

The power consumption of the conventional addressing scheme, with the voltage V_{DD} of the power supply, is

$$P_{conv} = V_{DD}\,I = V_{DD}\left(N\,C_{load}\,V_s \cdot \frac{f_r}{2}\right), \tag{14.83}$$

where N is the number of rows, C_{load} is the total row capacitance and f_r is the frequency of the row driver. For addressing with recycling of charge, the power consumption is

$$P_{recycl} = V_{DD}(N\,C_{load}\,V_s/2 \cdot f_r/2). \tag{14.84}$$

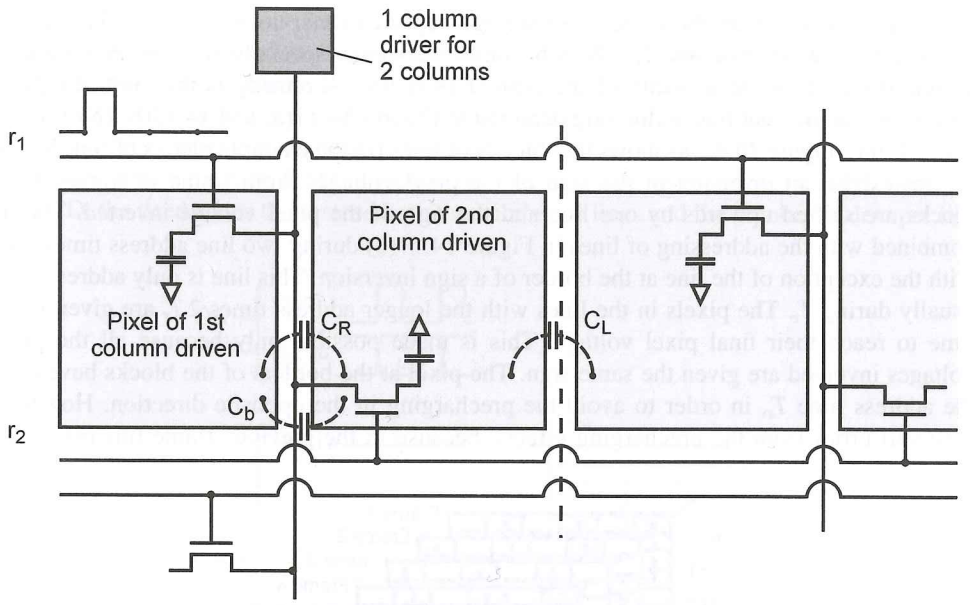


Figure 14.15 Addressing of an AMLCD with half the number of video drivers

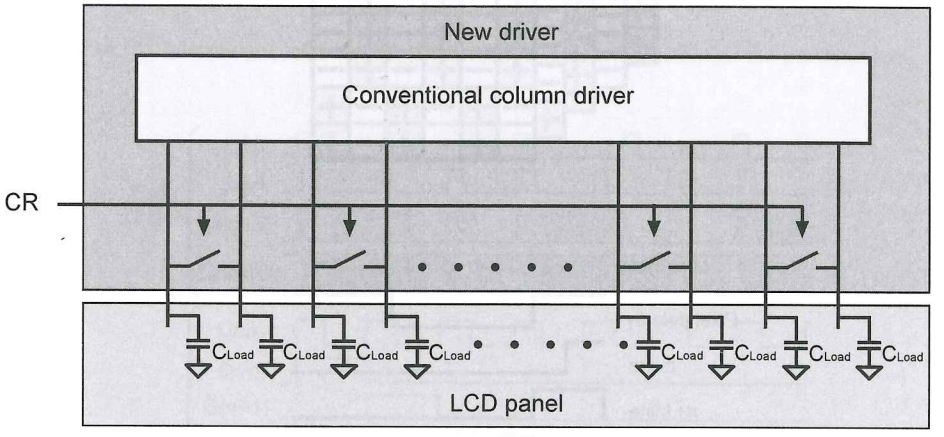


Figure 14.16 Recycling of charge by closing the switches by the control signal CR

For a 50 percent saving of power to be realized, the capacitance $C_{LC}+C_s$ of each pixel has to be discharged to a roughly zero voltage, for which the TFT has to be conductive with a zero drain-source voltage V_D.

A previous solution (Erhart and McCartney, 1997) with similar effect, used a large external capacitance on to which all the pixel capacitances were discharged. A further power reduction can be achieved by combining the charge recycling with the scheme using only half the number of video drivers.

In high resolution displays, the pixel storage capacitors can no longer be fully charged because the row address time $T_r = T_f/N$ becomes too short, especially at lower temperatures around 0°C, where the mobility of the a-Si-TFTs is low. A remedy is the multi-dot pixel inversion and the dual line addressing depicted in Figures 14.17(a) and 14.17(b) (Nishimura *et al.*, 1998). Figure 14.17(a) shows that blocks of lines (in the example blocks of four lines), do not exhibit an inversion of the sign of the pixel voltage. From frame to frame, these blocks are shifted upwards by one line and the sign of the pixel voltage inverted. This is combined with the addressing of lines in Figure 14.17(b) during two line address times $2T_r$, with the exception of the line at the border of a sign inversion. This line is only addressed as usually during T_r. The pixels in the lines with the longer address times $2T_r$ are given more time to reach their final pixel voltage. This is made possible only because all the pixel voltages involved are given the same sign. The pixel at the borders of the blocks have only the address time T_r, in order to avoid the precharging in the opposite direction. However, they still profit from the precharging effects, because in the previous frame this pixel was

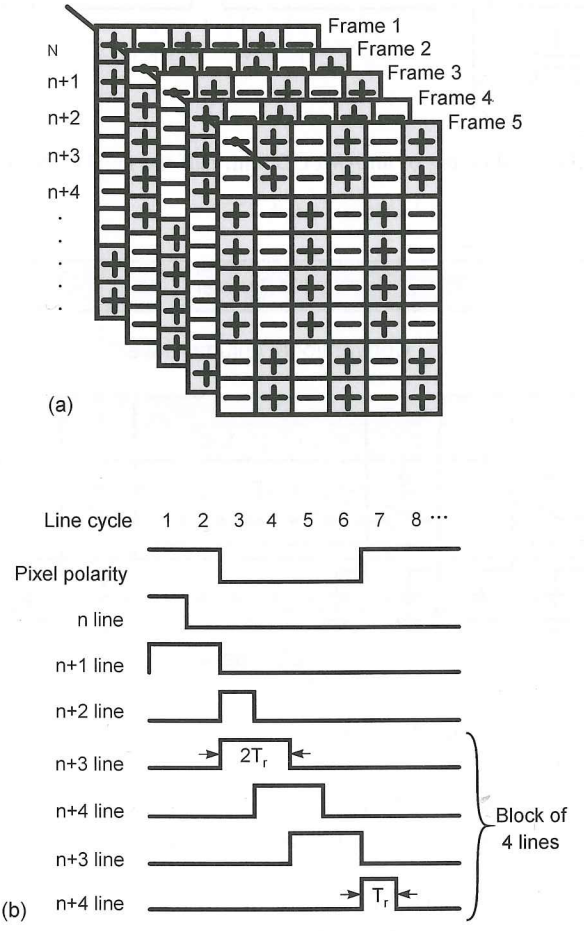


Figure 14.17 (a) Blocks of pixels with the same sign of the voltage V_{LC}; (b) addressing of a line during two row address times

already charged to the inverted polarity. The storage capacitors in a UXGA-LCD were charged only to 94 percent of the desired value when the common addressing scheme was used. The new scheme allowed charging to 99 percent of the desired value, with a beneficial effect on contrast, which reached 150 : 1, with contrast of 10 : 1 extended to 80° in all four directions. The framewise shifting of the block pattern also reduces flicker.

In cases where the format of the picture data has a smaller pixel count than the format of the LCD, the need arises to increase both the number of lines and the number of dots per line

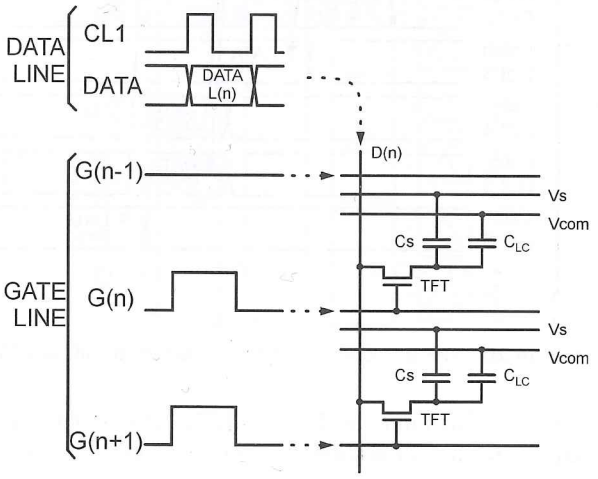


Figure 14.18 Introduction of a second line with the same information as the previous line

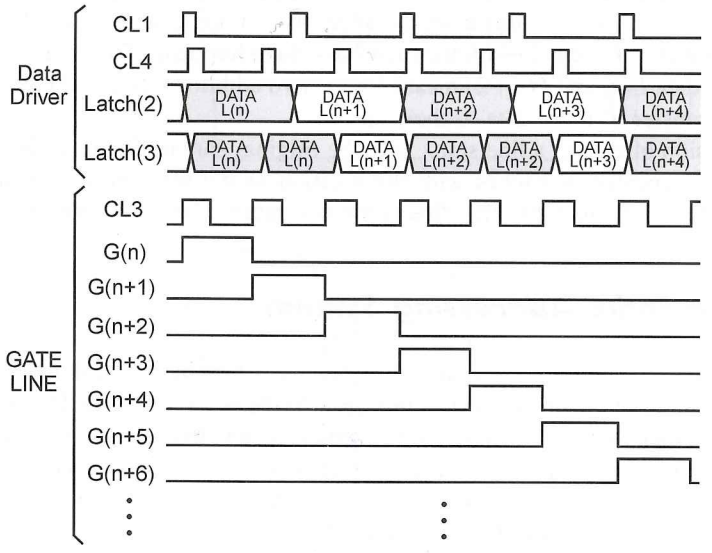


Figure 14.19 The introduction of an additional line if the capacitor C_s in Figure 14.18 is connected to the gate line

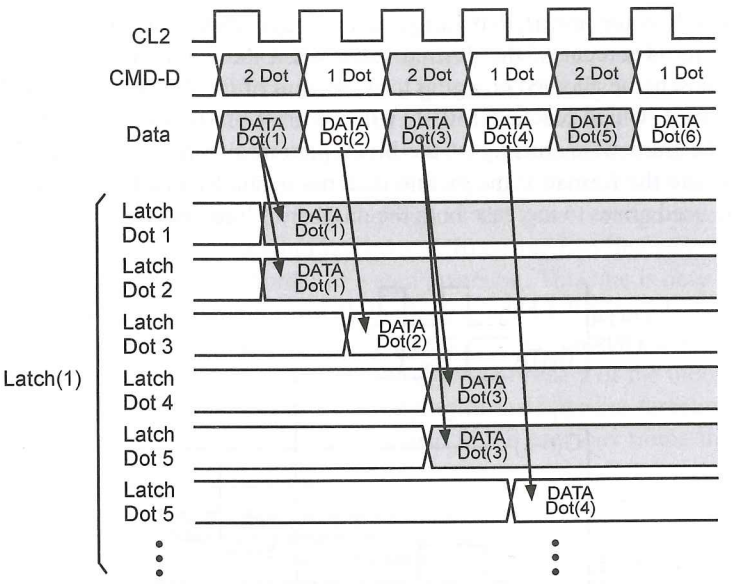


Figure 14.20 The introduction of an additional dot in an LCD

of the data before it can be written into the display. An easy to implement way of introducing two lines with the same information is shown in Figure 14.18, where two lines are scanned simultaneously while the columns feed in the same information in both lines. This works well as long as the storage capacitor C_s in Figure 14.18 has its own electrode V_s. This expansion of the number of lines does not require a line buffer, as did previous approaches. If C_s is connected to the gate line, the two falling edges of the gate pulse couple too large a parasitic voltage onto V_{LC}. In this case, the addition of a line is achieved in Figure 14.19 by writing the content of latch (2) with the increased clock frequency CL4 into latch (3), but by repeating the data $L(n)$ and $L(n+2)$ meant for the two additional lines. The gate pulses $G(\nu)$ achieve the transfer of these data to their lines.

The expansion of dots in a line starts with the original data in Figure 14.20, and transfers the dots to be repeated in latches with the location of the repeated dots underneath each other. A modified timing controller directs the dot data to their respective columns.

14.6 The Entire Addressing System

The entire addressing system in Figure 14.21 (Lauer, 1996) has the task to receive the time sequential data of the picture sources, tailor them to the needs of the LCDs by digital signal processing and then transmit them over to the drivers. The video sources are analog TV, digital TV, digital data from a computer and digital graphic data. The video adapter at the input transforms all analog data using a video decoder, a three-channel amplifier and an A/D converter into the same digital format as the other digital inputs already have. The adapter also matches the data to the format required by the LCD, such as a black and white or colour with vertical or diagonal filter stripes. The colour coding is, as a rule, at most 8-bit. The output R G B, C-Synch serves as monitor for colour and the synchronization pulse. Together with a

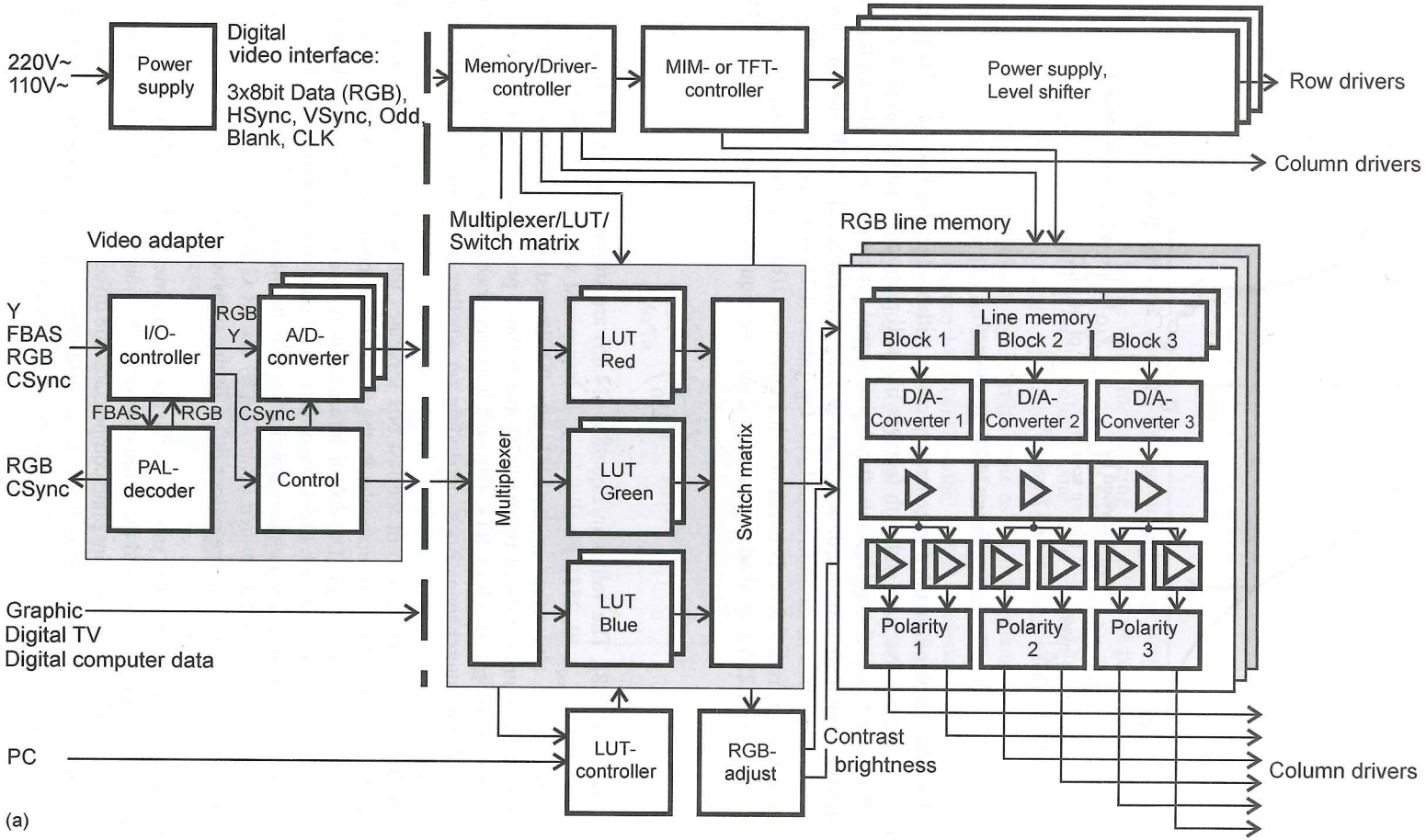
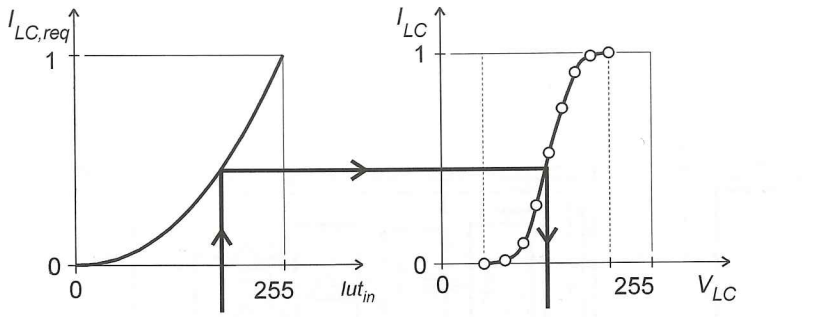


Figure 14.21 (a) The entire addressing system; (b) γ-correction



(b) $$I_{LC,req} = \left(\frac{lut_{in}}{255}\right)^{\gamma_{CRT}}, \quad 2.2 \le \gamma_{CRT} \le 2.8 \qquad (13)$$

Figure 14.21 (continued)

feature box, the adapter is enabled to generate pictures with a selectable half frame frequency, interlaced or progressive scan and with features like still pictures or picture in picture. The digital R G and B signals are fed into the digital signal processing box. The multiplexer translates the sequential incoming data stream into three parallel R-, G- and B-streams, which undergo a γ-correction in the individual Look Up Tables (LUTs) assigned to them. This γ-correction, known from CRTs, is explained in Figure 14.21(b). The luminance lut_{in} of the picture source with 256 grey shades is translated into the required luminance of the LCD

$$l_{\text{LC req}} = \left(\frac{lut_{\text{in}}}{256}\right)^{\gamma_{\text{CRT}}}, \qquad (14.85)$$

with $\gamma_{\text{CRT}} \in [2.2, 2.8]$. The values in Equation (14.85) are stored in the LUT; l_{LCreq} is reduced to values $l_{\text{Lcreq}} \in [0, 255]$. Finally, l_{LCreq} is transposed with the measured luminance-pixel voltage curve, also stored in the LUT, into the desired pixel voltage V_{LC}. After this procedure, the colours exhibited by the LCD match those produced by the internationally defined colours co-ordinates for CRTs. The switch matrix or commutator at the output of the digital signal box interchanges lines, depending on whether progressive or interlaced addressing is used.

The RGB line latch (memory) of the last box separates the write- and read-frequencies. One line latch consecutively receives the R, the G and the B colour information of one line as prepared by the commutator. The colour information is read out in block parallel format, starting with the first data in each block, then the second data in each block, etc. To do this, we need two line latches, of which one is written while the other is read out. After the D/A conversion, all channels are amplified controlled by the 'R G B adjust' to the same brightness. The two video signals at the output differ in the sign, which is used for frame-, line- and column-wise sign inversion.

The memory driver controller supervises the operation times of the line latches, the commutation, the D/A conversion and the column drivers. The line controller supervises the gate pulses; the level shifter for the front plate compensates the offset of V_{LC}, caused by the drop of the gate pulse. The outputs of the polarity stages feed into the video drivers in Figure 14.12, while the row drivers in Figure 14.11 are connected to the power supply in the level shifter.

14.7 Layouts of Pixels with TFT Switches

The performance of a display depends strongly upon the layout of the pixels. Key features are a large enough aperture ratio A, defined in percent for a transmissive display as

$$A = \frac{\text{transmissive area of a pixel}}{\text{total area of a pixel}} 100\%, \tag{14.86}$$

which produces high brightness and a large enough storage capacitor C_s for holding the information during the frame time, for reducing the effect of parasitic capacitive coupling in Equation (14.18) to the pixel voltage, and for shielding the pixel against detrimental couplings from pulses travelling on the columns and rows. For a reflective display, the word 'transmissive' in Equation (14.85) should be replaced by 'reflective'. The increased C_s and the shielding, as a rule, diminish the aperture ratio, as the materials used are not transparent. It is up to the designer to find an ingenious solution benefiting all criteria.

The basic pixel layout in Figure 14.22(a) (Lueder, 1998a) possesses a column made of Al or Cr-Al-Cr, which is insulated from the rows made of Cr or Mo-Ta. The rows are widened in the region of the storage capacitor C_s, which has a dielectric of SiO_2 or Si_3N_4 and an upper electrode of Al or ITO. This placement of C_s leaves more space for the ITO electrode, thus enhancing the aperture ratio to, as a rule, 65 percent. The a-Si TFT requires only about

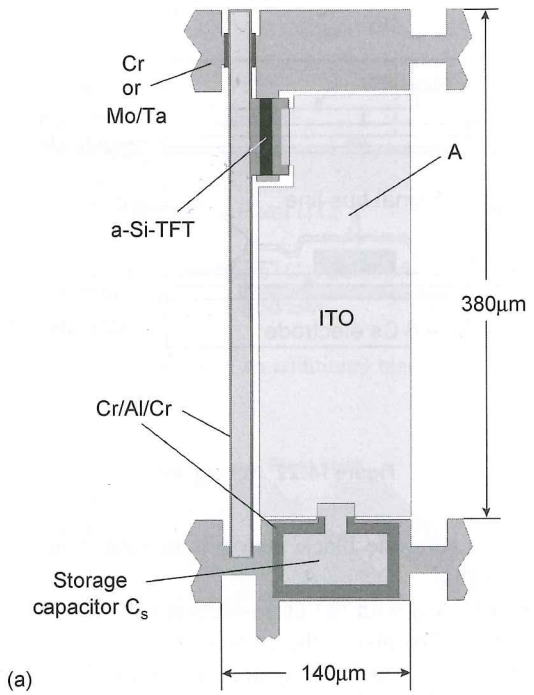


Figure 14.22 (a) Basic pixel layout of an AMLCD; (b) pixel layout with storage capacitor along the edges of the ITO-electrode; (c) cross-section along the line A–A′ in Figure 14.22(b)

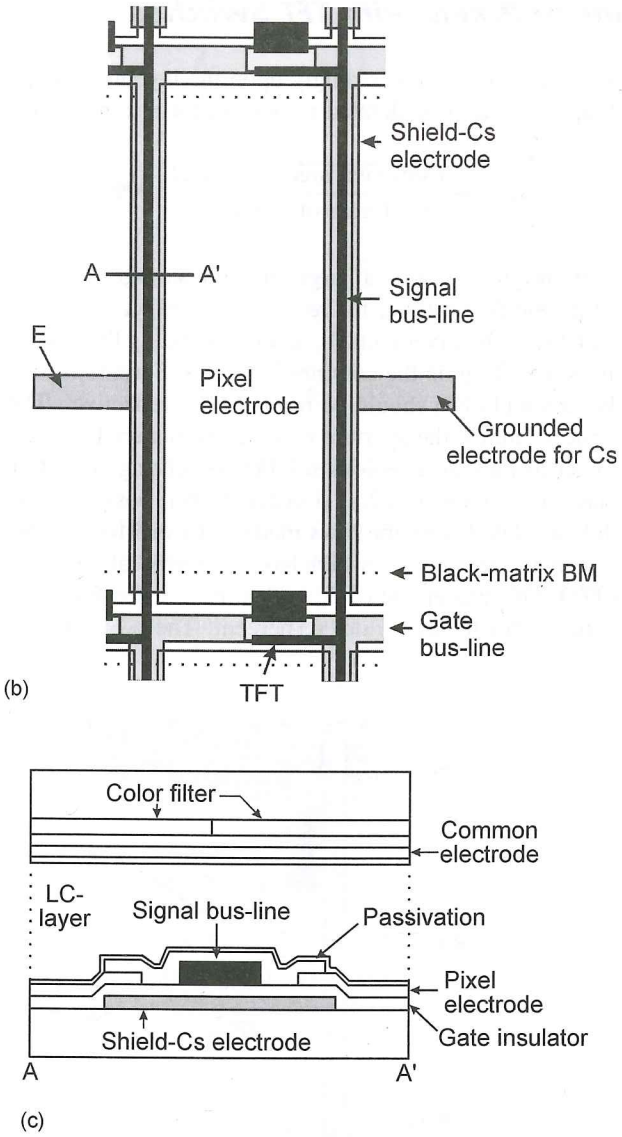


Figure 14.22 (continued)

2 percent of the area. As a rule, the black matrix is deposited on the opposite glass plate together with the colour filter.

The layout in Figure 14.22(b) with the cross-section in Figure 14.22(c) (Kitazawa *et al.*, 1994; Suzuki, 1994; Kim, 1996) places the capacitor C_s along the edges of the ITO electrode. Most importantly, it is shielded against crosstalk by a shield electrode. This electrode in Figure 14.22(c), from Mo-Ta, also serves as an additional black matrix layer. Furthermore, C_s is no longer connected to the gate-line, but has its own transparent ITO electrode E in Figure 14.22(b), not shown in the cut $A-A'$ in Figure 14.22(c). Hence C_s and,

as a consequence, V_{LC} is no longer affected by the pulses on the former bottom electrode of C_s. There is, however, still the downward shift of V_{LC} stemming from the gate pulse coupled in through the gate-source capacitance C_{GS}. The black matrix BM on the active matrix plate has the beneficial effect of blocking the oblique light beam O from the backlight, shown in the cross-section of the pixel depicted in Figure 14.23. Without the BM on the active matrix plate, backlight would be transmitted in the direction shown by the dashed arrow. Further advantages of the additional BM are the shielding of the imperfectly controlled LC stripe along the edge of the ITO electrode, and the introduction of the overlap of the two BMs in the range w, allowing for small misalignments of the two glass plates (Kim, 1996).

Figure 14.24 shows schematically some layers of a pixel in which the storage capacitor C_s is completely placed underneath the ITO pixel electrode (Maier, 1997). For a transmissive pixel, all layers have to be transparent, which is satisfied by the ITO bottom and pixel electrodes and the Si_3N_4 dielectric, which is also used as gate dielectric. The electric field from the neighbouring column ends mostly on the extended bottom electrode, resulting in a shielding of the capacitor C_s. The completed pixel layout with the light shield omitted is shown in Figure 14.25. C_s possesses the large value of 200 fF on an area of 1300 μm^2, with a thickness of 400 nm, which helps to diminish all effects of the parasitic couplings.

The pixel layout for a reflective cell drawn in Figure 14.26(a) (Egelhaaf *et al.*, 2000) shows that the entire pixel apart from the interpixel gap is covered by an Al mirror, yielding

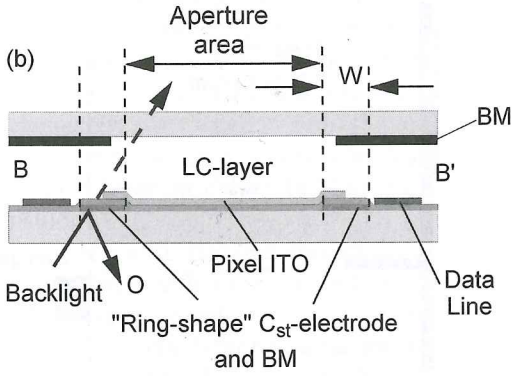


Figure 14.23 Cross-section of a pixel with an additional black matrix on the active matrix plate

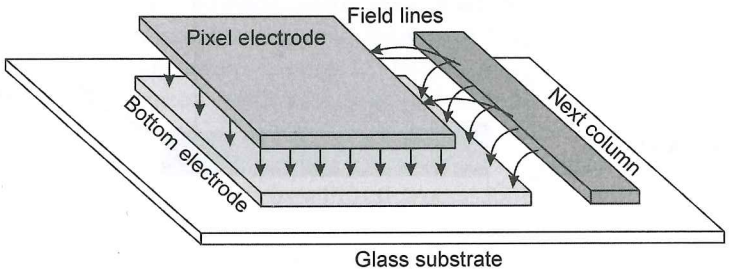


Figure 14.24 Pixel with the storage capacitor underneath the pixel electrode

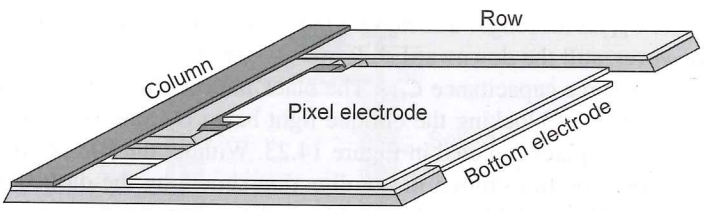


Figure 14.25 A pixel with C_s underneath the ITO electrode

a 92.6 percent aperture ratio. The TFT, the storage capacitor, the rows and columns are all underneath the mirror, as depicted in the cross-section in Figure 14.26(b). The column is shielded by a grounded electrode, preventing capacitive coupling of the video pulses onto the pixel voltage.

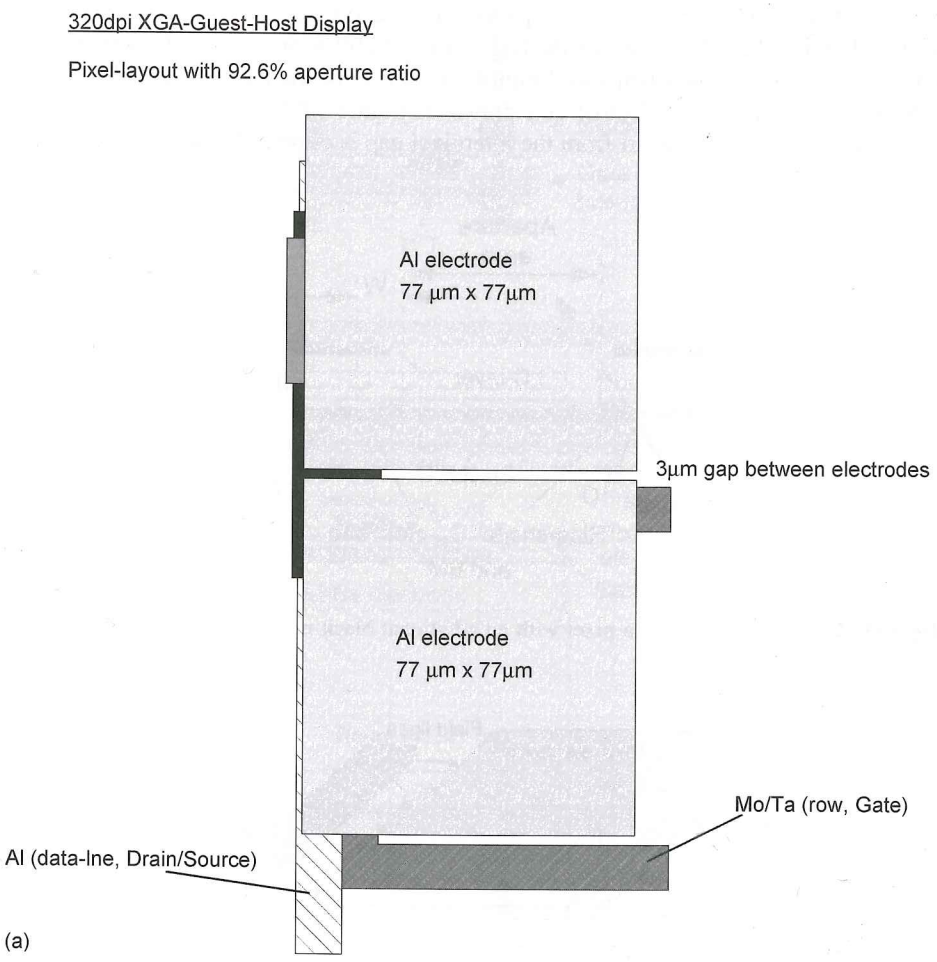


Figure 14.26 (a) The top view of a pixel in a reflective display with a mirror, which also covers the rows and columns; (b) cross-section of the pixel in Figure 14.26(a)

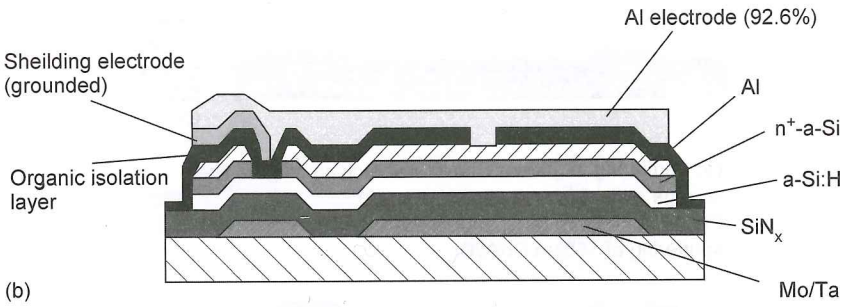
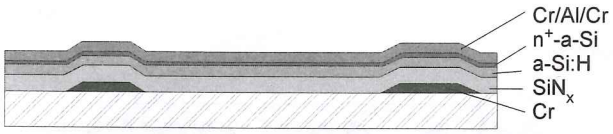


Figure 14.26 (continued)

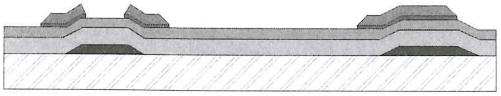
14.8 Fabrication Processes of a-Si TFTs

A criterion for the usefulness of a TFT fabrication process is a low mask count, presently in the range of 4 to 6. The rationale behind this is that a small number of mask alignments and a small number of processing steps associated with a small mask count is synonymous with an economic process. This is, however, only true if the low mask count does not narrow the process window, and still allows for a high fabrication yield. Furthermore, a small number of masks is only acceptable if it does not degrade the performance of the display.

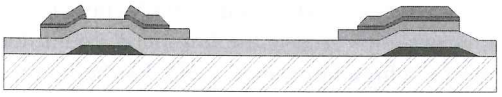
Figure 14.27 depicts the sequence of fabrication steps involved in a four mask fabrication of bottom gate a-Si TFTs (Glueck *et al.*, 1994; Lueder, 1994c). After a glass substrate (e.g. 0.7 mm thick) has been chemically cleaned in an ultrasonic bath, a 200 nm Cr- or Mo/Ta layer is sputtered and chemically wet etched to form the rows, the gate electrodes and the bottom electrode of the storage capacitor. The patterning shown in Figure 14.27(a) requires the first mask. The next three layers in Figure 14.27a are deposited by [Plasma Enhanced Chemical Vapour Deposition (PECVD)]. They are Si_3N_4 as gate dielectric and as the dielectric for C_s, intrinsic a-Si : H (i-a-Si : H) as semiconductor and n^+-a-Si as a layer providing an ohmic contact for drain and source. In the semiconductor, dangling bonds are neutralized by H, which enhances the electron mobility to values from 0.5 cm^2/Vs to 1 cm^2/Vs. This mobility of the amorphous Si layer is still far below the mobility of monocrystalline Si-FETs reaching more than 500 cm^2/Vs. Finally, a Cr/Al/Cr- or Mo/Ta layer is sputtered and chemically wet etched in Figure 14.27(b) to form the pattern for the drain and source electrode and the top electrode of C_s. For this, the second mask is required. The pattern of the Cr/Al/Cr serves as a mask for plasma etching of n^+-a-Si in Figure 14.27(b). As plasma etching also attacks a-Si, an end point control is required by watching the edging time or by monitoring the plasma emission at 204.4 nm stemming from CF and SiF radicals. This back channel etch is the most subtle step, as it has to remove all n^+-a-Si residues while leaving an a-Si-layer with a homogeneous thickness of around only 50 nm. This small thickness off current below 1 pA. A second plasma etch is required to reduce the using a third mask in Figure 14.27(c) removes i-a-Si : H, forming the i-a-Si islands for the TFTs. The sputtering and patterning of the ITO pixel electrode by a lift-off process, or preferably by plasma etching in Figure 14.27(d), requires the fourth mask. Finally, a PECVD passivation layer of SiN_x requires a fifth mask for opening the bond pads, whereas the deposition of a metallic light shield on top of the array uses a sixth mask. The two last masks do not have to be aligned as precisely as the others, and as a rule are not counted as yield-determining masks.



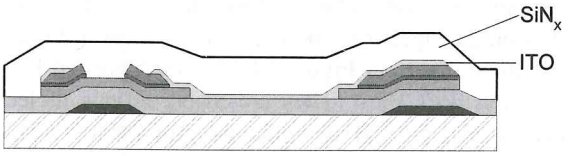
(a) Sputtering of 200nm Cr and wet-etching as gate line, storage capacitor and gate; *(1st mask)*
PECVD of 400nm SiN_x, 130nm i-a-Si and 50nm n^+-a-Si; sputtering of 150nm Cr/Al/Cr



(b) Wet etching of Cr/Al/Cr as source line, drain/source metallization, top electrode of storage capacitor; *(2nd mask)*
plasma-etching of n^+-a-Si with Cr/Al/Cr as etch mask with end point control



(c) Plasma-etching of i-a-Si:H forming a-Si-islands for TFT *(3rd mask)*



(d) Sputtering and patterning of 80nm ITO as pixel electrode and column redundancy; lift-off *(4th mask)*
PECVD of 350nm SiN_x as passivation;
opening of the passivation at the bond pads
not very accurate 5th mask light shield (6th mask)

Figure 14.27 The process steps for a four mask fabrication of a-Si : H TFTs

The ultimate in mask count is a two mask process, such as that depicted and explained in Figure 14.28 (Miyata *et al.*, 1998). An interesting feature is the self-aligned generation of the channel in Figure 14.28(c) by exposing the photoresist OFPR-800 from underneath using the Cr gate as a shadow mask. The ITO used for the pixel electrode is also applied as drain and source electrodes, which saves a mask. The last step is the back channel etch of n^+-a-Si. An improvement of the ITO electrodes for the TFT (Ban *et al.*, 1996) consists of introducing a doped microcrystalline Si-layer (μc–Si : H (n^+)) instead of n^+-a-Si : H, which enhances the mobility of a TFT with ITO contacts above 0.5 cm^2/Vs. A further two-mask process (Richou *et al.*, 1992) does not generate a-Si islands for the TFTs, and isolates the TFTs having a guard ring around them.

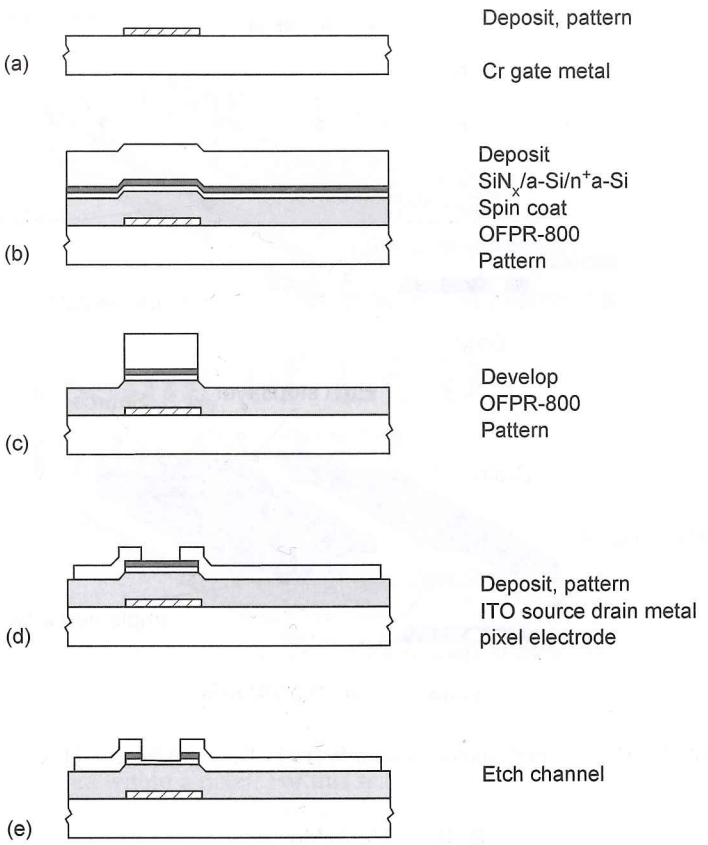


Figure 14.28 A two-mask fabrication of a-Si : H TFTs

An n^+-doped layer is formed in the a-Si: TFT in Figure 14.29(a) by implanting P ions through an etch stop layer, using Mo-layer as a stopping layer (Maier *et al.*, 1997). After deposition and etching of the Mo source and drain electrodes, which were used before as a stopping layer, we obtain the TFT in Figure 14.29(b). This process has the advantage that back channel etch is not required, and that the i-a-Si semiconductor is, throughout the manufacture, protected by the etch stop layer. The stopping layer has the task of placing a large concentration of the dopant at the surface of the i-a-Si-layer. The process requires an implanter for large areas (Eaton Corp., 1997).

A technological breakthrough was the introduction of Cu with a specific resistance of only 2 $\mu\Omega$cm for conductors and gates into AMLCDs, providing a low enough resistance for rows and columns of large area displays (Fryer *et al.*, 1996). Cu had previously been virtually forbidden in Si semiconductor devices, due to its reaction with Si. Furthermore, it does not adhere well to glass, and is difficult to contact to other metals. Figure 14.30 shows a cross-section of an a-Si TFT with a copper gate (Fryer *et al.*, 1996). The lowermost layer on glass is ITO, which is used as a pixel electrode, as an adhesion layer for the copper gate and as a contact bridge to copper without exposing the Cu to other metals. The configuration in Figure 14.30 does not require back channel etching, because after deposition of i-a-Si : H by PECVD an SiN_x layer was deposited and etched to only having an SiN_x protection film on top of the

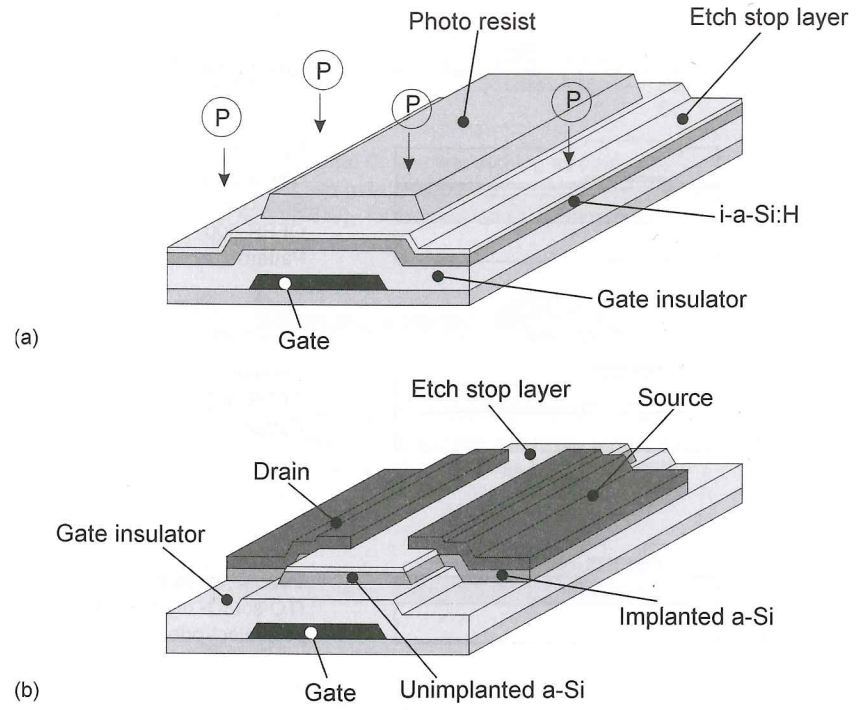


Figure 14.29 (a) The ion-implantation of an a-Si : H TFT and (b) the completed a-Si : H TFT

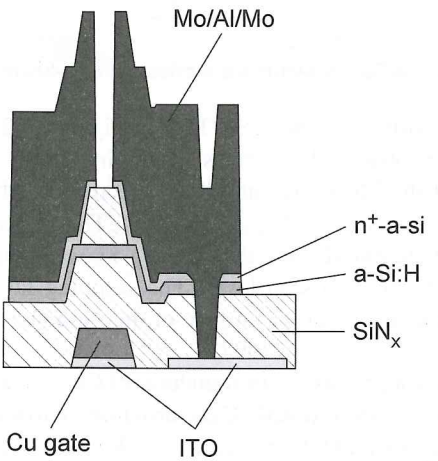


Figure 14.30 Cross-section of an a-Si:H TFT with a copper gate

channel. Then, only an n^+-a-Si : H-layer is generated, and etched off on top of the channel, as shown in Figure 14.30. This eliminates the subtle etching of n^+-a-Si : H on top of a-Si : H, and protects the a-Si : H channel by a dielectric. A via hole is necessary to connect the Mo/Al/Mo source to the ITO.