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(54) **DATA STORAGE APPARATUS WITH IMPROVED SECURITY PROCESS AND PARTITION ALLOCATION FUNCTIONS**

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(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(51) **Int. Cl.^{7}** **G06F 12/00**
(52) **U.S. Cl.** **711/164**; 711/173; 714/200; 714/202
(58) **Field of Search** 711/152, 151, 711/173, 163, 164, 112; 710/261, 264, 36, 28; 709/225; 713/200, 201, 202; 705/18

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(57) **ABSTRACT**

The apparatus enables access authorization to be assigned solely to specific host devices. A control device comprises: an address registration unit, in which the host address of each host device has been registered for authorizing access, a command interpretation and execution unit which on receipt of a command from a host device via a host device interface outputs the host address of the host device based on the command, and an address verification unit for verifying the host address output from a command interpretation and execution unit against the host address registered in the address registration unit, as well as determining whether or not the particular host device has access authorization. The command interpretation and execution unit incorporates an authorization pending function, so that on receipt of a command from a host device, the command is interpreted and executed only after access is authorized by the address verification unit.
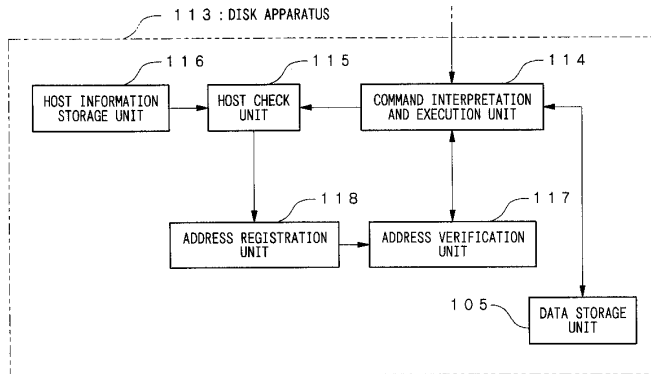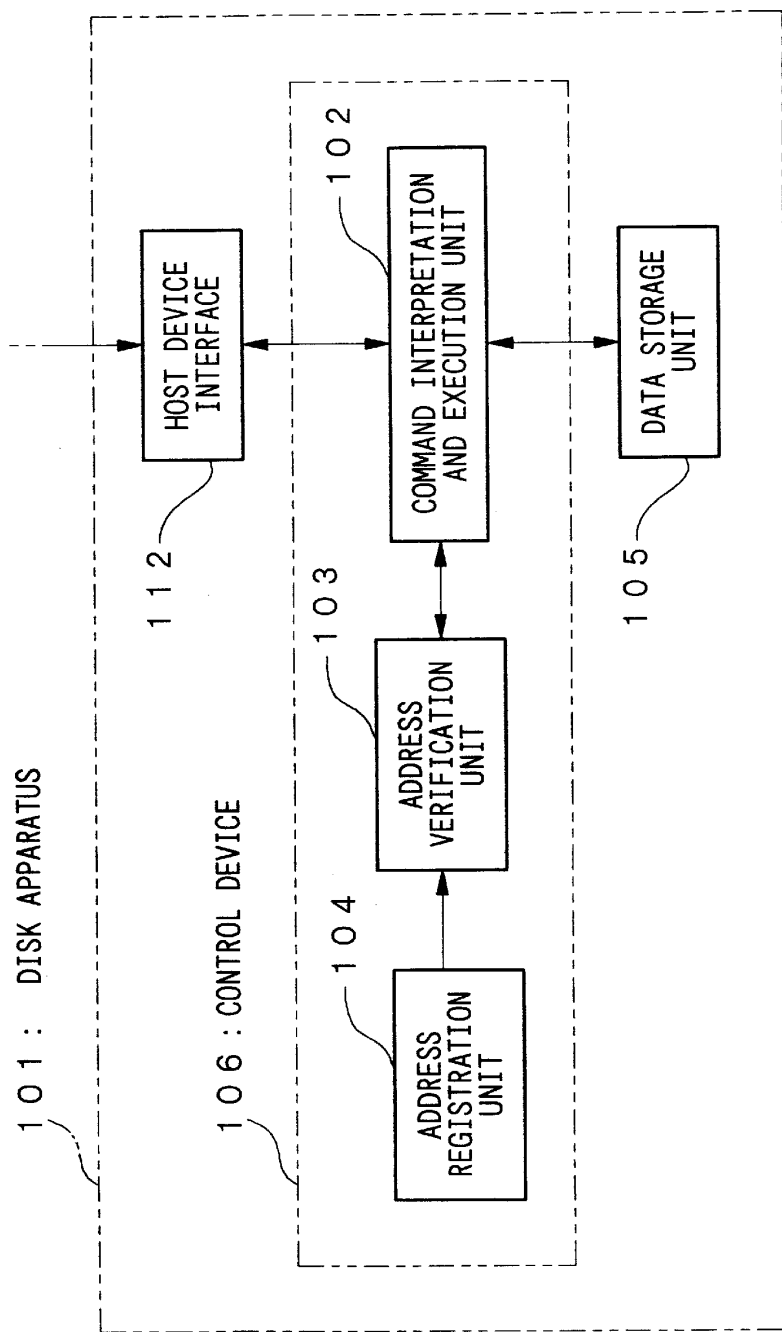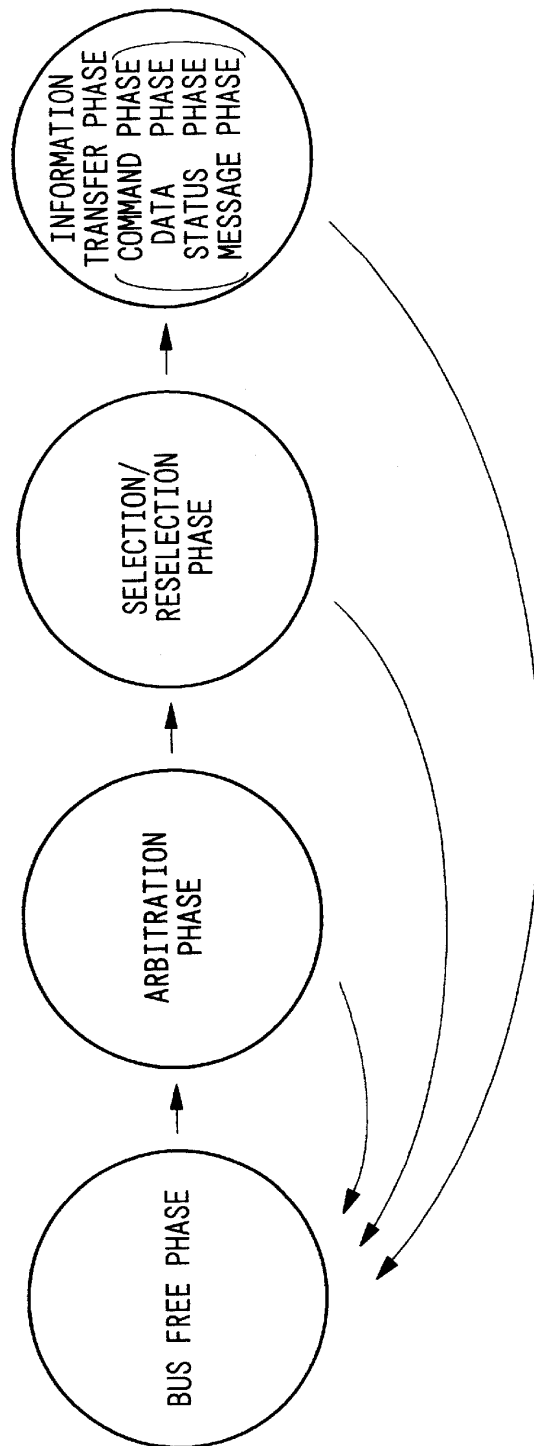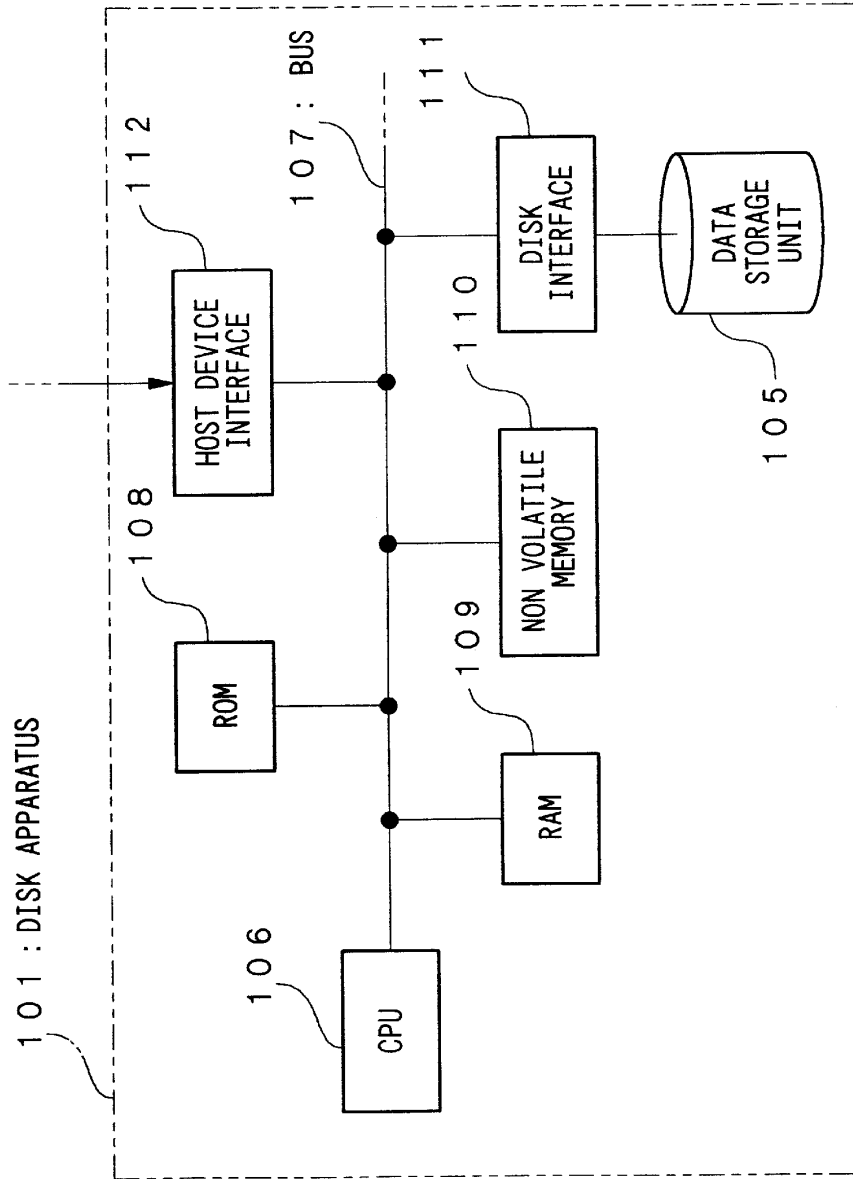
5 Claims, 5 Drawing Sheets

FIG.1

101: DISK APPARATUS

106: CONTROL DEVICE

112   HOST DEVICE INTERFACE

102   COMMAND INTERPRETATION AND EXECUTION UNIT

105   DATA STORAGE UNIT

103   ADDRESS VERIFICATION UNIT

104   ADDRESS REGISTRATION UNIT

FIG.2

INFORMATION
TRANSFER PHASE
COMMAND PHASE
DATA PHASE
STATUS PHASE
MESSAGE PHASE

SELECTION/
RESELECTION
PHASE

ARBITRATION
PHASE

BUS FREE PHASE

FIG.3

101 : DISK APPARATUS

112

107 : BUS

111

HOST DEVICE INTERFACE

DISK INTERFACE

DATA STORAGE UNIT

108

110

105

ROM

NON VOLATILE MEMORY

109

106

RAM

CPU

FIG.4

113 : DISK APPARATUS

116 HOST INFORMATION STORAGE UNIT

115 HOST CHECK UNIT

114 COMMAND INTERPRETATION AND EXECUTION UNIT

118 ADDRESS REGISTRATION UNIT

117 ADDRESS VERIFICATION UNIT

105 DATA STORAGE UNIT

DOCKET ALARM
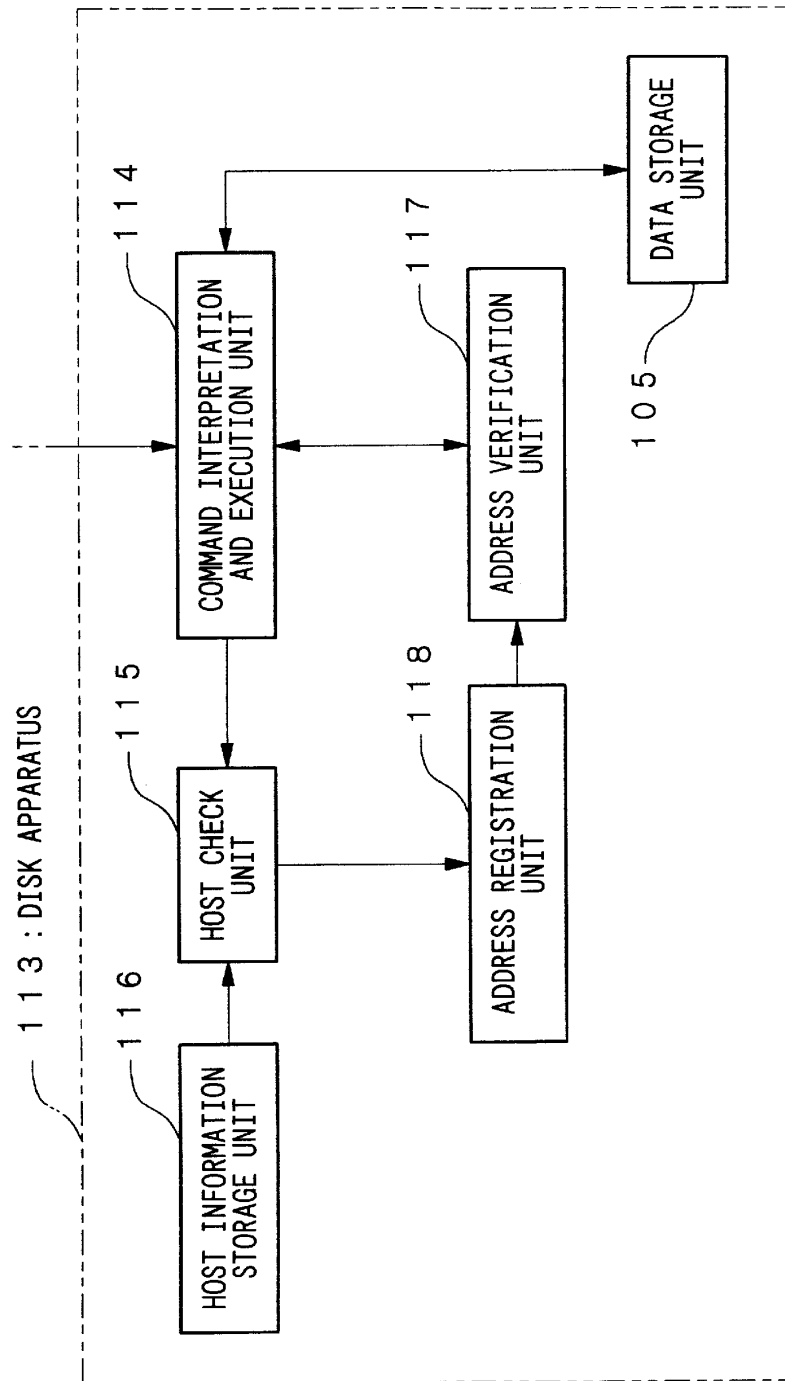
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