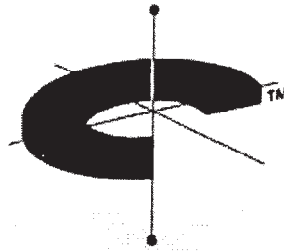


Verrazano

Fibre Channel to SCSI bridge
Revision 1.1



CROSSROADS

Crossroads Systems Inc.

Verrazano Software Architecture

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1. Introduction

This document provides the architectural details for the Verrazano Bridge and gives an overview of the methods, processes, and requirements involved in the software development effort. It is meant to provide the basic guidelines for development, and as such is subject to change as the implementation evolves.

2. Overview

2.1 Product Hardware Description

The target hardware is an embedded system centered around the Intel i960RP processor. Incorporated on the i960 bus are program memory, flash memory, and a serial UART. The secondary PCI bus from the i960RP will have an HP Tachyon Fibre Channel controller, using the Interphase TPI PCI interface, and 4MB DRAM for data buffering. This DRAM will interface to this PCI bus via a custom interface designed in house. The secondary PCI bus will also have the Symbios 53C875 PCI SCSI controller. The 960RP primary PCI bus will have an AMD 10BaseT Ethernet controller.

Specific details of the hardware architecture and design can be found in the Verrazano Requirements Document, and in the Verrazano Strategic Specification.

2.2 Prototype Description

To accelerate software development and to allow for software development to be overlapped with hardware development, a PC based prototype platform will be used. Functionally, the PC will be used for the PCI bus and system memory. The host processor will not be used except for limited debugging purposes. The processor used will be the Intel Cyclone board with the i960JX processor module. This will have 4MB of DRAM for program memory. The PLX 9060 PCI bridge on the Cyclone will allow for interfacing the 960 processor to the FC and SCSI devices over the PCI bus. The Fibre Channel interface will be the Interphase Tachyon based PCI adapter. The SCSI interface will be the Symbios SYM53C875 PCI adapter. Serial communication, flash memory, and other basic functionality is provided by the Cyclone board.

This provides an architecturally similar platform using essentially identical core components for development. Porting to the Verrazano hardware platform will require changes limited to the PCI bridge, memory and device mapping, and serial and other peripheral interfaces. The core driver and bridge code will remain unchanged.

2.3 Design Philosophy

- 'C' Code base
- Modular design
- Pass-through, event driven architecture
- Use Existing OS, Drivers, Protocol Stacks as possible
- Design for performance, future portability, maintainability

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3. Core Software Modules

3.1 Boot Code

At system boot, code will be required to initialize the hardware, perform basic system testing, and load the runtime code. The expectation is that this will consist in large part of modules available from Intel (mon960) and the runtime OS (VxWorks). Portions of this code will be modified and extended to support hardware specific characteristics which are TBD.

Requirements:

- Initialize hardware
- Run Power On Self Test
- Set Processor, PCI address mapping
- Initialize and start VxWorks, core software

3.2 Diagnostics

In addition to the power on self test code executed at boot time, further diagnostics will be required for manufacturing test, field diagnosis, and returned unit test. These tests should be more extensive than the POST, and should include tests for all major subsystems of the Verrazano board. Diagnostics should be accessible from the serial console, TELNET via Ethernet, and SNMP via Ethernet. Future extensions should include accessibility via SCSI and Fibre Channel via FC-IP.

Requirements:

- One base test suite is desired, covering:
 - Manufacturing Test
 - Field Test
 - Return Unit Test
- Processor test
- Memory test
- PCI test
- Buffer memory test
- Tachyon test - internal loop back, electrical (GLM) wrap, external loop back
- Symbios test - internal loop back, external loop back
- Ethernet adapter test - internal loop back, external loop back

3.3 Kernel

Currently VxWorks from Wind River Systems is the targeted runtime OS. Future ports may be targeted for IxWorks.

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