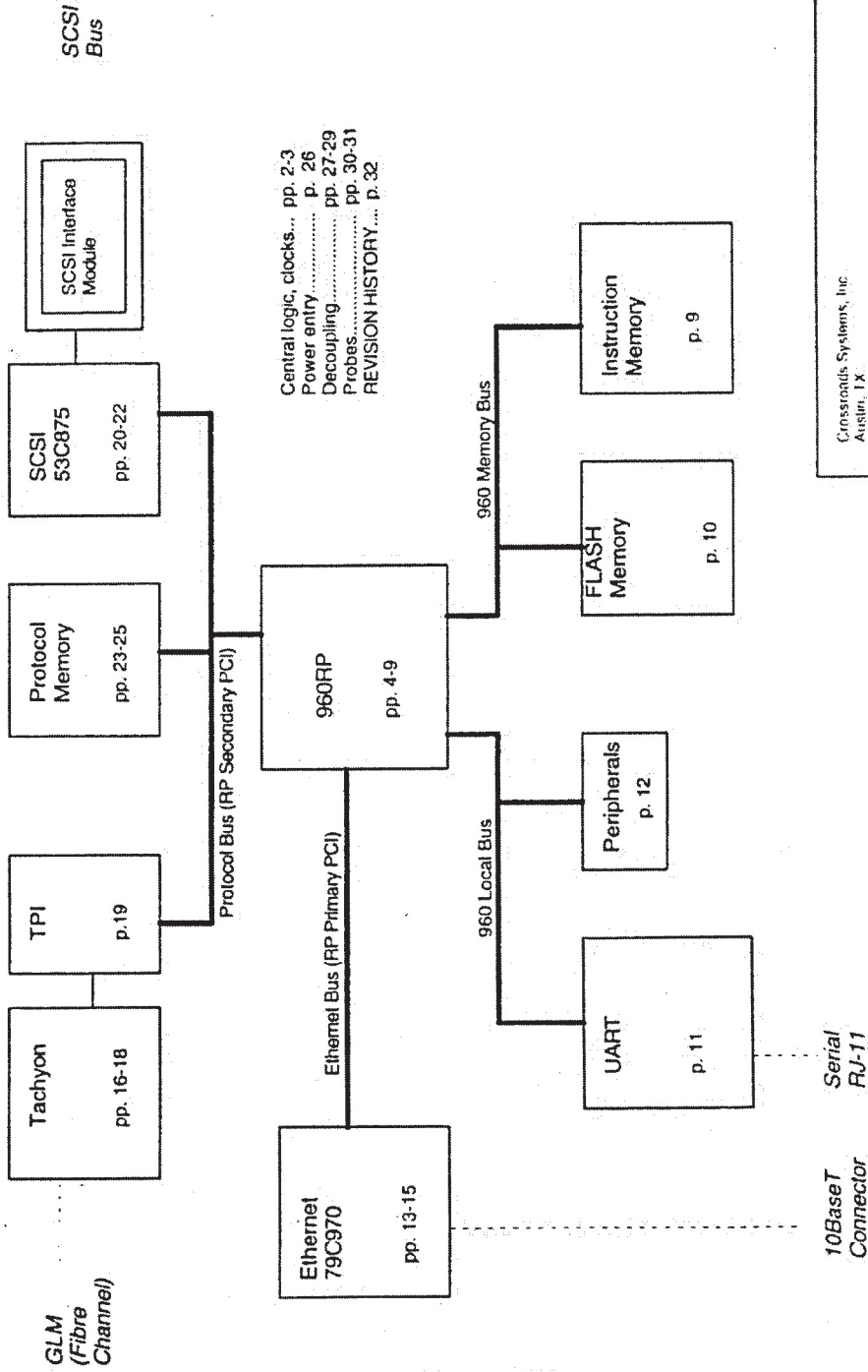


file: \\homed\jerry\Adm\Tech\Bial\Verrazzo and board - main\verrazzo board - m3.ppt (1,357 KB; 2/13/1997)

Verrazzo: System Structure

Board assembly p/n = AD90010



Central logic, clocks... pp. 2-3
 Power entry..... p. 26
 Decoupling..... pp. 27-29
 Probes..... pp. 30-31
 REVISION HISTORY... p. 32

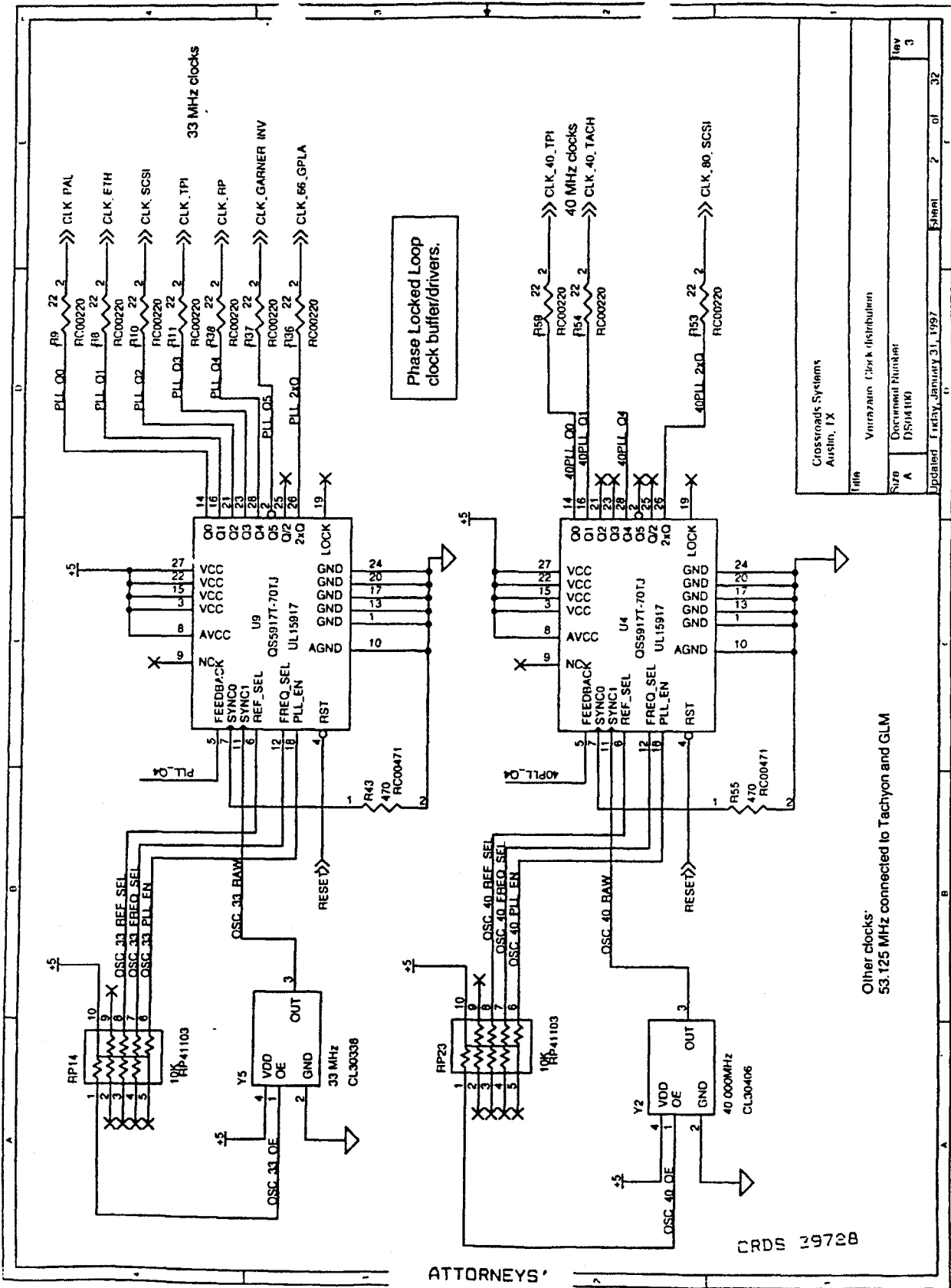
ATTORNEYS' EYES ONLY

CRDS 39727

Crossroads Systems, Inc Austin, TX	
File#	Verrazzo final design
Size	Document Number
A	15904100
Printed	Wednesday, January 22, 1997
Page	1 of 32

PLAINTIFF'S EXHIBIT
 A-00-CA-217-88

EXHIBIT
 4 - loose
 9-19-00

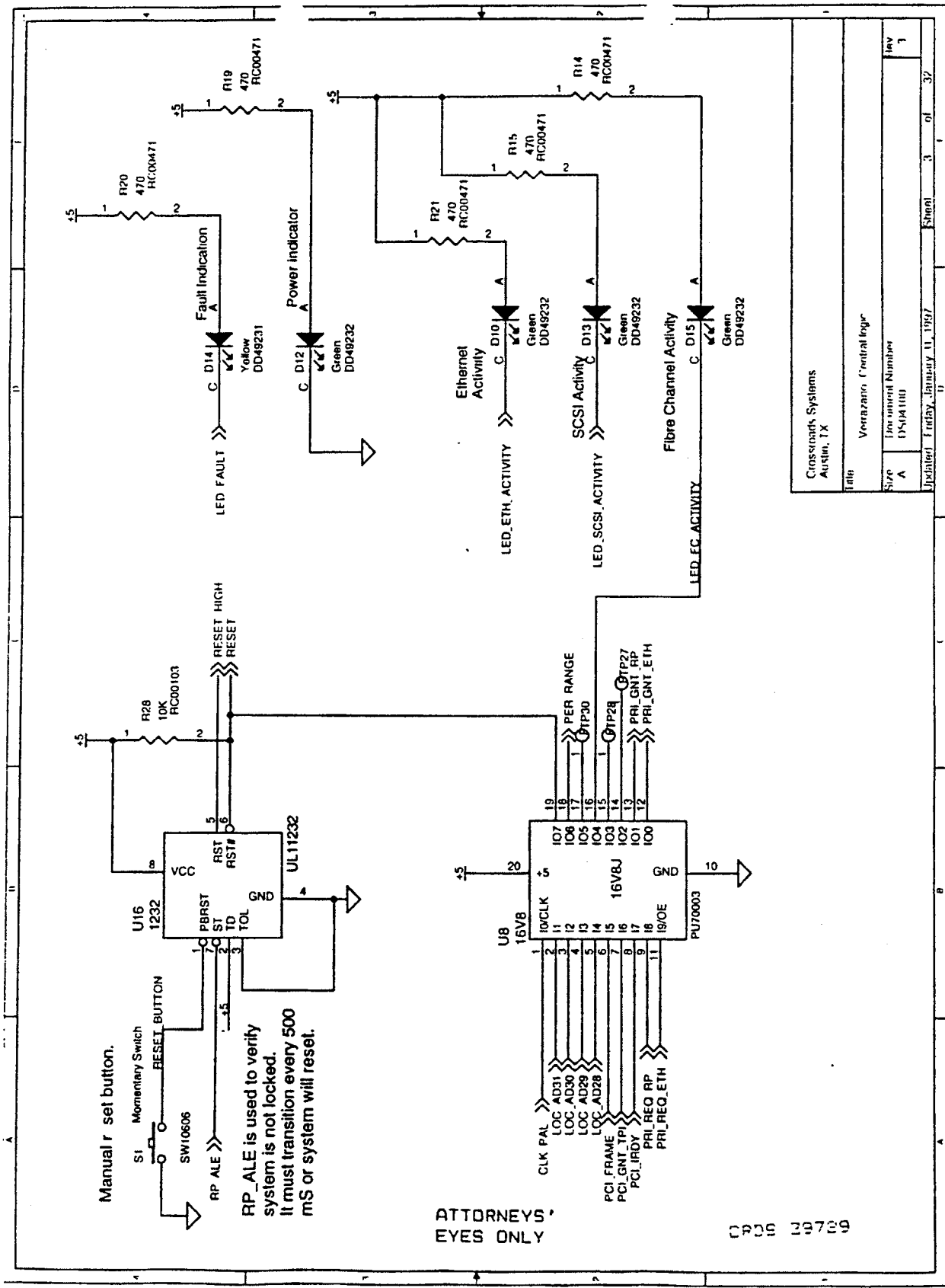


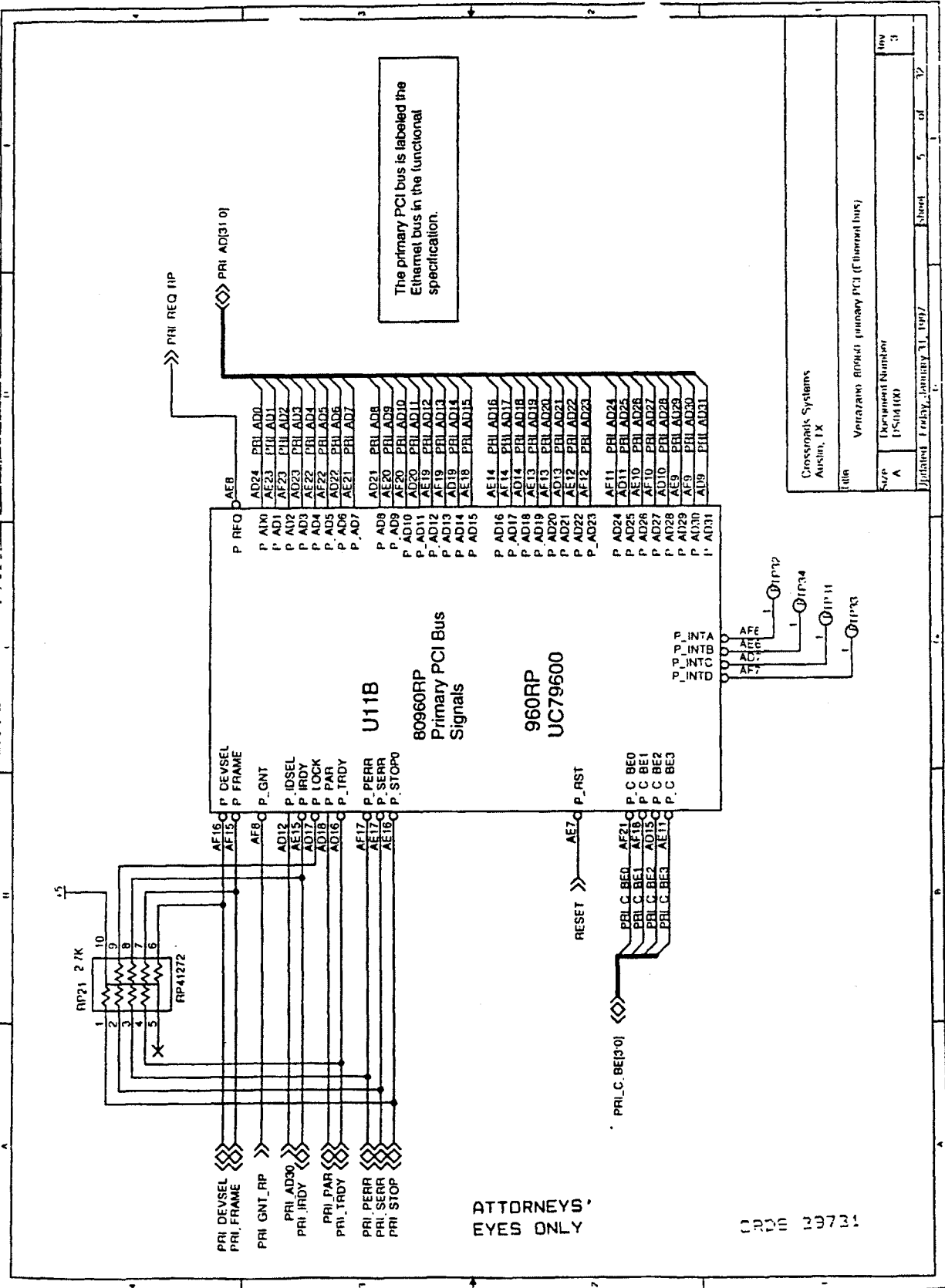
ATTORNEYS' EYES ONLY

CRDS 29728

Other clocks:
53.125 MHz connected to Tachyon and GLM

Crossroads Systems Austin, TX	
Title	Vincenzan Clock distribution
Size	A
Document Number	DS04100
Updated	Friday, January 31, 1997
Sheet	2 of 32
Rev	3





The primary PCI bus is labeled the Ethernet bus in the functional specification.

Crossroads Systems Austin, TX	
Title: Vertarano 80960 primary PCI (Ethernet bus)	
Size: A	Document Number: P504100
Rev: 3	Update: Friday, January 31, 1997
Sheet 5 of 12	

ATTORNEYS' EYES ONLY

0320 23731

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