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Verrazano

Verrazano Software Development

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1. Introduction

This document gives an overview of the methods, processes, and requirements involved in the software development effort for the Verrazano Bridge. It is meant as an overview intended to provide the basic guidelines for development, and as such is subject to change as the implementation evolves.

2. Overview

2.1 Product Hardware Description

The target hardware is an embedded system centered around the Intel i960RP processor. Incorporated on the i960 bus are program memory, flash memory, a serial UART, and a 10baseT Ethernet controller. The primary PCI bus from the i960RP will have an HP Tachyon Fibre Channel controller, using the Interphase TPI PCI interface, and 2MB DRAM for data buffering. This DRAM will interface to the PCI bus via a custom interface designed in house. The secondary PCI bus will have the Symbios 53C875 PCI SCSI controller.
Specific details of the hardware architecture and design can be found in the Verrazano Requirements Document, and in (hardware design documents, schematics, Jeff's whiteboard)

2.2 Prototype Description

To accelerate software development and to allow for software development to be overlapped with hardware development, a PC based prototype platform will be used. Functionally, the PC will be used for the PCI bus and system memory. The host processor will not be used except for limited debugging purposes. The processor used will be the Intel Cyclone board with the i960JX Squall module. This will have 2MB of DRAM for program memory. The PLX 9060 PCI bridge on the Cyclone will allow for ·· -facing the 960 processor to the FC and SCSI devices over the PCI bus. The Fibre Channel interface w. he Interphase Tachyon based PCI adapter. The SCSI interface will be the Symbios SYM53C875 PCI a...ter. Serial communication, flash memory, and other basic functionality is provided by the Cyclone board.
This provides an architecturally similar platform using essentially identical core components for development. Porting to the Verrazano hardware platform will require changes limited to the PCI bridge, memory and device mapping, and serial and other peripheral interfaces. The core driver and bridge code will remain unchanged.

2.3 Design Philosophy

- 'C' Code base
- Modular design
- Pass-though, event driven architecture
- Use Existing OS, Drivers, Protocol Stacks as possible
- Design for performance, future portability, maintainability

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3. Core Software Modules

3.1 Boot Code

At system boot, code will be required to initialize the hardware, perform basic system testing, and load the runtime code. The expectation is that this will consist in large part of modules available from Intel (mon960) and the runtime OS (currently VxWorks). Portions of this code will be modified and extended to support hardware specific characteristics which are TBD.

Requirements:

- Initialize hardware
- Run boot diagnostics
- Set Processor, PCI address mapping
- Initialize and start VxWorks, core software

3.2 Diagnostics

In addition to the power on self test code executed at boot time, further diagnostics will be required for manufacturing test, field diagnosis, and returned unit test. These tests should be more extensive than the POST, and should include tests for all major subsystems of the Verrazano board. Diagnostics should be accessible from the serial console, TELNET via Ethernet, and SNMP via Ethernet. Future extensions should include accessibility via SCSI and Fibre Channel via FC-IP.

Requirements:

- One base test suite is desired. covering:
  - Manufacturing Test
  - Field Test
  - Return Unit Test
- Processor test
- Memory test
- PCI test
- Buffer memory test
- Tachyon test - internal loopback, electrical (GLM) wrap, external loopback
- Symbios test - internal loopback, external loopback
- Ethernet adapter test - internal loopback, external loopback

3.3 Kernel

Currently VxWorks from Wind River Systems is the targeted runtime OS. Future ports may be targeted for IxWorks.

3.4 FC Driver

The Fibre Channel driver will be based on the current ICS FC DDK. Modifications may be made to the initialization and FC-4 layers. The interfaces to this code will be defined in section 4.2 of this document.

The FC driver provides the following functionality:

- Manage logins and logouts
- Manage FC-4 exchanges
  - Activation of new exchange for each FCP command
  - Manage FCP command(exchange) through all phases for that command
  - Provide means for FC-4 to do process login for an FCP attached device
  - Receive all FC-4 data commands
- Manage exchanges
  - Activation and Deactivation of exchanges
  - assignment of X_ID
- Manage sequences
  - Initiation and termination of sequences
  - SEQ_ID assignment
  - Managing sequence initiative
- Manage EE credit
- All FC-2 functionality

3.5 SCSI Driver

The SCSI driver will consist of two parts. The SCSI state machines will be implemented in the Symbios SCRIPTS language, which runs on the 875 internal processor. This code will interface with a higher layer interface running on the i960 processor. The interfaces to this code will be defined in section 4.3 of this document.

The SCSI driver provides the following functionality:

- Provide SCSI initiator support with a single SCSI ID
  - Manage Commands and Messages to targets
  - Manage DMA to/from buffer memory
- Provide SCSI target support
  - Respond to multiple target IDs
  - Process Commands and Messages
  - Manage DMA to/from buffer memory
- Manage all SCSI bus phases and transitions
- Manage Synchronous, wide, and fast negotiation

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