Trials@uspto.gov
571-272-7822

Paper 14
Entered: July 21, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ATOPTECH, INC.,
Petitioner,

v.

SYNOPSYS, INC.,
Patent Owner.

Case IPR2015-00760
Patent 6,237,127 B1

Before TRENTON A. WARD, PETER P. CHEN, and FRANCES L. IPPOLITO, *Administrative Patent Judges.*

IPPOLITO, *Administrative Patent Judge.*

DECISION
Denying Petitioner's Motion for Joinder
and Denying Institution of *Inter Partes* Review
37 C.F.R. §§ 42.108, 42.122

I. INTRODUCTION

Petitioner Atoptech, Inc. filed a Petition (Paper 1, "Pet.") to institute an *inter partes* review of claims 5 and 6 of U.S. Patent No. 6,237,127 B1 (Ex. 1001, "the '127 patent"). On the same day, Petitioner also filed a Motion for Joinder, requesting joinder of this proceeding with a related and instituted proceeding, IPR2014-01145. Paper 3 ("Joinder Motion"). Petitioner filed its Joinder Motion within one month after institution of a trial in IPR2014-01145, as required by 37 C.F.R 122(b). Patent Owner Synopsys, Inc. filed a Preliminary Response to the Petition. Paper 13 ("Prelim. Resp."). Patent Owner also filed an Opposition to Petitioner's Motion for Joinder (Paper 9, "Opp. To Joinder"), and Petitioner filed a Reply to Patent Owner's Opposition to Motion for Joinder (Paper 11, "Reply").

We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if "the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a).

For the reasons below, we determine that Petitioner has not shown that joinder is warranted in this instance. We also deny the Petition and do not institute *inter partes* review as to claims 5 and 6 of the '127 patent.

A. Related Proceedings

The '127 patent is involved in a district court proceeding in the U.S. District Court for the Northern District of California captioned *Synopsys, Inc. v. ATopTech, Inc.*, Case No. 3:13-cv-02965-MMC (N.D. Cal. 2013). Pet. 1–2.

Additionally, on July 11, 2014, Petitioner filed a Petition ("First Petition") to institute an *inter partes* review of claims 1–13 of the '127 patent in IPR2014-01145. On January 21, 2015, we instituted an *inter partes* review in IPR2014-01145 of claims 1–4 and 7–11 of the '127 patent. Case IPR2014-01145, slip op. at 25 (PTAB Jan. 21, 2015) (Paper 7) ("the '1145 Decision"). In that Decision, we denied Petitioner's request for *inter partes* review of claims 5, 6, 12, and 13 of the '127 patent. *Id.* Subsequently, Petitioner filed its Petition in the instant proceeding on February 18, 2015, challenging claims 5 and 6 of the '127 patent.

B. The '127 Patent

The '127 patent relates generally to the static timing analysis of digital electronic circuits, and in particular applies static timing analysis to synthesis of circuits by analyzing certain paths of a circuit using "non-default timing constraints known as exceptions." Ex. 1001, Title, 1:8–11. Exceptions allow a circuit designer, working with a circuit synthesis system, to specify certain paths through the circuit to be synthesized as being subject to non-default timing constraints. *Id.*, Abstract. The '127 patent discloses that static timing analysis had been used to verify that the design of a digital electronic circuit would perform correctly at the target clock speeds, and "[f]or similar reasons, it would be useful to apply, as efficiently as possible, static timing analysis to the synthesis process." *Id.* at 1:40–42. Specifically, the '127 patent discloses performing static timing analysis on units of a circuit, referred to as "sections," which comprise a set of "launch" flip flops, non-cyclic combinational circuitry, and a set of "capture" flip flops. *Id.* at 2:1–4.

The static timing analysis described in the ’127 patent is accomplished in two main phases: (1) propagation of tagged rise-fall (RF) timing tables and (2) relative constraint analysis. Ex. 1001, 8:37–41. In the first phase of the timing analysis, delays between inputs and outputs of circuit devices are represented by “timing arcs.” Ex. 1001, 8:44–45. Using the timing arcs for the circuit devices, maximum and minimum delay values for the rise time and the fall time are determined and stored in RF timing tables. *Id.* at 9:54–67. The timing tables are propagated through the circuit and the delays at each circuit node are added to the minimum and maximum values of the timing table from the previous node. *Id.* at 9:58–13:2, Fig. 5. Additionally, each timing table is associated with a “tag” that may include clock identifier and a variety of “labels.” Ex. 1001, 3:11–15, 10:21–25. The labels of a “tag” also may identify points in the circuit referenced by an exception. *Id.* at 3:29–32.

After the propagation of the timing tables through the circuit, the second phase of the timing analysis, relative constraint analysis, is performed. *Id.* at 13:3–4. Relative constraint analysis involves the comparison of the delay values included in the timing tables with the timing constraints of the circuit. *Id.* at 13:66–14:27. The ’127 patent describes maximum allowable path delays (MAPDs) and shortest allowable path delays (SAPDs), which are default timing constraints alterable by exceptions. *Id.* at 13:34–63, 14:30–38. The delay values stored in the timing tables are compared to the MAPD and SAPD values, and if the MAPD and SAPD timing constraints are satisfied, the circuit has passed the static timing analysis. *Id.* at 13:56–14:26.

Additionally, with respect to exceptions, the '127 patent instructs "[e]xceptions are specified by the circuit designer as individual syntactic units called 'exception statements' which are comprised of a 'timing alteration' and a 'path specification.'" Ex. 1001, 1:58–61. The timing alteration instructs the timing analyzer how to alter the default timing constraints for paths through the circuit to be analyzed which satisfy the path specification. *Id.* at 1:61–63. For example, a "set_false_path" exception indicates that for paths satisfying the path specification, the relevant MAPD value is set to infinity and the relevant SAPD value is set to zero for the relative constraint analysis. *Id.* at 14:47–54.

II. DECISION ON THE MOTION FOR JOINDER

A. Background

The statutory provision governing joinder of *inter partes* review proceedings is 35 U.S.C. § 315(c), which reads as follows:

> (c) JOINDER.—If the Director institutes an inter partes review, the Director, in his or her discretion, may join as a party to that inter partes review any person who properly files a petition under section 311 that the Director, after receiving a preliminary response under section 313 or the expiration of the time for filing such a response, determines warrants the institution of an inter partes review under section 314.

Section 315(b) of the statute generally bars institution of *inter partes* review when the petition is filed more than one year after the petitioner (or petitioner's real party in interest or privy) is served with a complaint alleging infringement of the patent. 35 U.S.C. § 315(b); 37 C.F.R. § 42.101(b). That one-year time bar, however, does not apply to a request for joinder. 35 U.S.C. § 315(b) (final sentence); 37 C.F.R. § 42.122(b). This is an important consideration here because Petitioner was served with a complaint

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.