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Craven et al.

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(45) **Date of Patent: May 22, 2001**

(54) **STATIC TIMING ANALYSIS OF DIGITAL ELECTRONIC CIRCUITS USING NON-DEFAULT CONSTRAINTS KNOWN AS EXCEPTIONS**

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(51) **Int. Cl.**[7] **G06F 17/50**; G06F 1/04; G06F 1/06; G06F 1/08

(52) **U.S. Cl.** **716/6**; 703/2; 703/15; 703/19; 716/1; 716/3; 716/5; 716/7; 716/2; 713/500

(58) **Field of Search** 703/2; 716/2, 1, 716/3, 5, 6, 7; 713/500

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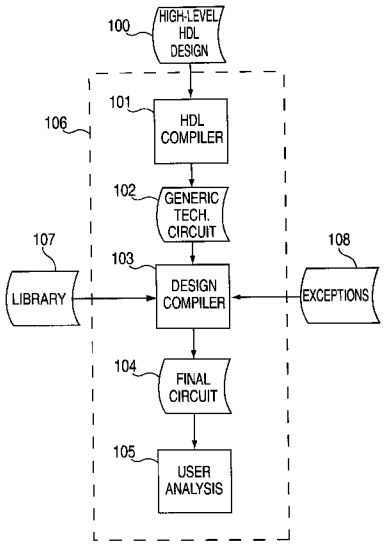
(57) **ABSTRACT**

Exceptions allow a circuit designer, working with a circuit synthesis system, to specify certain paths through the circuit to be synthesized as being subject to non-default timing constraints. The additional information provided by the exceptions can allow the synthesis system to produce a more optimal circuit. A tag-based timing analysis tool is presented, which implements exceptions, and can be used in a synthesis system. A circuit is analyzed in "sections," which comprise a set of "launch" flip flops, non-cyclic combinational circuitry and a set of "capture" flip flops. The tag-based static timing analysis of the present invention is performed in four main steps: preprocessing, pin-labeling, RF timing table propagation and relative constraint analysis. Preprocessing converts the exceptions written by the circuit designer into a certain standard form in which paths through the circuit to be synthesized are expressed in terms of circuit "pins." Pin-labeling causes the particular circuit pins, which are the subject of exceptions, to be marked. During RF timing table propagation, "RF timing tables" with rise and fall times are propagated onto all pins of the circuit section. Rise and fall times in the RF timing tables are based on "timing arcs" describing the delay characteristics of each of the state (flip flop) and combinational (logic gate) devices. Each RF timing table has a tag which indicates: i) a launch flip flop clock, and ii) the exception pins through which the RF timing table has propagated. During relative constraint analysis, each RF timing table at the input to a capture flip flop is analyzed for meeting certain relative constraints. These relative constraints may be either defaults, or the defaults may be modified according to an exception satisfied by the contents of the RF timing table's tag.

13 Claims, 22 Drawing Sheets



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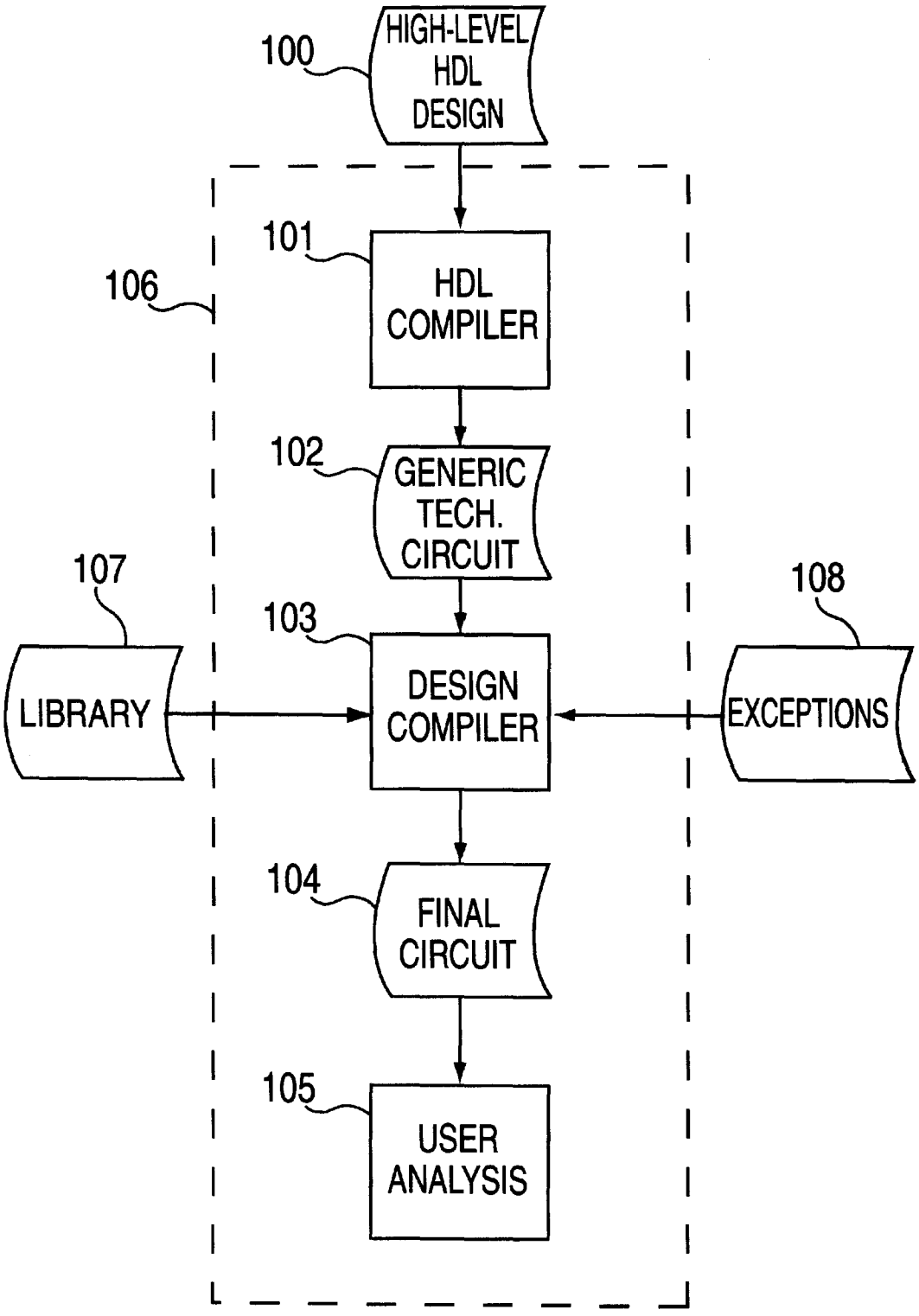

FIG. 1

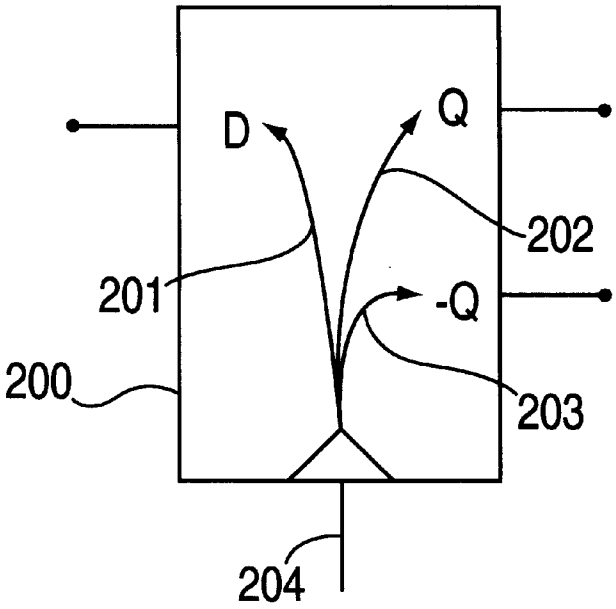

FIG. 2A

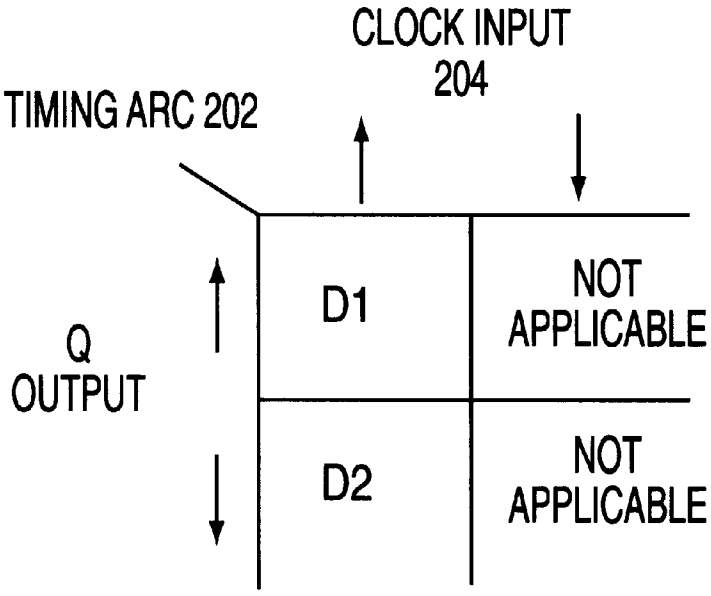

FIG. 2B

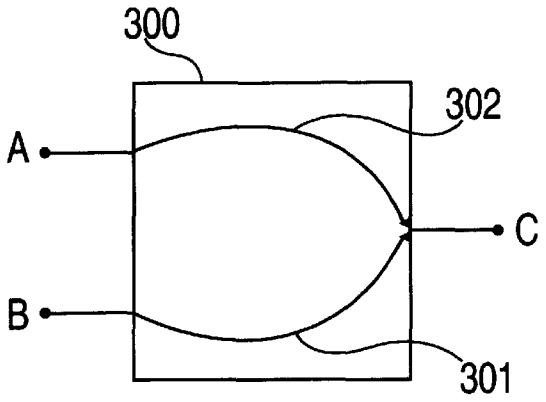

FIG. 3A

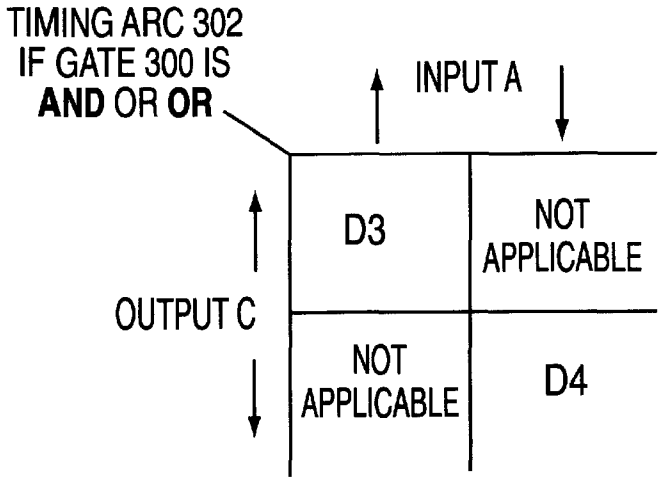

FIG. 3B

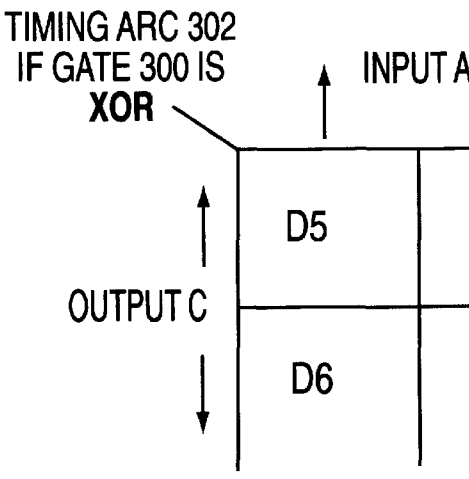

FIG. 3C

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