Keynote Paper

A Perspective on the Reliability of MEMS-Based Components for Telecommunications

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ABSTRACT

Despite the initial skepticism of OEM companies regarding reliability, MEMS-based devices are increasingly common in optical networking. This presentation will discuss the use and reliability of MEMS in a variety of network applications, from tunable lasers and filters to variable optical attenuators and dynamic channel equalizers. The failure mechanisms of these devices will be addressed in terms of reliability physics, packaging methodologies, and process controls. Typical OEM requirements will also be presented, including testing beyond of the scope of Telcordia qualification standards. The key conclusion is that, with sufficiently robust design and manufacturing controls, MEMS-based devices can meet or exceed the demanding reliability requirements for telecommunications components.

Keywords: MEMS, tunable laser, tunable filter, VOA, DCE, reliability, optical, Telcordia

1.0 INTRODUCTION

MEMS-based devices have been used for decades in applications like accelerometers and other sensors, demonstrating high reliability in demanding environments. More recently, Texas Instrument's digital micro-mirror devices (DMD) have enabled the successful deployment of over 1.5 million light projection systems, with estimated mean lifetimes of over 50 years [1]. In the telecommunications industry, the use of MEMS-based devices has proliferated over the past ten years, with applications in optical switching [3,7], tunable lasers and filters [2-5], optical cross-connects, attenuators, add/drop multiplexers, and DWDM [6].

There is a growing body of literature on the fundamental materials properties and size effects of MEMS structures [8-11], as well as their performance in extended cycling [12-13] and extreme shock and vibration environments [14-16]. However, given the wide variety of MEMS device structures and their relevant failure modes, there is a general lack of MEMS-specific qualification test requirements. In the absence of standardized testing, more extensive knowledge of failure modes, and the associated reliability of MEMS-based devices, many OEMs have developed their own requirements for device manufacturers.

2.0 MEMS STRUCTURES AND PROCESSING

The author has worked with two main types of MEMS structures: comb-driven actuators and diffractive mirrors. Both structures are composed of single crystal silicon and produced using deep reactive ion etching (DRIE), with typical out-of-plane thicknesses less than 100 microns and minimum in-plane thicknesses of comb and support elements of 5 microns. Scanning electron micrographs of each structure are shown in **Figures 1** and **2**.

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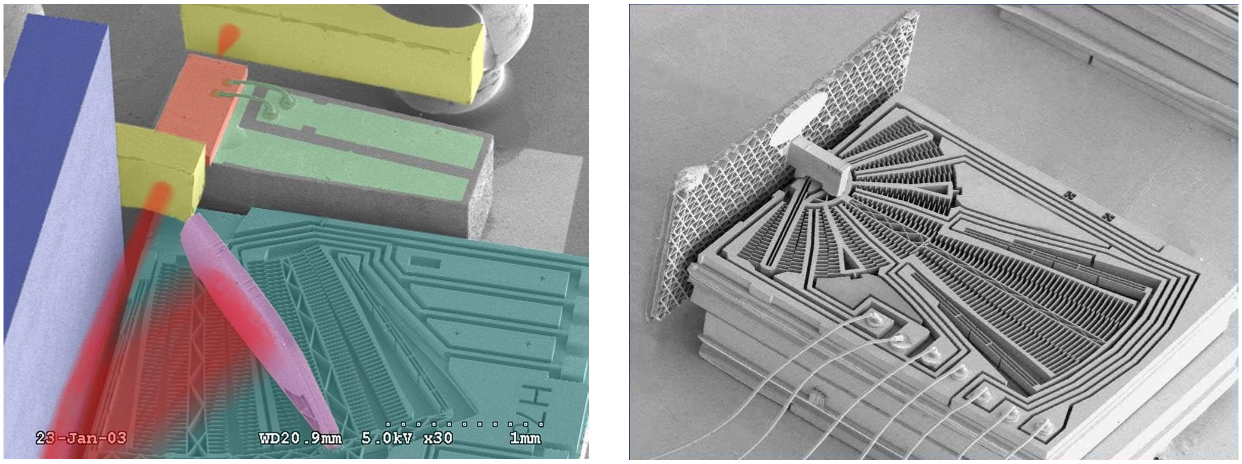
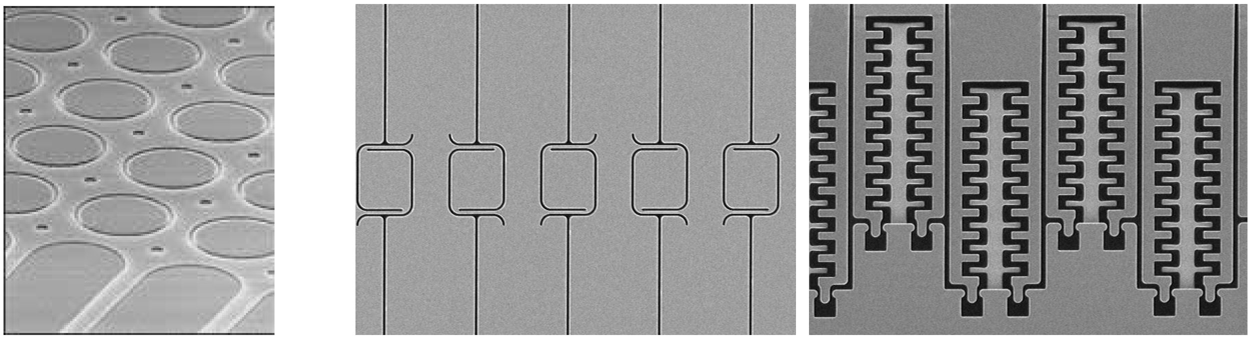
The actuator structures are used to move adhesively-attached mirrors that are also produced by DRIE etching. The first structure (**Fig. 1(a)**) is used in a Fabry-Perot tunable laser with a Littman-Metcalf external cavity, where the cavity is defined by the distance between the laser diode facet, grating, and MEMS mirror. The second structure (**Fig. 1(b)**) is used to modify the optical path length in a tunable filter. Both devices have closed loop control (the first with feedback from a wavelength locker subassembly, and the second with position detection off of the back surface of the mirror with a LED/split detector subassembly), and each enables tuning over 100+ channels of the C and/or L band, with 25 to 50 GHz channel spacing. The MEMS structures of both devices are co-packaged with other optical subcomponents and then hermetically sealed in conventional butterfly packages.



(a) (b)

Figure 1: MEMS actuators for (a) tunable lasers and (b) tunable filters/receivers.

The diffractive mirror structures are used in variable optical attenuators (VOAs, **Fig. 2(a)**) and dynamic channel equalizers (DCEs, **Fig. 2(b)**). In both cases, the optical beam path is perpendicular to the plane of the MEMS structures, and the mirrors tilt out of plane to affect attenuation of the reflected optical power. The VOA attenuates wavelengths more or less equally, whereas the DCE selectively attenuates up to 100 independent wavelengths spaced over the C and/or L band, similar to the tunable laser and filter. The MEMS components of each device are packaged individually into hermetic subassemblies (TO cans and 96-pin packages, respectively), and then integrated into larger structures.



(a) (b)

Figure 2: Diffractive MEMS structures for (a) VOAs and (b) DCEs (showing both the mirror pivots and combs).

3.0 MEMS FAILURE MECHANISMS

There are a variety of failure mechanisms that can affect the reliability of MEMS structures: flaw sensitivity (arising from low fracture toughness) and the associated size dependence of strength, fatigue, stiction, wear, and stress corrosion cracking (due to water vapor). Depending on the MEMS design, stiction and wear may be eliminated – all of the structures discussed in **Section 2** are non-contacting except in extreme shock and vibration events. Since elevated water vapor concentrations tend to exacerbate all failure mechanisms (stiction is usually inhibited by adsorbed water), the vast majority of MEMS devices in telecom applications are hermetically packaged. Fatigue can be effectively eliminated by maintaining a sufficient margin of safety between the design stresses and the stress associated with the fatigue crack growth threshold.

The fracture toughness of DRIE structures is roughly equivalent to that of bulk single crystal silicon. Literature values are below 1.0 MPa√m independent of the cleavage plane [11], compared to values as high as ~4 MPa√m for polycrystalline silicon. The higher values for polysilicon are due to grain boundary toughening and other crack deflection mechanisms; such mechanisms are completely absent in single crystal silicon. The generic relationship between fracture toughness, K_c, strength, σ_c, and flaw size, a, is given by:

$$K_c = Y \cdot \sigma_c \cdot \sqrt{\pi a} \tag{1}$$

where Y is a geometric factor that varies with loading conditions and sample size. Since fracture toughness is generally constant (in the absence of environmental factors), the strength is controlled by surface defects (either etching defects or intentional stress concentrators), as compared to both surface and bulk defects for polycrystalline silicon.

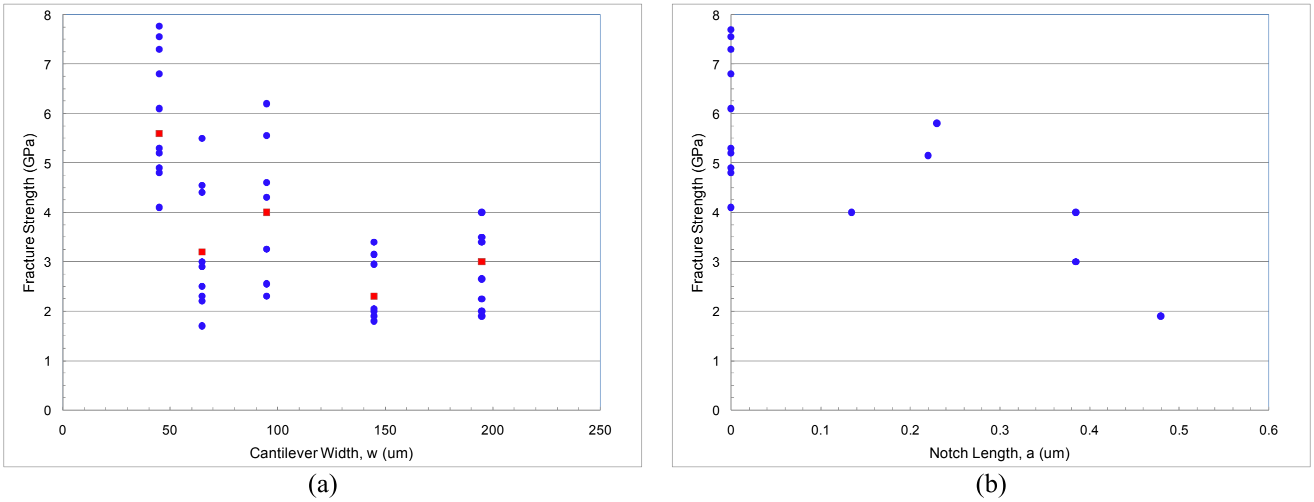
Size dependence of strength is a direct consequence of flaw sensitivity, since the likelihood on encountering a critical flaw increases as the surface area (or volume, for materials with bulk defects) increases. The failure probability, P_s, as a function of stress, σ, and surface area, A, is generally described using a two-parameter Weibull distribution of the form:

$$P_s(A) = \exp(-(A/A_o)\cdot(\sigma/\sigma_o))^m \tag{2}$$

where m and σ_o are the Weibull shape parameter and reference strength, respectively, and A_o is the sample surface area on which both are experimentally determined. Both the strength and Weibull modulus vary significantly based on the surface roughness and defect density, but generally values of 1.2 to 8 GPa and 2.7 to 12, respectively, can be obtained with secondary processes to improve sidewall quality [9,10].

The impact of MEMS element size and geometry on the resulting strength of simple unnotched and notched cantilever structures is shown in **Figure 3**, using data adapted from Minoshima *et al* [9]. The increasing spread in strength values as cantilever dimensions decrease is likely an impact of both slight variations in the nominal dimensions due to etching variations as well as the diminishing difference between surface flaw size and sample dimensions (a ratio of ~0.002 for the largest cantilever and ~0.1 for the smallest). The notches used in that study simulate single surface defects, and provide a vivid illustration of the effect of surface quality on strength – see **Figure 5** for images of typical sidewall quality.

Water vapor- and particulate-induced shorting (or blocking) of comb and diffractive MEMS structures are not intrinsic mechanisms, but nonetheless are likely the most commonly observed types of failures. Water vapor-induced failures can be eliminated using conventional hermetic packaging techniques, and hence such failures are strong indicators of poor process control and/or package design. Reduction of particulates in packaged devices is more difficult for a number of reasons: first, the silicon MEMS device itself is a large source of particulates, either as slivers from roughly-etched sidewalls that break loose during contact or as chips broken off from device edges and surfaces during handling; second, particulates from other ceramic, metallic, or glass subcomponents (arising from handling) are common even in well-controlled cleanroom environments. As discussed in **Sections 4** and **5**, more extensive screening tests are required to reduce the impact of particulates.



(a) (b)

Figure 3: Measured fracture strength of etched single crystal Si as a function of (a) cantilever width and (b) notch depth (adapted from Minoshima *et al.* [9]).

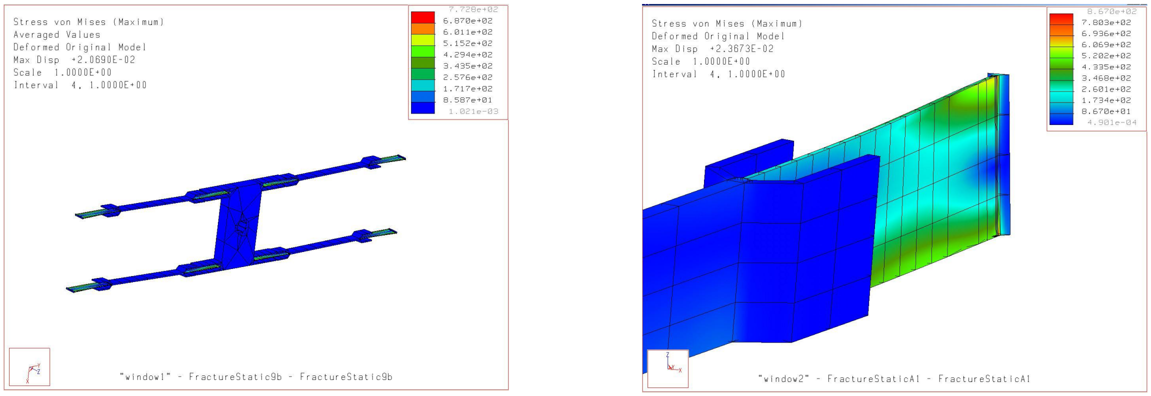
4.0 MEMS DESIGN, SCREENING, AND QUALIFICATION ISSUES

Much like any active opto-electronic component, substantial design, process control, and qualification testing is required to produce a reliable MEMS-based component. One of the goals of this paper is to highlight key test techniques during the development process, and thereby provide guidance for future MEMS-based telecom devices. Descriptions of various analyses, measurements, and tests are detailed in **Table 1** below.

Mechanical design and finite element analysis (FEA) software packages are indispensable tools for MEMS development. The most recent packages explicitly address surface roughness effects to identify the locations of highest stress concentration and subsequent fracture, which, as discussed in **Section 3**, are critical to evaluating MEMS processing parameters and their impact on flaw size distributions & subsequent fracture locations. On-wafer test structures and SEM or interferometric measurements of surface quality can then be used to provide accurate process capability assessments of material quality both within a given wafer and across multiple wafer lots. Relatively simple FEA analyses of a typical on-wafer test structure are shown in **Figure 4**. Representative SEM micrographs of wafers produced with two different processes are presented in **Figure 5**, overlayed on a graph showing the cumulative failure distributions (fracture load, as applied to the center of the structure in **Figure 4(a)**) for multiple test structures on each wafer. In this example, the fracture load in grams is roughly equivalent to the fracture stress in GPa. The values are consistent with those reported in other studies [9, 10].

Table 1: Summary of analysis and testing performed during development of MEMS devices for telecom applications.

Development Step	Description and Objectives
Design	• Mechanical/finite element analysis: dimensional parametric studies to assess resonant frequencies, peak stresses, and critical feature/flaw sizes
Process Development & Control	• Wafer processing: SEM/interferometry of etch quality on actual and test structures; adhesion and strength measurements on test structures • Actuation characterization: curve tracer measurements of displacement as a function of I/V
Evaluation	• Swept-frequency vibration (operational and non-operational): confirm resonant frequencies; assess optical performance variation; iterative development of closed loop controls (if necessary) • MEMS on submount: stepped shock testing to failure (500-5000 g+ acceleration) to identify functional limits
Screening	• MEMS on submount: "proof" testing at 750 g+ acceleration to identify low level defects • Device: "proof" testing at 500 g+ acceleration to identify low level defects • Random locking (fixed or variable frequency): assess stability of actuator movement, particularly particulate-induced blockage or shorting
Qualification (per relevant Telcordia standard)	• Operational vibration (5 g, 10-100 Hz; 2 g, 100-500 Hz): GR-468 • Non-operational vibration (20 g, 20-2000 Hz): GR-468,-1073, and -1221 • Operational shock (10g, 0.3 msec half sine; customer requirements up to 50 g, 0.1 msec half sine): GR-468 • Non-operational shock (500 g, 1 msec half sine with TEC; 1500 g, 1 msec half sine with no TEC): GR-468;-1073, and -1221 • Endurance locking/actuation (10 k-10 M cycles): GR-1073



(a) (b)

Figure 4: Typical FEA analysis of an actuator test structure, indicating the location of maximum stress. Note that these calculations do not explicitly account for surface roughness and defects, but that such can easily be implemented in FEA as a design/verification tool.

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