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PROVISIONAL APPLICATION FOR PATENT COVER SHEET (Small Entity)

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53 (c).

INVENTOR(S)/APPLICANT(S)

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☐ *Additional inventors are being named on page 2 attached hereto*

TITLE OF THE INVENTION (280 characters max)

HIGH FREQUENCY PULSE WIDTH MODULATION DRIVER, PARTICULARLY USEFUL FOR ACTUATING MEMS ARRAY, VER. 2

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ENCLOSED APPLICATION PARTS *(check all that apply)*

☒ Specification	*Number of Pages*	**16**	☒ Small Entity Statement
☒ Drawing(s)	*Number of Sheets*	**7**	☐ Other (specify)

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☒ No.

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Respectfully submitted,

SIGNATURE Charles S Guenzer

Date **7 February 2001**

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USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

Provisional Patent Application
Attorney Docket No.: 3822.06-PV2
Movaz Docket No.: 2000-02

Title: High Frequency Pulse Width Modulation Driver, Particularly Useful for Actuating MEMS Array, ver. 2

Inventors:
Steven L. GARVERICK
Michael L. NAGY

Technical Description

Several technologies have been proposed as a means to accomplish Wavelength Cross Connect (WXC) switching. Bubbles, crystals, fabrics, and micro electromechanical systems (MEMS). MEMS has several advantages. One configuration for the MEMS array is described in US Provisional Application 60/234,683, filed 22 September 2000, incorporated herein by reference in its entirety. A slightly earlier version is described in US Provisional Application ____ with title "High Frequency pulse Width Modulation Driver, Particularly Useful for Actuating MEMS Array," filed 26 January 2001.

The size and number of micro-mirrors in the MEMS array is determined by a number of optical parameters, as well as the tradeoff between chip size and manufacturing yield. An array size of 12 x 80 mirrors appears to be optimal for early implementation. Although micromirrors are the described embodiment, it is understood that the invention is applicable to driving a wider class of actuators

Once an approximate actuator array size is determined, several actuation methods for MEMS, all well known to those skilled in the art, are available. Thermal actuators rely on the thermal expansion of materials when (relatively) large amounts of current are run through them. Although capable of fairly large forces, this actuation method is sensitive to changes in ambient temperature, consumes a great deal of electrical power when the entire array is considered, and suffers from aging, wear, and nonlinearity effects. It is also slow to respond. Electromagnetic actuators establish a magnetic field across the array and then run controlled amounts of current through each actuator. Although capable of bi-directional actuation and relatively precise, these actuators tend to be difficult to fabricate, require large size to accommodate large planar coils, and can dissipate large amounts of power – possibly creating enough heat to damage the system. Additionally, high field magnets are subject to aging and temperature effects. Piezoelectric actuators comprise structures made of a deposited piezoelectric thick- or thin-film, typically PZT. This technology is difficult to fabricate, is not suitable for large displacements, and generally cannot accommodate the kinds of small feature sizes required for extremely tight pitch. The actuation technology of choice for an array of the required dimension is electrostatic. Imposing a voltage across two nodes creates an attractive, electrostatic force between them. Of all the options, electrostatic actuation features the lowest power consumption and hence the best thermal environment, does not require an external magnetic field, accommodates small device sizes, performs well over temperature and time, and has a high switching speed.

An example of a cell of an electrostatically controlled MEMS array is illustrated in the plan view of Figure 1. It includes a gimbal structure of an outer frame 10 twistably supported in the support structure 12 of the MEMS array through a first pair of torsion bars 14 extending along and twisting about a minor axis and a mirror plate 16 having a reflective surface twistably supported by the outer frame 10 through a second pair of torsion bars 18 arranged along a major axis perpendicular to the minor axis and twisting thereabout. In the favored MEMS fabrication technique, the illustrated structure is integrally formed in an epitaxial (epi) layer of crystalline silicon. The process has been disclosed in US Provisional Application, Serial No. 60/260,749, filed 10 January 2001, incorporated herein by reference in its entirety. The structure is controllably tilted in two dimensions by a pair of electrodes 20 under the mirror plate 16 and another pair of electrodes 22 under the frame. Air gaps 24, 26 are formed respectively between the frame 10 and the support structure 12 and between the mirror plate 16 and the frame 10 and overly a cavity formed beneath the frame 10 and mirror plate 16 so that they can rotate. The support structure 12, the frame 10, and the mirror plate 16 are held at a common node voltage and the frame 10 and mirror plate 16 form one set of plates for variable gap capacitors. The electrodes 18, 20 are at the bottom of the cavity so the cavity forms the gap of the two capacitors between the electrodes 18, 20 and the frame 10 and mirror plate 16.

One drawback of electrostatic actuation is a phenomenon known as 'snap down'. Because electrostatic force is inversely proportional to the distance between the electrodes, there comes a point at which the attractive force increases very rapidly with greater electrode proximity. Beyond this point, a small decrease in distance leads to an enormous increase in force, until the electronic control system cannot respond fast enough and the electrodes 'snap' together. With an architecture such as ours, where the electrodes comprise a flat plate suspended over a cavity by small tethers, a rule of thumb states that the plate will begin to 'snap down' at a deflection corresponding to approximately four ninths the depth of the cavity. Hence, in order to achieve a deflection of x, the cavity must be approximately 2.25x deep. Optical constraints define the deflection distance requirement for the electrostatic micromirrorn actuator. The rms voltage level required to generate a given amount of deflection results from a combination of mirror size, tether spring constant, and cavity depth. The cavity depth required to avoid snapdown generally dictates high voltages, typically in excess of 40V, which is the upper limit for many standard IC processes. The generation of voltages in the 50V, 100V, 200V, and higher ranges requires an electronics system comprised of High Voltage (HV) semiconductor components, either off-the-shelf or customized, which are fabricated by specialized HV processes.

The optical requirements on the system not only dictate a 12 x 80 array of mirrors, but they also require tilt in both directions along two axes. The 'see-saw' MEMS architecture accomplishes tilt by placing two electrodes symmetrically about the central tether for each axis. Hence there are four electrodes per actuator, giving a total of 3840 independently controlled electrodes for the entire array. An optical technique called 'interleaving' allows us to split the array into two 12 x 40 chips, but even with this amelioration the i/o count at the MEMS chip is 1920 High Voltage inputs. While i/o counts of several thousand are commonplace in certain low voltage digital technologies such as memories, in our situation the inputs are analog and High Voltage. High analog i/o count brings about two packaging penalties: (1) interfacing the MEMS chip to the drivers, and (2) housing the drivers.

Conventional methods for silicon chip i/o include wire bonding and die-to-substrate attachment known as 'flip-chip'. People skilled in the art know that wire bonding becomes impractical at about 800 i/o's, due to the large chip perimeter required to contain the bond pads. IC's with higher i/o counts are typically attached to a substrate with solder bumping, a well known technology. However, in our case the substrate in question must ultimately route the MEMS chip's signals to 3840 independent High Voltage drivers. An array such as this built out of discrete components would require a large number of electronics cards, plus cabling, that would increase the total system size significantly. A far better solution is to put the HV drivers on an Application Specific Integrated Circuit (ASIC), and connect this ASIC to the MEMS chip by chip-on-chip solder bumping, frit bonding, or similar means. Besides containing the high voltage drivers, the ASIC can now demultiplex drive signals from the larger system. We are left with a Dual Chip Stack, with the High Voltage ASIC below the MEMS chip, leaving the upper (mirrored) surface of the MEMS chip exposed. The chips are precision aligned such that each MEMS actuator is positioned over its dedicated electrodes, which are fabricated in an upper metal layer of the ASIC. The single electrical connection to the MEMS actuator's Common Node can be accomplished by eutectic bonding, polymer bonding, or wirebond(s) from the top side. The HV ASIC receives drive command signals from the outside world via a small number of wirebond pads on its periphery (typically several dozen), which are wirebonded to a standard patterned substrate carrier (ceramic or plastic carriers are typical). The HV ASIC's on-chip electronics multiplex the wirebonded command signals, convert them to high voltage, and send them through the bondpads to the MEMS chip. Perhaps an even more significant advantage of this arrangement is that the unwanted capacitance of a typical solder bump to ground (called "parasitic capacitance") is far lower than the parasitic capacitance associated with a wirebond plus long PWB track, allowing for smaller driver transistors and lower thermal dissipation.

Figure 2 is a cross sectional sketch of one cell of the MEMS device showing the mirror plate 16 with a cavity 28 between it and the mirror plate electrodes 20. The frame is not shown. . The relative dimensions are not to scale. The device has a large lower "substrate" region 30 and a thin upper "MEMS" region 32, separated by a thin insulating oxide layer 34. The tilting actuators are etched into the upper region, each actuator suspended over the cavity 28 by several tethers. The electrodes are patterened onto the substrate, which can be an ASIC, a ceramic, or a PWB. . All the actuators in the upper region form a single electrical node, called the "Common Node". Each actuator is suspended above four electrodes, each electrode being isolated from every other electrode. To cause the actuator to tilt in a given direction, we produce an electrostatic force between the actuator and one or more of its electrodes by imposing a potential difference between the Common node and the desired electrode. Note that each actuator has two pairs of complementary electrodes - one causing tilt along the "Major Axis" and the other causing tilt along the "Minor Axis". Fabrication details are supplied in the aforementioned Provisional Application 60/260,749.

This design includes an array of electrostatic microactuators that require high voltage drive, on the order of 100V - 300V rms. Each actuator has two perpendicular axes of tilt, called the Major Axis and the Minor Axis, shown in Figure 1. Each axis has a pair of electrodes. When a high voltage is applied to an electrode (with respect to the actuator node), the attractive force will cause the actuator to tilt in the desired direction. We wish to drive an array of 12 x 80 actuators, ultimately scaling to 24 x 80 actuators.

To ease packaging constraints, minimize parasitic capacitances, and provide for a small system volume, we have adopted a chip-on-chip architecture, where the micro electro-mechanical system (MEMS) actuator array is bonded directly to our High Voltage (HV) application specific integrated circuit (ASIC). This bonding can be accomplished with frit bonding, eutectic bonding, soldering, polymer bonding, or other means known to those skilled in the art. This implies an ASIC that not only drives each actuator independently, but can also demultiplex those drive signals on-chip, thus minimizing i/o count for the system.

Several factors constrain the HV ASIC design:

1. Experiments have shown that imposing pure dc voltage across the MEMS actuator over long periods of time causes a residual static charge buildup, sufficient to inhibit future movement of the actuator. Therefore, any should be a bipolar ac signal, symmetric about ground potential, which still maintains the required 200Vrms potential difference across the actuator.

2. The drive signal's frequency must not be near the mechanical resonance frequency of the MEMS structure (currently estimated to be about 5 kHz).

3. The resolution of the control voltage must be - very precise, ideally better than 0.1% of full scale tilt for desired angles.

4. Total area of each driver cell in the array must be minimal. Typical value of area available for each cell is roughly 450 x 600 micron.

5. High voltage devices with large die area, such as high voltage capacitors and high voltage field-effect transistors (FETs), should be avoided (due to constraint #4). HV FETs with high current output tend to be very large.

The decision to go to a HV ASIC limits us to ASIC technologies that are capable of packing High Voltage CMOS into a very tight array area. The need to minimize physical size of drive transistors and on-chip multiplexing circuitry will inform all subsequent design.

With the MEMS / HV ASIC Dual Chip Stack architecture defined, we now have a choice in the type of drive voltage used to tilt the Electrostatic MEMS actuators. Candidates include: (1) dc voltage, (2) single-ended ac voltage (i.e.

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