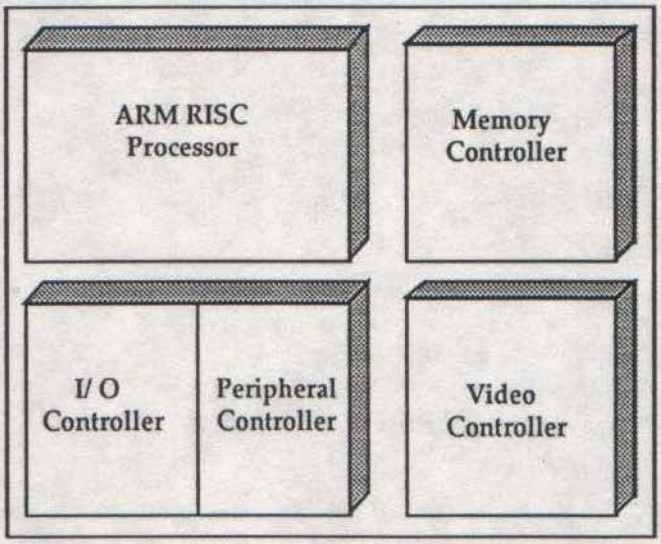
ARM250 - Integrated Controller

The ARM250 is a complete computer system on a chip - comprising a 32-bit RISC processor, a memory controller with DRAM interface, a bit-mapped video controller and an I/O controller. It is suitable for a wide range of cost-sensitive embedded control, portable and consumer games applications - particularly (but not only) those which require a video display.

The device is designed to drive up to 4 Mbytes of DRAM directly at 12 MHz, and at these speeds can sustain about 10 MIPS (peak).

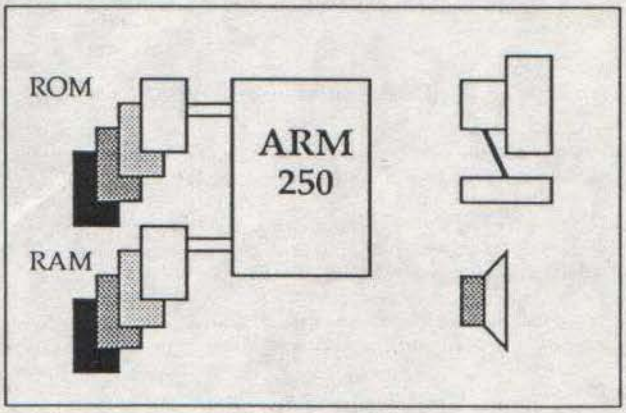


- ARM 32 bit RISC core
- Memory Controller
- Video Controller
- Flexible I/O Controller
- Reduced system cost
- 10 MIPS (peak) @ 12 MHz
- Small footprint 160 PQFP package
- Low power consumption

Applications

- Portable Computers
- Desktop Computers
- Games Consoles
- Palmtop Computers
- Low cost X terminals

Example - Video games console



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1. Overview

The ARM250 is a highly integrated microcontroller based on a *32 bit RISC processor.* In addition to the central processor the ARM250 includes :

a *Memory Controller* with direct interface to DRAM and ROM and support for memory mapping and protection.

a *Video controller* for bit-mapped display with integral palette. On-chip video and sound DACs allow interfacing to video monitors with minimal external circuitry..

an *I/O controller* interfaces to a wide range of standard peripheral chips. Provides timers, serial port, parallel port and a range of interrupt and configuration inputs.

The I/O subsystem contains some on-chip functions such as timers, and in addition can directly drive industry standard peripheral chips. The video subsystem is capable of a wide variety of display modes up to Super VGA resolutions (600 X 800 pixels), as well as adding impressive sound capability

The device is based on 4 standard chips from the ARM RISC chip set - ARM2aS, MEMC1a, VIDC and IOC. In order to reduce the size of this datasheet, the datasheets for these parts are not duplicated here as they retain identical functionality (but with improved performance) within ARM250. The relevant datasheets, available on request from Advanced RISC Machines Ltd, are as follows :

- ARM2aS Datasheet
- MEMC1a Datasheet
- VIDC Datasheet
- IOC Datasheet

The main blocks in ARM250 are the processor (ARM2aS), memory controller (MEMC), video controller (VIDC), input/output controller (IOC) and I/O extension block (IOEB). The first four of these blocks are based on standard chips from the ARM RISC chip set. Some extra logic, known as IOEB, is used in the I/O system and is documented in this datasheet.

A simplified block diagram appears in Figure 1. A list of relevant documentation is given later in this datasheet and a detailed block diagram of ARM250 appears at the end of this chapter.

1.1 Processor

The processor (ARM2aS) is an implementation of the Advanced RISC Machines' ARM processor which is a general purpose 32-bit single-chip microprocessor. The architecture is based on Reduced Instruction Set Computer (RISC) principles and provides a high instruction throughput and an excellent real-time interrupt response from a small silicon area.

Pipelining is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM instruction set has proved to be a good target for compilers of high-level languages. Where required for critical code segments, assembly code programming is also straightforward, unlike some RISC processors which depend on sophisticated compiler technology to manage complicated instruction inter-

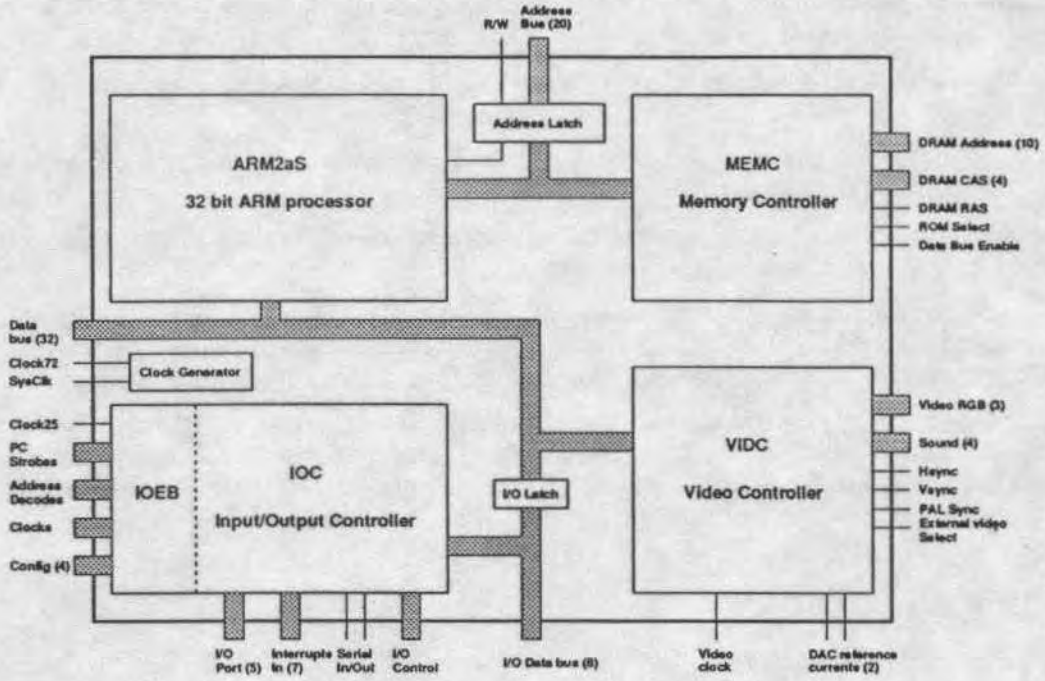

Fig 1 : Simplified Block Diagram

dependencies.

ARM Ltd provides a complete cross development toolkit for the ARM, consisting of the tools and documentation needed to develop software for ARM-based systems, including simulation and debug tools which allow ARM targeted software to be debugged and evaluated in more familar, fully hosted, software development environments.

1.2 Memory Controller

The memory controller (MEMC) acts as the interface between the ARM processor, the video controller, the I/O controller, read-only memories and dynamic memory devices, providing all the critical system timing signals and partitioning the memory map.

ARM250 is designed principally for use with two types of memory - read-only memory (ROM) and dynamic RAM (DRAM). In both cases, a 32 bit data bus is used to transfer memory data. A 20 bit address bus is used to supply addresses for ROMs and for I/O port memory mapping. Internally, a 26 bit address bus is used but only 20 bits are brought out to pins. To interface to up to 4 megabytes of DRAM, ARM250 provides multiplexed addresses and row and column strobes which drive the DRAM chips directly.

The memory controller also contains a Logical to Physical Address Translator which maps the physical memory into a 32MByte logical address space (with three levels of protection) allowing virtual memory and multi-tasking operations to be implemented. Fast "page-mode" DRAM accesses are used to maximise memory bandwidth.

The memory controller provides a Direct Memory Access (DMA) system for the video controller. It contains pointer registers to 3 separate RAM buffers which it automatically transfers to the video controller when required.

1.3 Video Controller

The video controller (VIDC) uses buffers in RAM to generate a video display with a hardware cursor and stereo sound. The memory controller is responsible for coordinating transfers from these buffers to the video controller by DMA. The video controller requests data from the memory when required, and holds it in one of three internal buffers before using it. Data from the internal buffers is serialised and then presented to a digital to analogue converter (DAC). There are DACs for both sound and video, allowing driving of video monitors and audio systems with minimal external buffering. The video data also passes through a colour look-up palette before being output.

Three forms of video synchronisation pulses are generated with programmable timing and polarity. The video clock may be selected from a variety of sources and appears on pins to allow the video to be "genlocked" to an external signal.

DMA transfers move video, cursor and sound data in blocks of four 32-bit words, allowing efficient use of page-mode DRAM without locking up the system data bus for long periods. The video controller is programmable, offering a very wide choice of display formats. The pixel rate can be selected from a range of sources and programmable prescaling applied. Video data can be serialised to either 8, 4, 2, or 1 bit per pixel. The horizontal timing parameters can be controlled to units of 2 pixels, and the vertical timing parameters can be controlled to units of a raster. The colour look-up palette which drives the three on-chip video DACs is 13 bits wide, offering a choice of 4096 colours or an external video source.

The hardware cursor is 32 pixels wide and may be any number of rasters high. It can be positioned anywhere on the screen. Three simultaneous colours (again from a choice of 4096) are supported, and any pixel can be defined as transparent, making it possible to define cursors of many shapes.

The sound system incorporates an exponential DAC and stereo image table for the generation of high quality sound. Up to 8 channels are supported, each with a separate stereo position.

1.4 I/O Controller

The I/O controller is based on a chip known as IOC together with some additional logic, known as IOEB, which is used to provide additional functionality. The I/O system is based around an 8 bit I/O bus which connected to the main data bus by latches which allow the memory and I/O systems to operate asynchronously. This bus can be upgraded to 16 bits with the addition of two external latches.

The I/O controller contains three 16 bit timers which are clocked at 2 MHz. Two of the timers are general purpose and may be used to provide timed interrupts. The third provides the clock for the serial interface which provides a UART-like interface for asynchronous serial data at baud rates up to 31250.

The memory controller defines part of the memory map as containing memory mapped I/O devices and the I/O controller controls accesses made in this area of memory. It provides four different cycle times for use with peripheral devices of varying speeds. The I/O part of the memory map is further divided by address decoding to provide a number of pins which are active in various parts of the I/O space. One of these areas is designed for interfacing directly to one of the highly integrated PC combination chips which provides interfaces to hard and floppy discs, parallel printer port, etc. It is also possible to bypass the I/O controller for certain I/O accesses so that the cycle timing is determined by external logic.

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