Comparison of Passive and Active Pixel Schemes for CMOS Visible Imagers

L.J. Kozlowski,[a] J. Luo[a] W.E. Kleinhans[b] and T. Liu[b]

[a]Rockwell Science Center, 1049 Camino dos Rios, Thousand Oaks, CA, 91360
[b]Valley Oak Semiconductor, 31255 Cedar Valley Drive Suite 314, Westlake Village, CA 91362

ABSTRACT

An active pixel sensor (APS) integrated in standard CMOS process technology is shown to be superior to an alternative passive pixel sensor (PPS). Further, the CMOS APS provides video sensitivity and SNR comparable to CCDs. Though the CMOS PPS has lower performance, it offers >50% optical fill factor without microlenses and can be produced at lower cost for applications not requiring broadcast quality SNR (>35 dB) under low light conditions (<20 lx). APS and PPS SNRs of 50 dB and 44 dB are reported at 200 lx using green filtering with ~80 nm bandpass.

Keywords: CMOS, APS, passive pixel, CCD

1. INTRODUCTION

Developments in CMOS image sensor technology are paving the way for a new generation of digital imaging products. Though most currently available electronic visible-light cameras use charge-coupled device technology for low-noise image capture, CMOS technology offers practical advantages with respect to on-chip integration of many camera-related functions and fundamental technological advantages with respect to temporal noise. The read noise of a CCD is effectively set by external circuits to a relatively wide bandwidth compatible with the video rate assuming that supporting chips are used to eliminate reset noise. CMOS APS read noise can be much lower because the noise bandwidth is much smaller – it is set by the on-chip electronics in the on-chip circuits servicing each column of pixel elements to service relatively low line rates. A second advantage is the relative ease at which higher sensitivity can be achieved in the CMOS imager paradigm. The key technical impediment to CMOS APS proliferation is the need to suppress the pixel-to-pixel fixed pattern noise generated by the same amplifiers that produce the clear-cut advantage in temporal noise.

Hybrid infrared imagers have used CMOS readouts since about 1985 for low-noise readout of photo-generated signals. Shrinking circuit geometries and advances in imager design have since enabled rapid improvements in the performance of the CMOS readouts used to interface various infrared detectors. Monolithic visible imagers have become available only recently because of the necessity for submicron photolithography to exploit the same low-noise signal extraction perfected for infrared sensors. The "sudden" emergence of CMOS imagers is, hence, only one more consequence of Moore's Law, which predicts the ability to double transistor integration on each integrated circuit about every 18 months. Shown in Figure 1 are the associated process and imager development trends, including the current general availability of CMOS processes having ~1 μm minimum feature and the imminent ability for much higher levels of transistor integration. CMOS imager development is consequently behaving as a delta function, where the amplitude depends on each developer's capability and imager complexity is driven by the application rather than process technology. The ongoing migration to even finer lithographies will thus enable the rapid development of CMOS imagers having even higher resolution, better image quality, higher levels of integration and lower overall imaging system cost than CCD-based solutions. The silicon wafer production infrastructure which has put personal computers into many homes is now enabling CMOS-based imaging in consumer products such as video and digital still cameras.

Further principal author information –
Email: ljkozlow@rsc.rockwell.com; WWW: http://www.rsc.rockwell.com/function/779/mct_fpa/; Telephone: 805-373-4267; Fax: 805-373-4687

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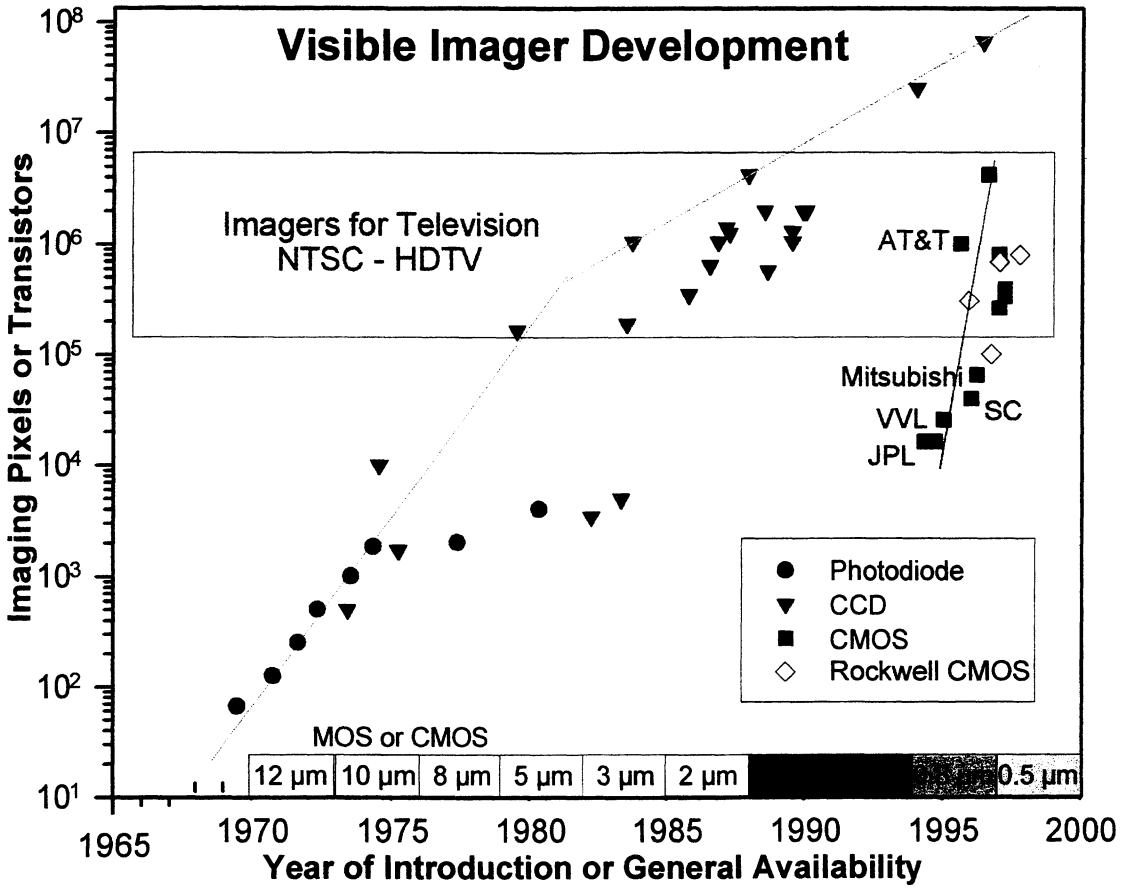

Figure 1.Chronology of Imager Pixel Count and CMOS Process Availability.

CMOS imagers use either active or passive pixels as shown in simplified form in Figure 2. Active-pixel sensors (APS) include some form of amplification in each pixel. Passive pixels are instead read out without pixel-based amplification. Since passive pixel sensors (PPS) have simple pixels consisting often of only a photodiode and a MOSFET switch, the circuit overhead cost is low and they have a high optical collection efficiency (fill factor) of 50 to 80 percent. The large optical fill factor maximizes signal collection and hence, minimizes fabrication cost by obviating the need for microlenses. Microlenses are a standard feature of CCD and CMOS APS imagers. When accurately deposited over each pixel, microlenses concentrate the incoming light into the photo-sensitive region. When the fill factor is low and microlenses are not used, the light falling elsewhere is either lost or, in some cases, creates artifacts in the imagery by generating electrical currents in the active circuitry.

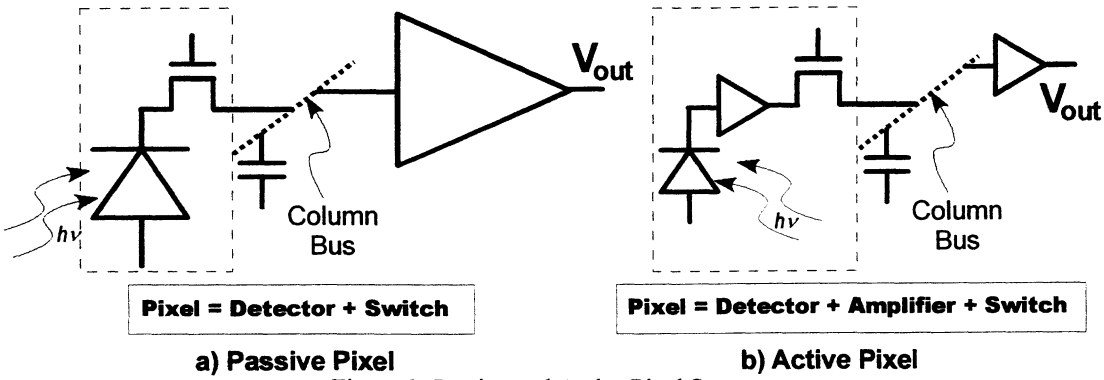

Figure 2. Passive and Active Pixel Sensors.

Active pixel sensors incorporate transistors in each pixel to convert the photo-generated charge to a voltage, amplify the signal voltage and reduce noise. Adding these components reduces APS fill factor in 0.6 μm processes to about 20 to 30 percent. To maximize the effective fill factor, APSs often use microlenses (Figure 2) to capture light that would otherwise strike the pixel's insensitive area. Microlenses double or triple the effective fill factor. Figure 3 shows the cross-sectional view of a CMOS PPS imager with color filters and optional microlens.

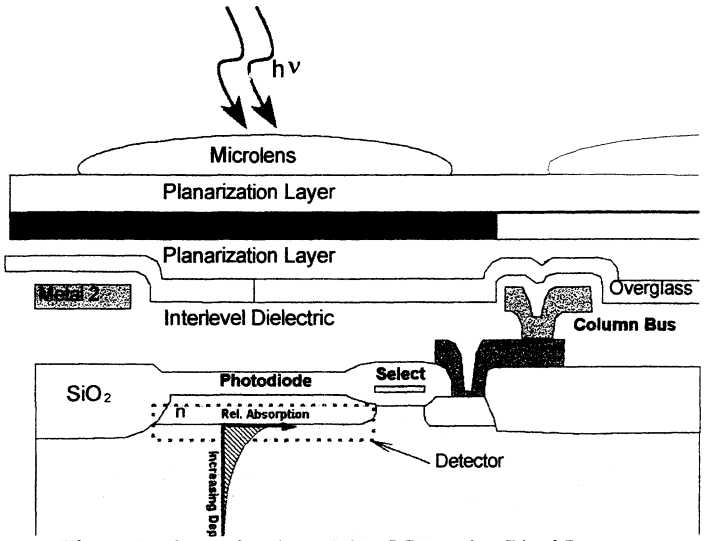

Figure 3. Cross-Section of CMOS Passive Pixel Imager

2. PASSIVE PIXEL SENSORS

The simplest passive pixel comprises a photodiode and an access transistor; the photo-generated charge is passively transferred from each pixel to downstream circuits.[1] The charge must, however, be efficiently transferred with low noise and nonuniformity. Since each column of pixels often shares a common bus (along a row or column) for reading the signal, suppression of temporal noise and offset nonuniformity are typically facilitated in the buffer servicing each bus. Plummer[2] used a buffer consisting of a transimpedance amplifier with capacitive feedback to yield reasonable sensitivity (Figure 4) considering the large bus capacitance and the MOS technology available at the time. Since such charge-amplification means were not generally practical for on-chip implementation in early MOS imaging sensors, alternative means compatible with NMOS technology were used. Koike[3] and Ohba,[4] for example, implemented a scheme which was mass-produced by Hitachi for camcorders.[5] The key refinements with respect to Plummer were anti-blooming control and circuitry for reducing fixed pattern noise. Though these imagers were proven inferior to the emerging charge coupled device (CCD) imagers available at the time due to MOS process immaturity, similar MOS imagers are still being offered commercially.[6]

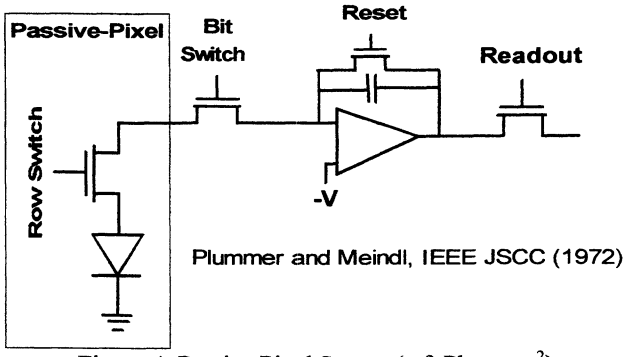

Figure 4. Passive Pixel Sensor (c.f. Plummer[2]).

Subsequent efforts at improving passive-pixel imager performance focused on column buffer enhancements. Ando[7] improved the column buffer by using an enhancement/depletion inverter amplifier to provide reasonably large amplification in a small amount of real estate; its 40 lx sensitivity was nevertheless nearly an order of magnitude below that of competing CCD-based sensors. Sonoda[8] both enhanced sensitivity and facilitated automatic gain control via charge amplification in the column buffer. Wyles[9] and Denyer[10] have recently revisited Plummer's original capacitive-feedback transimpedance amplifier (CTIA) concept because the CTIA is nearly ideal for passive-pixel readout if issues with temporal noise pickup and fixed-pattern noise are adequately addressed.

2.1 352x288 Passive Pixel Sensor

Expanding on Plummer's original concept by using mixed-signal 0.6 µm CMOS, we have developed a 352x258 (Common Intermediate Formate; CIF) passive pixel sensor with CTIA-based column buffer with 10 µm x 9.15 µm pixel size. The imager's noise performance was modeled similarly to our other capacitive transimpedance amplifier (CTIA) designs.[11] Appropriately modifying the CTIA paradigm and applying the various device parameters which were either extracted or purposely implemented in the CIF imager design including ~1.7 pF bus capacitance, Figure 5 was generated where N_{imager} is the total noise including background shot noise (N_{photo}) at 0.35 lx, detector noise (N_{det}), and PPS read noise (N_{read}). $N_{channel}$ and $N_{amp1/f}$ are the dominant column buffer noise sources. N_{out} is the noise of camera electronics. The total predicted noise is 61 e- at the expected detector capacitance of 48 fF. We subsequently measured actual read noise of 75 e- ±10 e- on several of the PPS imagers. Though much progress has thus been made in developing passive-pixel imagers, their temporal S/N performance is fundamentally inferior to competing CCD imagers because the bus capacitance effectively translates to white noise on the order of 100 e-. CCDs, on the other hand, typically have read noise of 20 to 40 e- at video frame rates.

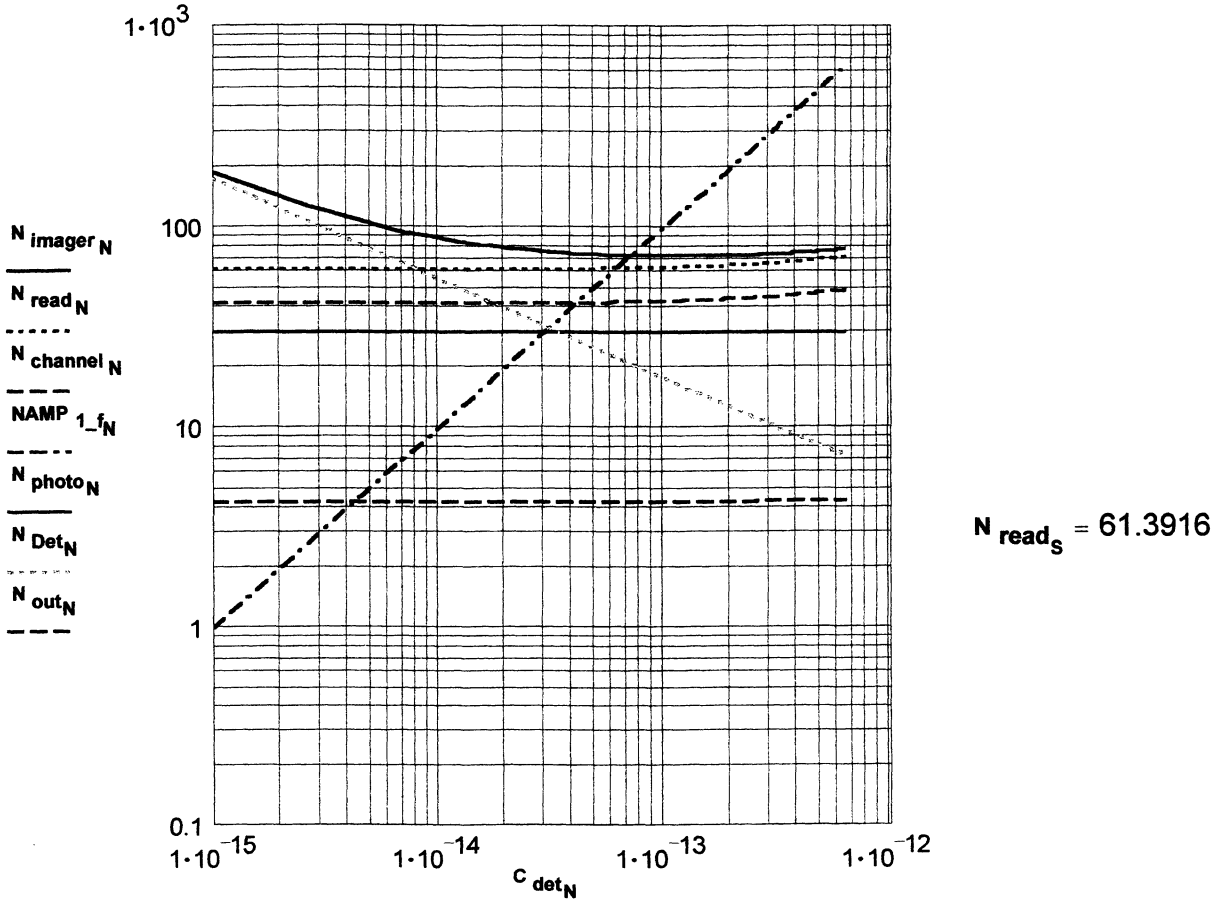

Figure 5. Passive Pixel Sensor Noise vs. Detector Capacitance.

Variable sensitivity was integrated on-chip by using several feedback capacitors in the column buffer CTIA which was programmable in 16 combinations. Figure 6 shows the measured sensitivity as a function of feedback capacitance. The minimum and maximum sensitivities are 4 and 48 μV/e-, respectively. By programming the various capacitors as a function of scene illumination, automatic gain control is facilitated. The rms gain nonuniformity of the PPS with CTIA column buffers was ≤0.6% rms with evidence that the nonuniformity was at least partially due to the light source.

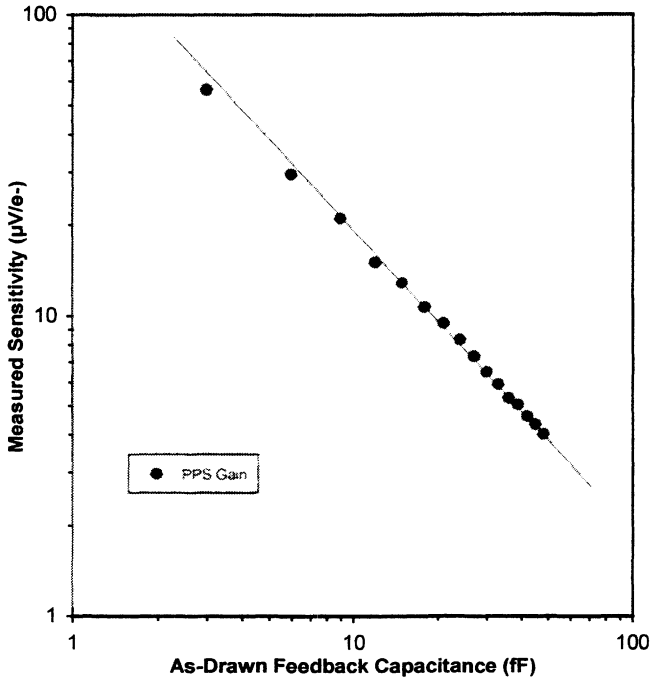

Figure 6. Measured PPS Sensitivity vs. As-drawn Feedback Capacitance.

Since each column buffer has a differing input offset voltage, on-chip offset cancellation circuitry was used to cancel these offsets. Figure 7 is an oscillogram showing the output of a typical line of video, both with the canceller enabled and for raw video. By enabling the offset canceller, the peak-to-peak nonuniformity is reduced from 14 mV to 2 mV. Using a custom digitizing acquisition system with 14-b resolution to measure the offsets, the rms nonuniformity is 160 μV. The rms nonuniformity relative to the maximum video swing of 1.2 V at 5 V supply voltage is 0.01%. Reducing the supply voltage to 3.3 V reduces the video swing to 1.1 V and thus increases the nonuniformity to 0.015%.

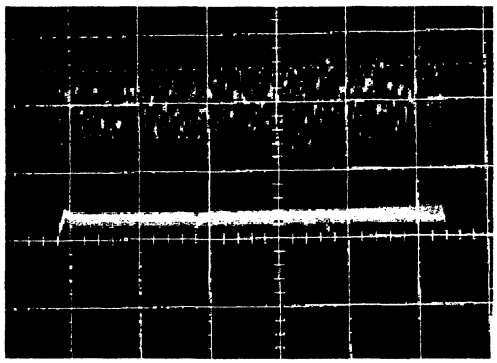

Figure 7. Oscillogram for one line of video at 10 mV/division with and without on-chip offset cancellation.

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