

CMOS Passive Pixel Imager Design Techniques

by

Iliana L. Fujimori

M.Eng. in Electrical Engineering and Computer Science,
Massachusetts Institute of Technology,
June 1997

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Massachusetts Institute of Technology,
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Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

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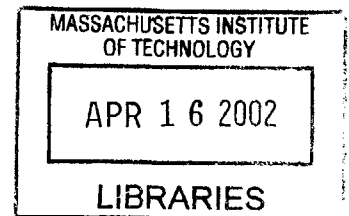
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Author

Department of Electrical Engineering and Computer Science
February 1, 2002

Certified by.

.....
Charles G. Sodini
Professor of Electrical Engineering
Thesis Supervisor

Accepted by

.....
Arthur C. Smith
Chairman, Department Committee on Graduate Students

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Abstract

CMOS technology provides an attractive alternative to the currently dominant CCD technology for implementing low-power, low-cost imagers with high levels of integration. Two pixel configurations are possible in CMOS technology: active and passive. The active pixel requires a minimum of three transistors to convert light to voltage. The passive pixel, on the other hand, consists of a single transistor, and its output is in the form of charge. Column-parallel opamps are used to amplify the charge to a voltage output. The main advantage of the passive pixel is a higher fill factor in a given pixel geometry. This advantage becomes increasingly important as we scale to smaller pixel sizes. The higher fill factor comes at a high cost as the charge output on the high impedance node of the column line is susceptible to disturbances, namely a parasitic current and temporal noise. The goal of this thesis is to determine the source and effects of the disturbances on the image sensor characteristics and the repercussions for scaling to high-density arrays.

A signal-dependent parasitic current composed of optically-generated carrier diffusion, blooming and subthreshold currents contaminates the pixel output. This parasitic current is detrimental to the imager because a few bright pixels can affect the rest of the pixels on the column line, resulting in bright vertical stripes on the image. A correlated-double sampling circuit in a differential architecture is used to remove the effects of the parasitic current. Column fixed-pattern noise is maintained below 1.5% for the linear illumination range of the imager.

A noise analysis reveals the opamp read noise is the dominant source of temporal noise. The effects of the sample-and-hold readout circuit on the output-referred opamp read noise are modeled and closely match the measured noise. The output read noise power is directly proportional to the vertical resolution of the imager and inversely proportional to the pixel area, resulting in a strong dependence between noise and pixel density.

This co-dependence is further analyzed in a scaling model where the fill factor, noise and dynamic range are observed for varying pixel size and vertical resolution over three fabrication technologies. The fill factor decreases with pixel size, and is highest for the technology with the smallest feature size, $0.18\mu m$. The noise increases with decreasing pixel size and increasing vertical resolution and has the best performance in the $0.18\mu m$ technology. The dynamic range decreases with pixel density, but has a strong dependence on the power supply voltage of the technology.

Thesis Supervisor: Charles G. Sodini
Title: Professor of Electrical Engineering

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