CMOS Passive Pixel Imager Design Techniques

by

Iliana L. Fujimori

M.Eng. in Electrical Engineering and Computer Science,
Massachusetts Institute of Technology,
June 1997

B.S. in Electrical Engineering and Computer Science,
Massachusetts Institute of Technology,
June 1997

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2002

Author .....
Department of Electrical Engineering and Computer Science
February 1, 2002

Certified by .....
Charles G. Sodini
Professor of Electrical Engineering
Thesis Supervisor

Accepted by .....
Arthur C. Smith
Chairman, Department Committee on Graduate Students

The author hereby grants to MIT

Magna 2045

CMOS Passive Pixel Imager Design Techniques

by

Iliana L. Fujimori

Submitted to the Department of Electrical Engineering and Computer Science
on February 1, 2002, in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy in Electrical Engineering and Computer Science

Abstract

CMOS technology provides an attractive alternative to the currently dominant CCD technology for implementing low-power, low-cost imagers with high levels of integration. Two pixel configurations are possible in CMOS technology: active and passive. The active pixel requires a minimum of three transistors to convert light to voltage. The passive pixel, on the other hand, consists of a single transistor, and its output is in the form of charge. Column-parallel opamps are used to amplify the charge to a voltage output. The main advantage of the passive pixel is a higher fill factor in a given pixel geometry. This advantage becomes increasingly important as we scale to smaller pixel sizes. The higher fill factor comes at a high cost as the charge output on the high impedance node of the column line is susceptible to disturbances, namely a parasitic current and temporal noise. The goal of this thesis is to determine the source and effects of the disturbances on the image sensor characteristics and the repercussions for scaling to high-density arrays.

A signal-dependent parasitic current composed of optically-generated carrier diffusion, blooming and subthreshold currents contaminates the pixel output. This parasitic current is detrimental to the imager because a few bright pixels can affect the rest of the pixels on the column line, resulting in bright vertical stripes on the image. A correlated-double sampling circuit in a differential architecture is used to remove the effects of the parasitic current. Column fixed-pattern noise is maintained below 1.5% for the linear illumination range of the imager.

A noise analysis reveals the opamp read noise is the dominant source of temporal noise. The effects of the sample-and-hold readout circuit on the output-referred opamp read noise are modeled and closely match the measured noise. The output read noise power is directly proportional to the vertical resolution of the imager and inversely proportional to the pixel area, resulting in a strong dependence between noise and pixel density.

This co-dependence is further analyzed in a scaling model where the fill factor, noise and dynamic range are observed for varying pixel size and vertical resolution over three fabrication technologies. The fill factor decreases with pixel size, and is highest for the technology with the smallest feature size, $0.18\mu m$. The noise increases with decreasing pixel size and increasing vertical resolution and has the best performance in the $0.18\mu m$ technology. The dynamic range decreases with pixel density, but has a strong dependence on the power supply voltage of the technology.

Thesis Supervisor: Charles G. Sodini
Title: Professor of Electrical Engineering

Acknowledgments

After ten and a half years at MIT, I feel indebted to a multitude of extraordinary individuals. This page is by no means complete, as it allows me to thank only a small fraction of those who helped shape my decade at the 'tute.

I would first like to thank my advisor and mentor, Prof. Charlie Sodini, for his guidance and support during the length of this project. His advice and encouragement proved more valuable than any CAD program in the world! I also wish to acknowledge my thesis readers, Prof. Harry Lee and Marc Loinaz, for taking the time to read my thesis. Their many suggestions and challenging questions helped shape this thesis.

Many thanks go to my contemporaries of the Sodini group, Ching-Chun Wang, Pablo Acosta-Serafini, and Don Hitko, for listening, humoring, commiserating, and going to Tosci's at a moment's notice. I am also thankful to the rest of the Sodini/Lee groups for their support and friendship: Ayman Shabra, Kush Gulati, Dan McMahill, Susan Dacy, Mark Spaeth, Mark Peng, and Andy Wang.

I am thankful to Pat Varley for showing me the ropes around the MIT procurement system. I thank Marilyn Pierce and Monica Bell for their friendly reminders about departmental requirements and deadlines. Many thanks go to Myron (Fletch) Freeman and Mike Hobbs for all their help with computer emergencies.

I thank my grad school buddies for making this academic experience a little less academic: Samara Firebaugh, Alice Wang, Joel Voldman, Jeanie Cherng and Debb Hodges-Pabon. I also wish to thank all my 6.012 students (Spring 97 and Fall 99) for inspiring me to seek a career in teaching someday.

I am extremely grateful to my fiance Zony Chen for his love and support, especially during the final stages of this thesis. He played a crucial role in the conclusion of this thesis by cooking for me, driving me to school and staying up with me to ensure I met deadlines.

Most of all I thank my parents, Pedro and Elizabeth Fujimori, for all the sacrifices they made to get me to this point in life. Our journey to America was worth it all!

The author was funded by an NSF fellowship, and a Lucent Technologies and GRPW fellowship. This project was funded by DARPA contract DAAL-01-95-K-3526 and the MIT Center for Integrated Circuits and Systems.

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.