A CMOS Area Image Sensor With Pixel Level A/D Conversion

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Abstract

A CMOS 64×64 pixel area image sensor chip using Sigma-Delta modulation at each pixel for A/D conversion is described. The image data output is digital. The chip was fabricated using a 1.2μm two layer metal single layer poly n-well CMOS process. Each pixel block consists of a phototransistor and 22 MOS transistors. Test results demonstrate a dynamic range potentially greater than 93dB, a signal to noise ratio (SNR) of up to 61dB, and dissipation of less than 1mW with a 5V power supply.

Charge-coupled devices (CCD) are at present the most widely used technology for implementing area image sensors. CCD image sensors have their shortcomings, however. They suffer from low yields, they consume too much power [3], and they are plagued with SNR limitations due to the shifting and detection of analog charge packets, and the fact that data is communicated off chip in analog form.

Several alternatives to CCD area image sensors that use standard CMOS technology have been developed. Self scanned photodiode arrays have been used to produce both binary and grayscale image sensors [2, 3]. Bipolar junction phototransistor arrays [6], and charge injection arrays [5] have also been used. However, these alternatives can suffer from low resolution due to limited pixel observation time, limited SNR due to analog sensing, and as with CCDs, data is communicated off chip in analog form.

In this paper we describe an area image sensor that can potentially circumvent the limitations of CCDs and their alternatives. The proposed image sensor uses a standard CMOS process and can therefore be manufactured with high yield. Digital circuitry for control and signal processing can be integrated with the sensor. Moreover, CMOS technology advances such as scaling and extra layers of metal can be used to improve pixel density and sensor performance.

The analog image data is immediately converted to digital at each pixel using a one-bit Sigma-Delta modulator [1]. The use of Sigma-Delta modulation also allows the data conversion circuitry to be simple and insensitive to process variations [1]. A global "shutter" provides variable light input attenuation to achieve wide dynamic range [2]. Data is communicated off chip in a digital form, thus eliminating the SNR degradation of analog data communication.

To demonstrate the viability of our approach, an area image sensor chip has been designed and fabricated in a 1.2 μm [1] CMOS technology. A functional block diagram of the chip is given in Figure 2. It consists of an array of 64×64 pixel blocks, a clock driver, a 6:64 row address decoder, 64 latched sense amplifiers, and 16 4:1 column multiplexers. The chip also contains data compression circuitry which will not be described in this paper. A die photograph is given in Figure 5 and a summary of the main characteristics of the chip are listed in Table 1.

[1] μ is the symbol for 10^{-6}.

A circuit schematic of the function implemented at each pixel is given in Figure 1. The phototransistor is a vertical bipolar PNP transistor; the emitter is formed using source-drain p+ diffusion, the base is the n-well surrounding the emitter and the collector is the p- substrate. The n-well is exposed to light, while the rest of the circuitry is covered with the second level of metal to reduce the chance of photon induced latch-up. The physical construction and operation of bipolar phototransistors are described in [7, 4]. Control of the input photocurrent is achieved by setting the duty cycle (the ratio between the on and off times) of the shutter input **SHUTTER** — the higher the duty cycle the larger the input photo current. Current from the phototransistor is integrated on **C1** and quantized using a regenerative latch clocked via **PHI2**. The quantized value is converted into a current using a 1 bit D/A converter and fed back to the input capacitor **C1**. The duty cycle of **PHI1** and the voltage **VBIAS1** control the magnitude of the feedback signal Delta. **PHI1** and **PHI2** constitute a two phase nonoverlapping clock. At the completion of each two phase clock cycle a single bit is produced. The bit is read by enabling the word line **WORD**. If the bit is high the precharged bit line **BIT** is pulled down and sensed by a simple single-ended sense amplifier.

The operation of the area image sensor chip is as follows: after an image is focused on the chip the Sigma-Delta modulators are reset via the global **RESET** signal. **SHUTTER** is then globally set to maximize image SNR without saturating the data conversion circuitry. Next the Sigma-Delta modulators are globally clocked at a rate F_s above the image frame rate $2F_d$. This is necessary since a Sigma-Delta modulator reduces quantization error at the cost of extra data. At the end of each clock cycle the outputs of the Sigma-Delta modulators form a 64×64 array of bits referred to as a "bit plane." Each bit plane is read out row by row. The image is fully captured using a number of bit planes determined by the target SNR. Using the theoretical analysis in [1] the number of bit planes L needed versus SNR is given by

$$\text{SNR} = 9 \log_2 L - 5.2\text{dB}.$$

The maximum achievable SNR has been measured at 61dB. SNR degradation due to charge injection of the digital circuitry in close proximity to the analog sensors is negligible since the frequency of operation is very low (1kHz) and the circuitry consumes less than 20nA per pixel.

Figure 3 shows the output from a single pixel's Sigma-Delta modulator

The digitized pixel values are reconstructed using a decimation filter [1]. Depending on the type of application in which the sensor is used, this reconstruction may be implemented in software, using special purpose hardware external to the sensor, or integrated with the sensor. In a low resolution application where no local reconstruction is needed, e.g. video phone or surveillance camera, the sensor digital output is compressed and immediately transmitted. Reconstruction is done at the receiving end using general or special purpose hardware. If the image is to be displayed or processed locally one or more decimation filters are integrated with the sensor and an external RAM is used. The pixel values stored in the RAM are recursively updated by reading them into the sensor, updating their values using the decimation filters and the new bits from the corresponding sigma delta modulators, and storing the new values back into the RAM. This scheme appears feasible even for a sensor with as many as 1 million pixels operating at 30 frames per second at 8 bits per pixel resolution.

The sensor can achieve a dynamic range[2] potentially greater than 93dB. This is because the magnitude of the photocurrent can be varied by a factor of 1000, or 60dB, and the maximum measured SNR is approximately 33dB with the **SHUTTER** duty cycle set at 100%, the frame sampling rate set at 30Hz, and the oversampling ratio set at 64.

Figure 4 shows a scan from a 35mm print, and the image obtained by the sensor when contact exposed to the 35mm negative.

The sensor's estimated total power of less than 1 mW is significantly lower than that of other types of image sensors.

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