A 128 × 128-Pixel Standard-CMOS Image Sensor with Electronic Shutter

Chye Huat Aw and Bruce A. Wooley, *Fellow, IEEE*

Abstract—A 128 × 128-pixel image sensor with a 20 s–10^{-4} s electronic shutter has been integrated in a 1.2-μm digital CMOS technology. The pixel cell consists of four PMOS transistors and a photodiode with antiblooming suppression. Each pixel measures 24 μm by 24 μm and has a fill factor of 25%. Current is used to transfer pixel signals to the column readout amplifiers in order to minimize voltage swings on the highly capacitive column lines. Correlated double sampling is used to reduce intracolumn fixed pattern noise. The saturation voltage is 470 mV. The peak output signal to noise ratio is 45 dB, and the optical dynamic range is 56 dB. The frame transfer rate is 1.7 ms per frame.

I. INTRODUCTION

GROWTH in the market for multimedia systems has generated an increasing demand for image acquisition systems that are able to directly import both video and photographic images into personal computers. Currently, such systems are usually implemented using charge-coupled device (CCD) technology. However, CCD imagers have several disadvantages [1], [2]. First, although efforts have been made to integrate signal processing circuits together with CCD imaging arrays [3], [4], the CCD fabrication requirements can be incompatible with the fabrication yield and performance needed to implement large amounts of on-chip signal processing. Second, they require near perfect charge transfer between pixels in order to maintain signal integrity, and the charge transfer requirement becomes even more stringent as the array size increases. Finally, CCD arrays typically require the use of relatively high voltages, which is not compatible with deep-submicron VLSI technology. Notwithstanding their limitations, CCD technologies currently allow the implementation of imagers with much smaller pixels than can be achieved with alternative approaches.

To overcome the limitations of CCD imagers, attention is increasingly being focused on the possibility of implementing imaging arrays in standard CMOS technologies [5]–[11]. CMOS image sensors with integrated signal processing have been implemented for a number of applications [12], [13]. Most current CMOS imaging arrays have been designed for video applications, while less attention has been given to arrays designed specifically for digital photography.

This paper describes the design and implementation of a prototype 128 × 128, active-pixel, standard-CMOS, still-image sensor suitable for digital photography applications that do not require the resolution of conventional film photography.
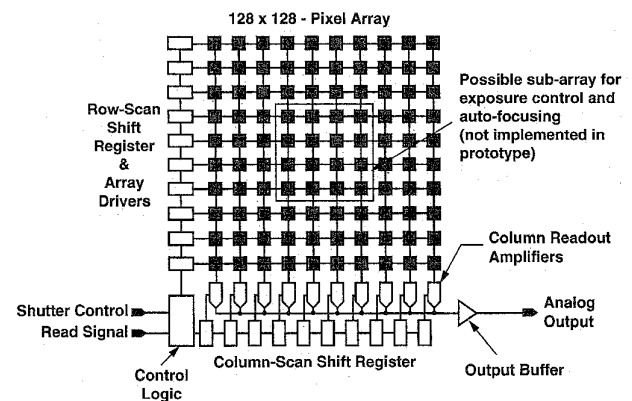
Fig. 1. Image sensor architecture.

Objectives in the design of this circuit included 1) implementation in a standard digital CMOS technology, 2) a single 5-V power supply, 3) an electronic shutter with a wide range of exposure times, and 4) a readout speed fast enough for 640 × 480-pixel video at 30 frames per second. Additional goals were a large dynamic range, low fixed pattern noise, low lag, antiblooming, low smear, and a fill factor greater than 20%. While state-of-art CCD sensors often include an electronic shutter capability, this feature typically requires the use of relatively high voltages.

The prototype array was designed for implementation in a 1.2-μm, n-well CMOS process without the use of analog-specific components such as capacitors. Although designed for gray-scale imaging, the array can easily be adapted for color imaging through the addition of color filters to the CMOS process. The cost and complexity of the additional processing would be the same as that required for other types of integrated color image sensors. Adopting the design for video, rather than still image, applications is only a matter of redesigning the control logic to implement the proper timing control.

II. ARCHITECTURE

The architecture of the proposed image sensor is shown in Fig. 1. The core of the sensor is a 128 × 128 array of four-transistor active pixels. In response to input signals such as the *Shutter Control* and *Read Signal*, a control logic unit generates the internal signals needed to perform such tasks as opening the electronic shutter, scanning the array, and correlated double sampling readout. Row- and column-scan digital shift registers are used to generate the signals used to scan the rows and
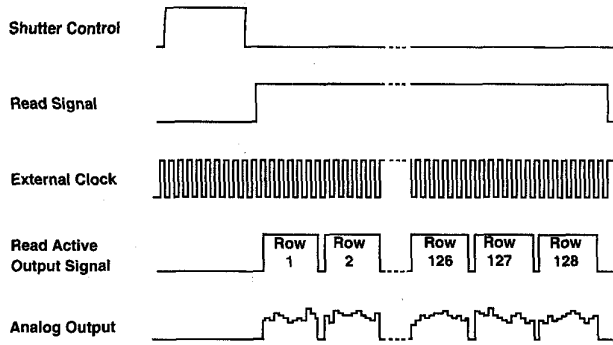
Fig. 2.   Single frame exposure and readout sequence.

Fig. 3.   Pixel circuit schematic.

Fig. 4.   Pixel cross-section view showing antiblooming structure and metal2 light shield.

columns, respectively, during readout. Each column of the array has a column readout amplifier that generates an analog output voltage proportional to the gray scale intensity of the image. An output buffer is used to drive external loads.

A feature that can be easily implemented in the sensor, but was not included in this prototype, is the ability to read out a subarray of the image. Such a subarray can be used for exposure control and autofocusing prior to capturing the photograph. Image aspect ratio switching [3] can also be implemented easily.

Incident light on each pixel of the imager generates a photocurrent that is integrated and stored as a voltage. Photo-integration is performed simultaneously on the entire array. A transconductance buffer in the pixel converts the stored voltage into a current that is read out on the column line. The use of a current-mode readout minimizes the voltage swings required on the highly capacitive column lines. Each column readout amplifier converts the current-mode signal from the selected pixel into an offset-compensated analog voltage sample that is multiplexed out sequentially.

Fig. 2 illustrates the exposure and readout sequence for a single frame. Note that the timing is not to scale; the *Shutter Control* pulse is usually much longer than the readout timing. The *Shutter Control* and *Read Signal* provide the external control of the image sensor. The pixel array is held in a reset state until *Shutter Control* goes high. The electronic shutter is then "opened" for the duration of the *Shutter Control* pulse, thereby exposing the image. When the *Shutter Control* goes low, the electronic shutter is closed and readout commences on the assertion of *Read Signal*. The first row is activated and the signals in all pixels of that row are simultaneously read out and sampled by the column readout amplifiers. After settling, the sampled signals are sequentially multiplexed out through the output amplifier. The output signals are synchronized with the *External Clock*. Readout proceeds from row to row until the entire array has been scanned. The *Read Active Output Signal* indicates the duration of valid signals to facilitate external acquisition of the output data.

III. CIRCUIT DESIGN

A. Pixel Structure and Circuit

In order to achieve a small pixel size, only a single type of MOSFET is employed within the pixel. For reasons explained
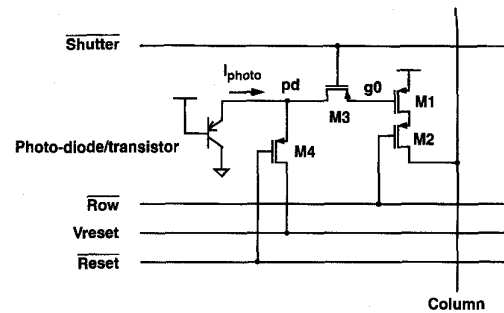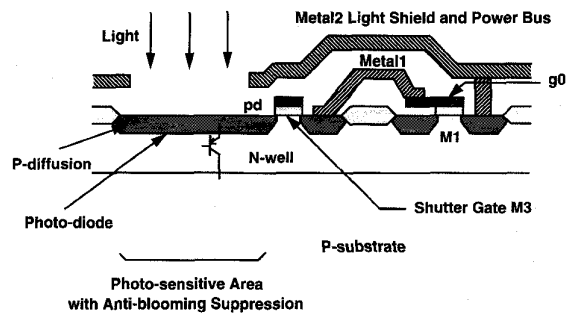
later in this section, the use of p-diffusion/n-well junctions as the photodiodes provides the benefit of antiblooming suppression. Therefore, PMOS transistors are used in the pixel.

Fig. 3 shows the circuit schematic of a pixel. It consists of four PMOS transistors and a photodiode. Transistor $M1$ acts as a transconductance buffer that converts the voltage at node $g0$ into a current, $M2$ is the row access transistor, $M3$ is the shutter transistor and $M4$ is the reset transistor. The pixel design, with the exception of the transconductance buffer, is similar to that described in [7]. The vertical column lines in the array are implemented using second-layer metal, while first-layer metal is used for the horizontal row lines. The VDD power bus is realized in second-layer metal and covers all active areas of the pixel except the photodiode.

Prior to the exposure of a frame, $M3$ and $M4$ are on, resetting nodes pd and $g0$ to V_{reset}. This reset action is fast and complete, resulting in low lag for rapidly changing frames. During exposure, $M4$ is turned off while the shutter transistor $M3$ remains on. The photocurrent is integrated onto the parasitic capacitances at nodes $g0$ and pd. The shutter is closed by turning off $M3$. The photosignal is stored as a voltage on node $g0$. During readout, the row access transistor $M2$ is turned on, and the drain current of $M1$ is fed via the column line to the column readout amplifier.

A cross-sectional view of a pixel is presented in Fig. 4. To achieve antiblooming, a p-diffusion/n-well junction is used as the photodiode so that excess charges generated by strong incident light will be drained away by the vertical substrate PNP bipolar action. This prevents the excess charges from leaking to neighboring pixels, to node $g0$ within the pixel, or
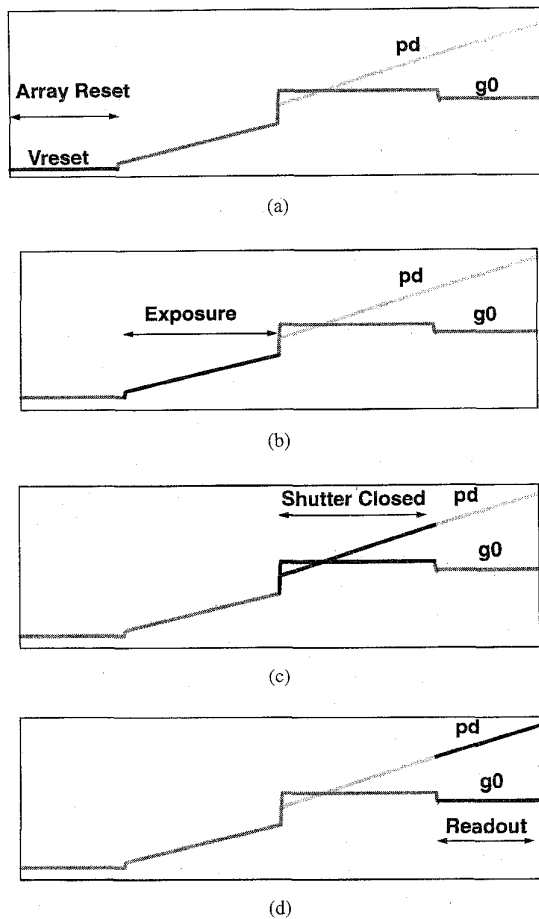
Fig. 5. Waveforms at nodes pd and $g0$ in the pixel during: (a) array reset, (b) exposure, (c) shutter closed, and (d) readout.

C1, C2, and Cc are MOSFET capacitors
B1, B2, and B3 are source followers

Fig. 6. Column readout amplifier.

directly to the *column* line through the output drain of the row access transistor $M2$. In addition to bringing in V_{DD}, the Metal2 power bus serves as a light shield that covers all active areas of the sensor and prevents unwanted photo-integration at node $g0$ when the shutter gate is off. This light shield also helps to achieve low smear. Outside the active regions, Metal2 is used to implement interconnects. Each pixel measures 24 μm by 24 μm and has a fill factor of 25%.

B. Pixel Operation

Fig. 5 shows the waveforms at nodes pd and $g0$ during an exposure cycle. The pixels in a row are reset by holding both $\overline{Reset}$ and $\overline{Shutter}$ low, turning on $M3$ and $M4$. The voltages at nodes pd and $g0$ are thereby reset close to V_{reset}. There is a small voltage drop across transistor $M4$ during reset because light is continuously incident on the photodiode, which induces a positive photo current. If this voltage, which is the drain-to-source voltage of $M4$, is small, it is given approximately by

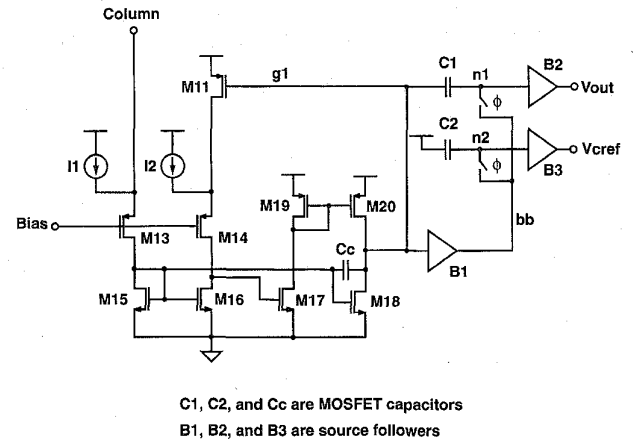$$V_{DSM4} = \frac{I_{photo}}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_T)}. \qquad (1)$$

The small-signal drain-to-source resistance of $M4$ is nominally 18 kΩ, while I_{photo} is typically less than 1 pA. Thus, V_{DSM4} is less than 18 nV and can be neglected.

During exposure $\overline{Reset}$ goes high, turning $M4$ off, while $\overline{Shutter}$ remains low, so that $M3$ remains on. The photocurrent is then integrated onto the parasitic capacitances at pd and $g0$. At the end of the exposure period, $\overline{Shutter}$ goes high, turning off $M3$ and cutting off the photocurrent into node $g0$. While the voltage at pd continues to rise, $g0$ holds a voltage proportional to the intensity of light falling on the pixel's photodiode. A positive offset in the voltage at $g0$ is induced by charge injection that results from turning off $M3$. To the first order, this offset is cancelled by the correlated double sampling used in the readout amplifier.

Readout is initiated when $\overline{Row}$ goes low, turning on $M2$. The voltage at the drain of $M1$ falls from V_{DD} to the bias voltage of the *column* line, and this change couples a small negative offset into node $g0$. The drain current of $M1$ is fed via the *column* line to the column readout amplifier.

C. Column Readout Amplifier

Fig. 6 is a schematic of the column readout amplifier. The design of this amplifier provides a low impedance load for the column line, converts the readout current from the selected pixel into a voltage that is proportional to the integrated photovoltage in the pixel, uses correlated double sampling to achieve low fixed pattern noise, and provides a column output reference voltage to reduce output voltage offset due to charge injection mismatch and bias ambiguity.

$M13$ operates as a common-gate transistor so as to provide a low impedance load for the column line, thereby reducing the voltage swing required on the column. The current from the selected pixel is mirrored by the current mirror formed by $M15$ and $M16$. The negative feedback loop implemented by transistors $M17$–$M20$ forces the V_{DS} of $M16$ to be very close to that of $M15$. $M11$ replicates the transconductance buffer transistor, $M1$, in the pixel cell, and the $M15$–$M16$ current mirror forces the incremental current flowing through $M11$ to be the same as that in the selected pixel. The closed loop provided by the $M17$–$M20$ amplifier produces a voltage
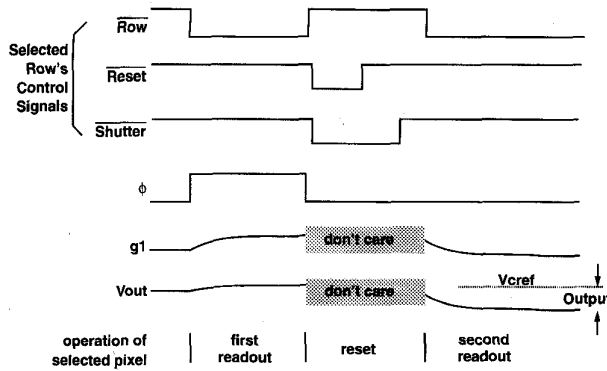
Fig. 7. Correlated double sampling of a single row.

Fig. 8. Actual implementation of MOSFET-capacitors and adaptive biasing in column readout amplifier.

at node $g1$ that is proportional to the voltage at node $g0$ in the pixel.

As mentioned earlier, correlated double sampling is implemented in the readout process. The diagram in Fig. 7 illustrates the timing sequence of the double sampling for a single row. During the first readout period, the row access transistor, $M2$, in the selected pixel is turned on and the photovoltage at $g0$ in the pixel is proportionally reproduced at $g1$ in the column readout amplifier. This voltage is sampled onto $C1$ when clock ϕ is high. Node $n1$ at the other terminal of $C1$ is biased to the voltage at node bb which varies with the voltage at $g1$. As will be explained later, this biasing scheme is used to ensure the proper biasing of $C1$ and $C2$, which are implemented with MOSFET's. $C2$ is added to provide a memory of the bias voltage so as to serve as a reference for the final output signal. After ϕ goes low, the selected row of pixels is first disconnected from the *column* lines and then reset. The reset operation follows exactly the same sequence of $\overline{Reset}$, $\overline{Shutter}$, and $\overline{Row}$ signals during array reset and exposure so as to obtain, to first order, the same charge injection. The selected pixels are then read out again. This produces a voltage at $g1$ corresponding to the reset value at $g0$ in the pixel. The output signal is the final difference between V_{cref} and V_{out} in Fig. 6.

Since a goal of this design is to use only components available in a standard digital CMOS technology, the capacitors have been implemented with MOSFET's biased in the inversion region. If the MOSFET-capacitors are to remain properly biased for different signal levels and process parameters, a fixed bias voltage cannot be used at node bb in Fig. 6. Consequently, an adaptive biasing approach has been adopted. Fig. 8 is a circuit schematic of the actual implementation of the MOSFET-capacitors and the adaptive biasing. Node bb is biased to a voltage that varies with the voltage established at $g1$ when ϕ is high. The source follower $B1$ in Fig. 6 is formed by $M21$, $M22$, and $I3$. This circuit serves both as a buffer and a voltage level translator to ensure that $C1$ and $C2$ are biased in strong inversion.

Without adaptive biasing, the bias voltage would have to be low enough so that $C1$ and $C2$ would remain in strong inversion when the voltage at $g1$ is low, corresponding to low light intensity. However, this level of bias would not work properly for double sampling a pixel with strong light intensity. In such a case, the first readout of the double
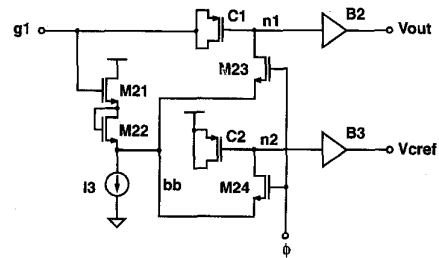
sampling sequence produces a high voltage at $g1$, while the second readout produces a low voltage corresponding to the reset value. This results in the top plate (gate) of $C1$, node $n1$ in Fig. 6, being pulled below ground during readout of the pixel reset level. The drain-to-well junction of $M23$ would then be forward biased and $C1$ would be discharged. Adaptive biasing avoids this problem by moving the biasing voltage higher with higher $g1$ voltage.

V_{cref} provides a reference output level that compensates for the bias adjustment. It also serves to provide a local reference voltage so as to compensate for nonuniformities among the column readout amplifiers, such as mismatch in the source-follower buffers $B2$ and $B3$ and the charge injection in the switches.

D. Column Biasing

A common-source transconductance stage such as $M1$ in the pixel cell is normally biased in the saturation region so as to achieve the maximum gain. However, in this image sensor, the column lines are biased at a high voltage in order to keep the pixel transconductance buffer $M1$ in the linear region during readout. Three reasons for this are as follows. First, in order to achieve a large dynamic range, V_{reset} in the pixel should be low. However, this will result in large readout current if $M1$ is operating in the saturation region, since a low V_{reset} corresponds to a large V_{GS} for $M1$. Increasing the channel length of $M1$ will reduce the readout current but will result in higher parasitic capacitance at node $g0$ in the pixel because of the increased gate capacitance, reducing the photosensitivity of the pixel. Therefore, $M1$ is operated in linear region so as to achieve lower readout current and power consumption. Second, if $M1$ operates in the saturation region, the readout current will vary widely with process variations. If $M1$ is biased in the linear region, its V_{DS} can be controlled so as to compensate for such variations. Finally, biasing the column lines at a relatively high voltage provides a large voltage range at the input to the column readout amplifier, allowing more flexibility in its design.

Fig. 9 shows how the biasing of the column lines is accomplished. $MB1$ and $MB2$ in the bias generator mirror the transistors $M1$ and $M2$ in the pixels. $MB3$ and $IB1$ mirror $M13$ and $I1$ in the column readout amplifiers. The transistor sizes and current sources in the column bias part of the bias generator are four times those in the column readout amplifiers and the pixels in order to provide a low impedance drive for
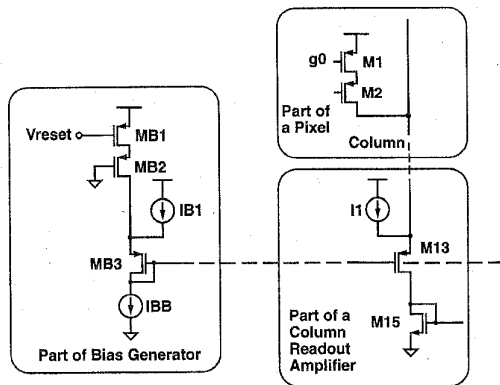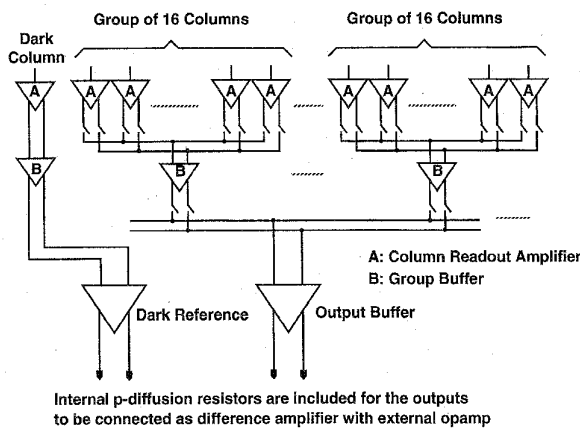
Fig. 9. Column biasing implementation.

Fig. 11. Column-scan shift register clocking.

Fig. 10. Buffering in the output signal path.

the bias line. By setting an appropriate value of I_{BB}, the bias circuit establishes the voltage on *column* line, and therefore the drain current of $M1$ when $M2$ is on. I_{BB} is provided by an on-chip bias current generator that is designed to be relatively insensitive to process variations.

E. Buffering in the Output Signal Path

If the column readout amplifier buffers, $B2$ and $B3$ in Fig. 6, were to drive the analog output buffer in Fig. 1 directly, their sizes and power consumption would need to be quite large because of the large loading capacitance of the signal path. To overcome this, intermediate buffering is used. The readout amplifiers are divided into groups of 16, each with an intermediate buffer that drives the output buffer as depicted in Fig. 10.

The image sensor array also includes a dark reference column in which the pixels' photosensitive areas are completely covered by the Metal2 light shield. During testing, the dark reference was connected to an external difference amplifier and subtracted from outputs of the light-sensitive pixels. While an external difference amplifier was used for this prototype, the amplifier could be included on-chip in future designs.

F. Minimizing Digital Noise Coupling

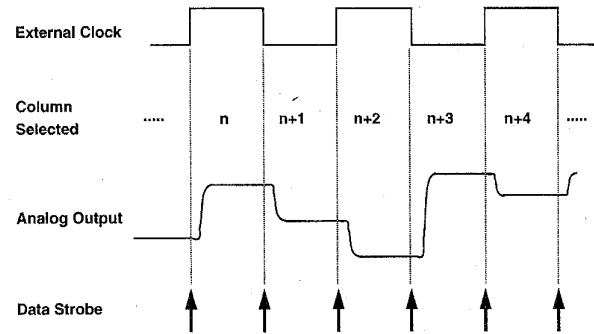Noise coupling from digital circuits into analog signal paths is a major concern in mixed-signal circuit design [14]. In the prototype imager, several design techniques have been used to minimize digital transitions during the settling of analog signals. First, the internal clock generator that provides the two-phase clocks for driving the scanning circuits is disabled until readout commences. This provides an environment that is almost free of digital noise during the array reset and exposure operations.

Second, to minimize coupling into analog circuits via the substrate, the on-chip traces of the external clock are shielded with grounded metal lines. The shielding ground is fed directly off the chip to minimize coupling into the on-chip analog and digital grounds.

Finally, in order to avoid a clock transition during the analog settling period, the digital shift register used to scan the columns is designed to shift at each edge of the external clock. Each pixel's output is accessed for half the period of the external clock, which has a 50% duty cycle. The outputs of the odd and even columns are strobed on the positive and negative edges of the external clock, respectively, and the analog output rate is thus twice the external clock frequency. Circuit nodes in the shift register change state only on the transitions of the external clock, thus eliminating digital switching during analog signal settling period.

Fig. 11 illustrates the analog output signal and the strobing of the output data relative to the external clock transitions. Fig. 12 shows the implementation of the column-scan shift register. Fig. 12(b) depicts a register cell, which is used to access two adjacent columns. Data is shifted into the cell at the *In* terminal and shifted out of the cell at the *Out* terminal. Bc, which is an output that feeds into the Nc input terminal of the preceding cell, disables the preceding column when the current column is selected. $S1$ and $S2$ are the select signals for the two columns served by the register cell. As a digital "1" is shifted into the cell from the left, $S1$ goes high when $\phi1$ goes high. When $\phi1$ falls, $S1$ goes low and $S2$ goes high, selecting the next column, as $\phi2$ transitions high. $\phi1$ and $\phi2$ are generated from the external clock by an internal two-phase nonoverlapping clock generator.

G. Layout

The experimental image sensor has been fabricated in a 1.2-μm CMOS technology. A die photograph of this circuit is shown in Fig. 13. The digital row-scan shift register and array

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.