EXHIBIT 1052

U.S. PATENT NO. 5,892,540 TO KOZLOWSKI *et al.*

("the '540 Patent" or "KOZLOWSKI")

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PETITION FOR *INTER PARTES* REVIEW
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Kozlowski et al.

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[54] **LOW NOISE AMPLIFIER FOR PASSIVE PIXEL CMOS IMAGER**

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[51] **Int. Cl.**[6] **H04N 5/217**; H04N 5/335

[52] **U.S. Cl.** **348/300**; 348/241; 348/308; 348/310; 250/208.1

[58] **Field of Search** 330/86, 282, 308; 348/207, 222, 241, 243, 244, 245, 250, 294, 302, 303, 307, 308, 309, 310, 300, 301; 250/208.1; H04N 5/335, 5/217

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,387,402	6/1983	Lewis	358/213
4,786,831	11/1988	Morse et al.	307/490
5,043,820	8/1991	Wyles et al.	358/213.28
5,153,421	10/1992	Tandon et al.	250/208.1
5,296,696	3/1994	Uno	250/208.1
5,345,266	9/1994	Denyer	348/300
5,349,380	9/1994	Stein	348/250
5,461,425	10/1995	Fowler et al.	348/294
5,619,262	4/1997	Uno	348/297
5,734,191	3/1998	Chi et al.	257/462
5,751,189	5/1998	Shyu et al.	330/9

OTHER PUBLICATIONS

Degrauwe et al., "A Micropower CMOS–Instrumentation Amplifier," *IEEE Journal of Solid–State Circuits*, vol. SC–20, No. 3, pp. 805–807, Jun. 1985.

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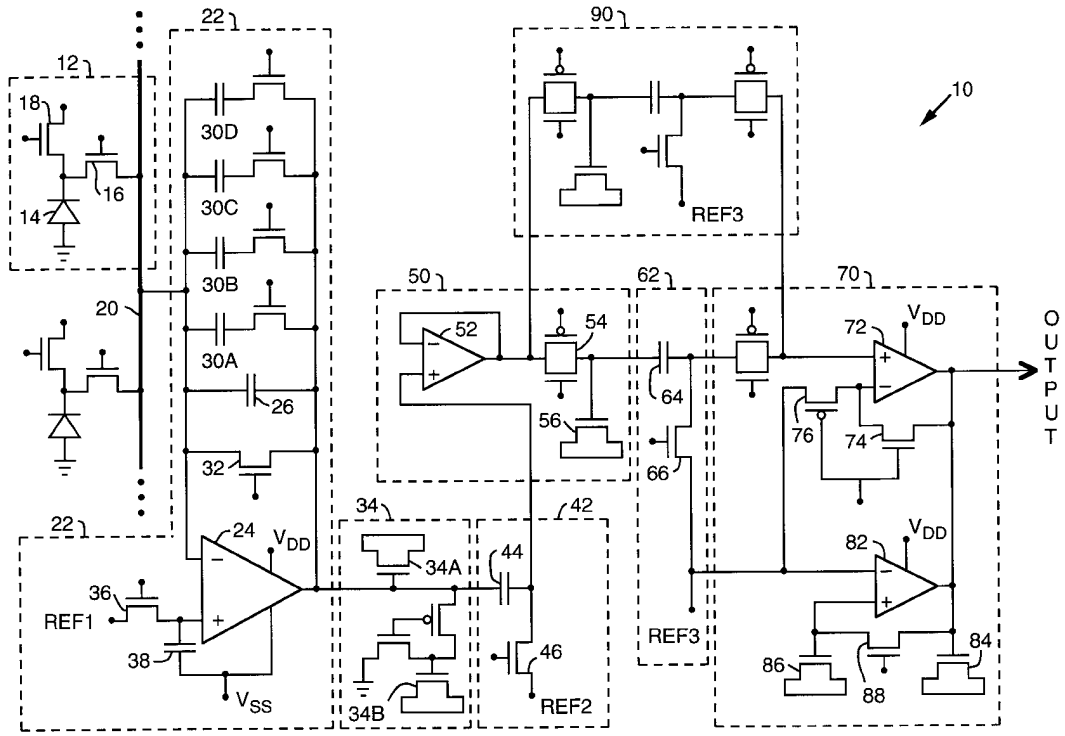
[57] **ABSTRACT**

A CMOS imaging system provides low noise read out and amplification for an array of passive pixels, each of which comprises a photodetector, an access MOSFET, and a second MOSFET that functions as a signal overflow shunt and a means for electrically injecting a test signal. The read out circuit for each column of pixels includes a high gain, wide bandwidth, CMOS differential amplifier, a reset switch and selectable feedback capacitors, selectable load capacitors, correlated double sampling and sample-and-hold circuits, an optional pipelining circuit, and an offset cancellation circuit connected to an output bus to suppress the input offset nonuniformity of the amplifier. For full process compatibility with standard silicided submicron CMOS and to maximize yield and minimize die cost, each photodiode may comprise the lightly doped source of its access MOSFET. Circuit complexity is restricted to the column buffers, which exploit signal processing capability inherent in CMOS. Advantages include high fabrication yield, broadband spectral response from near-UV to near-IR, low read noise at HDTV data rates, large charge-handling capacity, variable sensitivity with simple controls, and reduced power consumption.

20 Claims, 2 Drawing Sheets



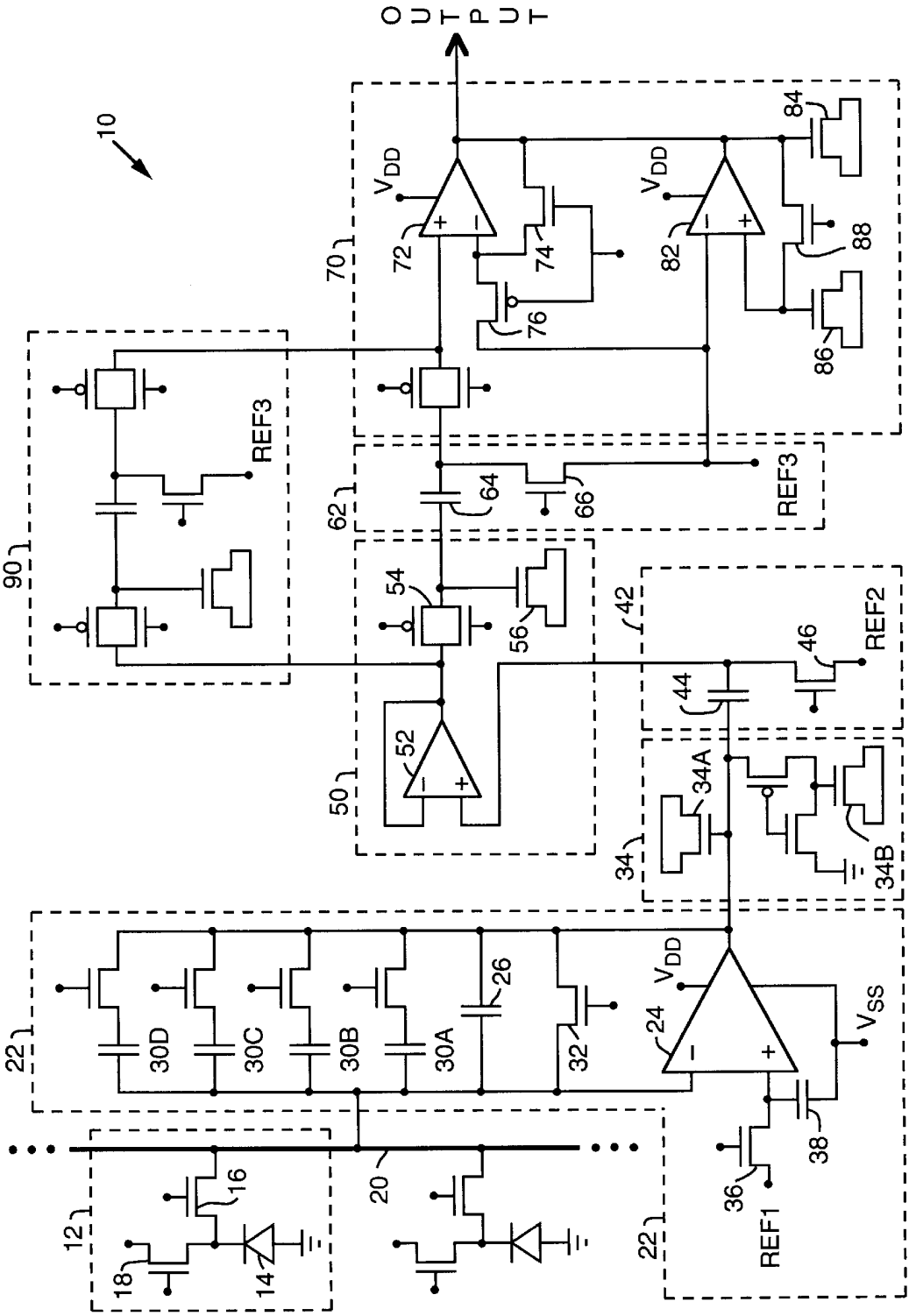


Figure 1

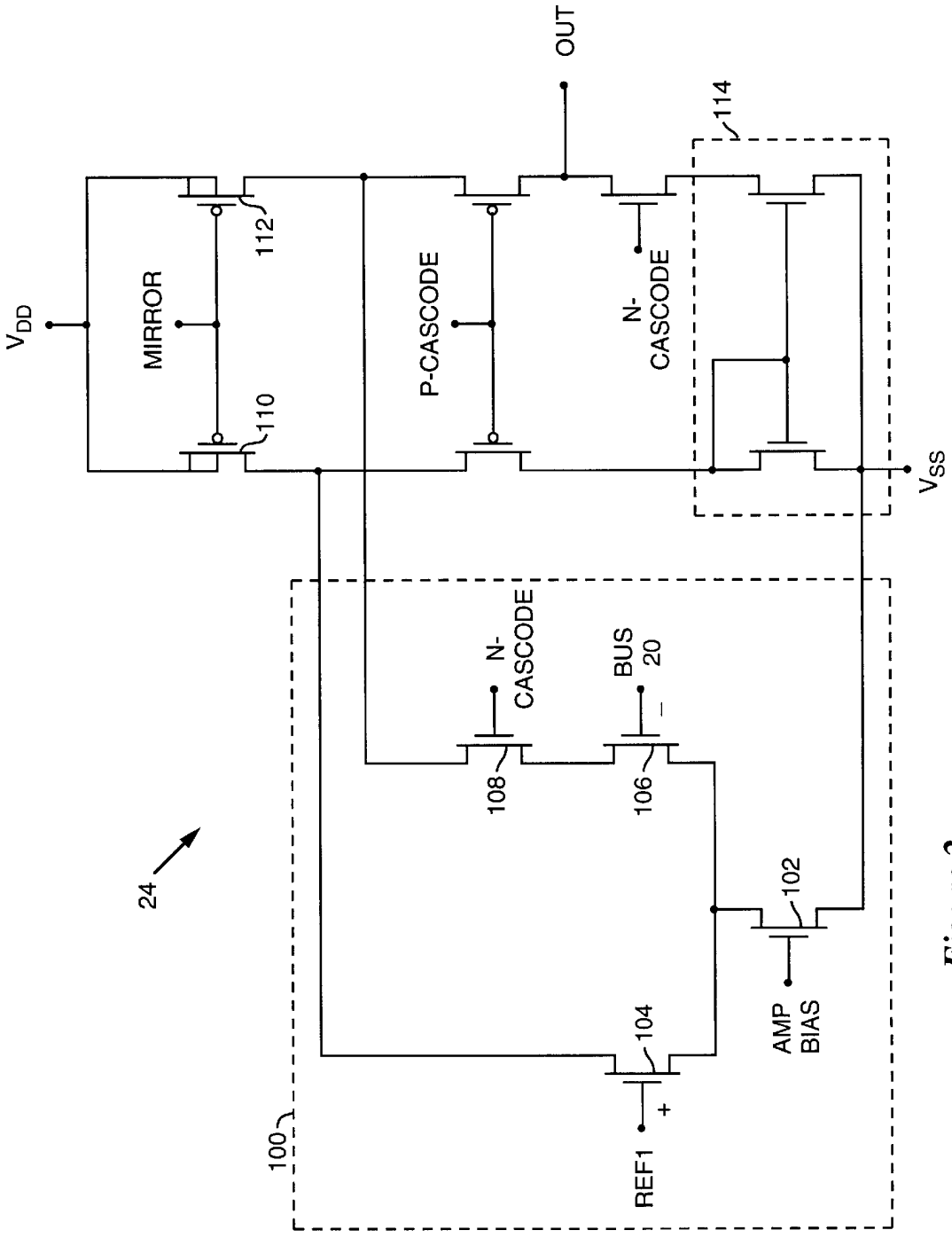


Figure 2

LOW NOISE AMPLIFIER FOR PASSIVE PIXEL CMOS IMAGER

TECHNICAL FIELD

The present invention relates to electronic imaging devices and, in particular, to a low noise amplifier system having charge integrating column buffers for a passive pixel CMOS imager.

BACKGROUND OF THE INVENTION

Most currently available video cameras use charge coupled devices (CCDs) for generating video images. Although these cameras are suitable for many applications, the relatively high cost of CCD-based camera technology limits its use in high volume commercial markets, such as personal computer teleconferencing, for example.

The higher cost of CCD camera systems results from a combination of factors, such as many mask levels for CCD processes; lower yields for the photosensor due to high complexity; shared pixel real estate for the photosensor and CCD shift register, which requires micro-optics or alternative die-area doubling frame transfer schemes (or otherwise limits the optical fill factor); front-illuminated designs that may require photodetection through overlying polysilicon layers, which generally degrade response in the blue and near-UV regions of the spectrum; complex interface and signal processing electronics that may not be compatible with battery operation; support electronics functions that are not readily integrated onto the CCD imager; and interface electronics that require high voltage clock drivers and DC biases to operate the CCD and the video signal conditioning amplifier (including correlated double samplers and other circuitry needed to manipulate the video into the proper protocol).

Various MOSFET-based alternatives to CCD sensors are also known in the prior art for lower cost applications. Hitachi, for example, has produced a MOS-based photodiode imaging array for high-volume applications, including camcorders (Hitachi Part No. HE98221). This basic scheme, commonly referred to as a passive pixel sensor, typically includes an array of pixels connected to an amplifier by horizontal and vertical scanners. Each passive pixel (i.e., having no pixel-based amplification) comprises a silicon photodiode and a pixel access transistor.

Early passive pixel devices fabricated using n-MOS technology were not competitive with emerging CCD-based imagers, except for niche applications such as spectrometry, because the read noise (including blooming and fixed pattern noise) was too high. Furthermore, the circuitry servicing each column did not adequately extract the low-level signal current in the presence of switching noise, vertical smear noise, and random noise. The column buffer, generally comprising a bipolar transistor in emitter follower configuration with a correlated double sampler, typically yielded temporal and fixed pattern noise that was about an order of magnitude higher than that produced by competing CCDs. Nevertheless, companies such as EG&G Reticon continue to produce MOS photodiode arrays having passive pixel designs with various multiplexing schemes.

The advantage of producing imagers using conventional MOS fabrication technologies, rather than esoteric CCD processes requiring many implantation steps and complex interface circuitry, has led to successive improvements. The column buffer was refined by using an enhancement-depletion inverter to provide greater amplification with a small area of wafer "real estate." The amplifier gain effectively reduced the column capacitance, and thus suppressed kTC noise and pattern noise. Low-light level performance was improved by about a factor of three (to a minimum scene illumination of 40 lux) relative to previous MOS imagers.

Subsequently, amplification was relocated to the pixel by means of a phototransistor. Cell-based amplification imagers are sometimes referred to as active pixel sensors. The Base-Stored Image Sensor (BASIS) used a bipolar transistor in emitter follower configuration, with a downstream correlated sampler, to suppress random and temporal noise. By storing the photogenerated signal on the phototransistor's base to provide cell-based charge amplification, the minimum scene illumination was reduced to 10^{-3} lux in a linear sensor array. The minimum scene illumination was higher ($\approx$0.01 lux) in a related two-dimensional BASIS imager having 310,000 pixels because the photoresponse nonuniformity was relatively high ($\leqq$2%). Although this MOS imager had adequate sensitivity, the pixel pitch was considered too large (at about 13 μm).

An active pixel sensor comprising a three-transistor pixel is described in U.S. Pat. No. 5,296,696 (Uno). The cell-based source-follower amplifier is augmented with a CMOS column buffer providing fixed pattern noise cancellation. In this scheme, at least one of the three transistors in the pixel is relatively large to minimize amplifier 1/f noise. A large S/N ratio with low pattern noise can be achieved, but the pixel optical fill factor is relatively small.

A compact passive pixel image sensor that can be fabricated using various technologies, including CMOS, NMOS, Bipolar, BiMOS, BiCMOS, or amorphous silicon, is described in U.S. Pat. No. 5,345,266 (Denyer). Denyer buffers the output signal from the passive pixels with charge-integrating column amplifiers to extract the signal from each pixel. However, Denyer does not disclose circuitry to minimize vertical streak noise, minimize random thermal noise, suppress fixed pattern noise, or improve testability.

Because of the complexity and relatively high cost that limit use of CCD-based imaging systems in high volume commercial markets, and the limitations of prior art active and passive pixel sensors, there is a need for new electronic imaging systems that offer significant reductions in cost and power requirements. Because the amplification requirements of a sensor system are quite formidable, considering the small charge originating at each pixel within an array, the amplifier design, whether realized in on-chip or external circuitry, must be rather sophisticated.

SUMMARY OF THE INVENTION

The present invention comprises a low noise readout system for a CMOS imager. The system provides low noise amplification for an array of passive pixels, each of which comprises a photodetector, an access MOSFET to read the signal and multiplex the outputs from the array of pixels, and a second MOSFET that serves as a signal overflow shunt and a means for electrically injecting a test signal. In a typical two-dimensional array, multiplexing may be performed by horizontal and vertical shift registers, for example, as is known in the prior art. The low noise amplifier of the present invention forms a column buffer for reading out each column (or row) of pixels. The low noise column buffer comprises a robust CMOS capacitive transimpedance amplifier (CTIA), gain-setting feedback capacitors, selectable load capacitors, correlated double sampling and sample-and-hold circuits, an optional pipelining circuit, and an offset cancellation circuit connected to an output bus to suppress the input offset nonuniformity of the amplifier.

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