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Single-Chip Image Sensors With a Digital Processor Array

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Abstract. The architectures, implementation and applications of two smart sensors, LAPP and PASIC, are described. The basic idea of these two designs is to integrate an image sensor array with a digital processor array in a single chip. The integrated camera-and-processor eliminates the bottleneck of sequential image read-out that characterizes conventional systems. They provide fast, compact and economic solutions for tasks such as industrial inspection, optical character recognition and robot vision.

1. Introduction

Embedding of parallel processors in a sensing chip, a smart vision sensor, is an emerging area of image sensor development. Smart sensors will play a significant role in industrial applications. However, commercially available image sensors today are developed mainly for television. Such sensors have excellent sensitivity, high resolution, can handle colors and have excellent reliability. Their pixel read-out architecture, fixed frame rate and fixed resolution have a number of drawbacks for many industrial applications. The *pixel-by-pixel* architecture limits the speed and flexible use of the sensor information.

High speed image processing can be achieved by line-by-line or frame-by-frame parallel processing. A single chip solution is necessary, otherwise a large number of pads will be needed in a line-by-line or *frame-by-frame* parallel image processor architecture. It is therefore desirable to incorporate the sensor array and the processor array on a single chip. This will provide a mechanism to concurrently perform computations previously intractable in real-time. The continuous progress of VLSI technology has provided this opportunity.

Some excellent work on photo-sensor arrays with analog processing inspired by biological retinas has been performed by Carver Mead [1]. The basic idea is to include a simple and dedicated analog signal processor for each sensor element in a single chip. This frame-by-frame analog signal processing provides very

CCD image sensor array integrated with an linear array of CCD analog processors to perform a simple edge detection algorithm line-by-line in real time [2]. By utilizing the ability of CCD technology that can sum and split charge packages, parallel convolutions with fixed coefficients are realized. However, these analog implementations are too specialized and do not have the flexibility to be tailored for different applications.

An alternative approach is to integrate a sensor array with a programmable digital processor array on a single chip. An experimental chip has been developed using 3-D technology [3]. The device consists of a 5-by-5 photo sensor array, a 5-by-5 2-bit CMOS A/D converter array, a 2-bit ALU array and shift registers arranged in a 3-layer structure. The size of a pixel is 1.05×1.05 mm^2. Signals from the photo diodes are transferred to the 2-bit A/D converters. The quantized digital data is then transferred to the third layer, the ALUs. Finally, the processed signals are read out with shift registers. The image sensing, quantization and data processing of all pixels are operated simultaneously frame-by-frame. This frame-by-frame architecture allows extremely high speed image processing. However, the low area resolution, the low signal amplitude resolution and the very high I/O bandwidth demands in this design are severly limiting the applications.

This article will describe the architecture, implementations and applications of two smart sensors, LAPP and PASIC. They provide fast, compact and economic solutions to tasks such as industrial inspection,

2 will describe the LAPP system which is designed for fast binary image processing. A smart sensor, PASIC, whose architecture is an expanded version of LAPP to an enhanced bit-serial processor array with a resolution programmable A/D converter array, is described in Section 3. Sections 4 and 5 discuss their similarities and differences. Finally, further development and trends will be discussed in Section 6.

2. LAPP — Linear Array Picture Processor

The first attempt of integrating an image sensor array and a processor array on a single chip was made several years ago at Linköping University, LAPP, [4], [5]. Figure 1 shows the photograph of the LAPP1100, which is a commercial version and having 128 photo sensor elements, 128 threshold units for digitization and a 128 bit-serial processor in a single chip. The chip size is 5×7 mm^2 using a 3μm CMOS technology.

2.1. LAPP Architecture

The block diagram of LAPP is shown in figure 2. The linear photo diode array (PD) uses threshold circuitry to communicate image information to a 128 bit internal bus. The register array (R0–R13) stores images and intermediate results. The computing units GLU, NLU, PLU perform the image operations. Results are passed on to the accumulator. From there the result is either stored in a register, or used as the second operand in two-operand instructions.

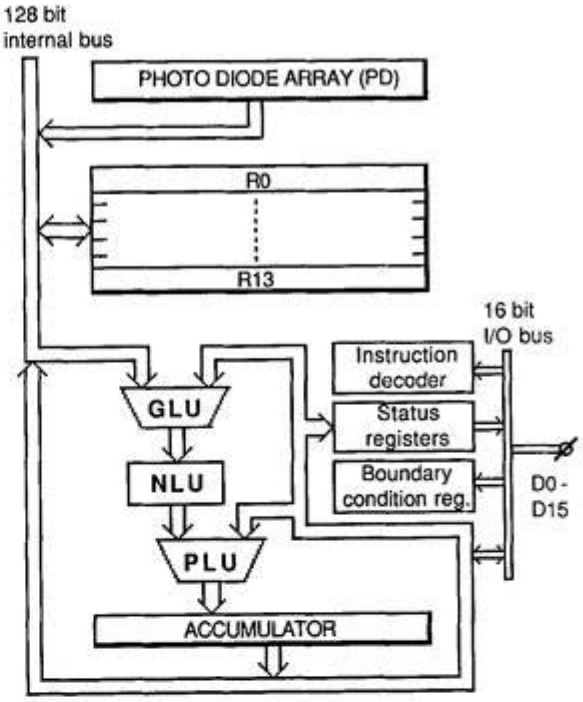

Fig. 2. The block diagram of the LAPP.

2.1.1. Photo-Diode and Comparator Array (PD). The photosensitive diode array consists of a linear set of diodes, pre-charge transistors and comparators as shown in figure 3. The active surface of each of the diodes is 35×35 μm^2 and the space between them is 50μm.

The diode is first reversely biased by pulsing the pre-charge transistor. The charged diode will then discharge