EXHIBIT 1038

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("the '820 Patent" or "WYLES")

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Wyles et al.

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[54] **FOCAL PLANE ARRAY READOUT EMPLOYING ONE CAPACITIVE FEEDBACK TRANSIMPEDANCE AMPLIFIER FOR EACH COLUMN**

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[51] **Int. Cl.**[5] **H04N 5/30**

[52] **U.S. Cl.** **358/213.28**; 250/208.1; 358/212; 358/213.27

[58] **Field of Search** 250/208.1; 358/213.12, 358/212, 213.28, 213.27

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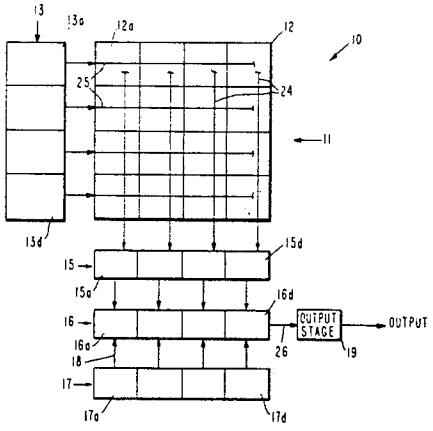
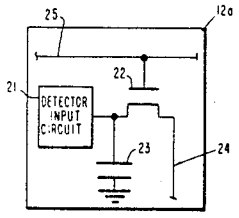
[57] **ABSTRACT**

A readout circuit for use with a focal plane array that employs a single transistor in each unit cell and a single capacitive feedback transimpedance amplifier to process the outputs of each column of detector elements of the array. The capacitive feedback transimpedance amplifiers extract the signals associated with the pixels along a particular row of the array. The present invention permits high performance readouts to be constructed with very little circuitry in the unit cells. Only a single minimum sized transistor switch is required in each unit cell to perform readout and reset functions for the array. In the disclosed embodiment, the readout circuit comprises an array of unit cells, each cell comprising a detector input circuit, a single transistor and a single charge storage capacitor. Row address circuits are coupled to the cells in each row of the array. A plurality of capacitive feedback transimpedance amplifiers are coupled to the cells in each column of the array. The amplifiers process charge derived from the detector elements and stored in the charge storage capacitor of each unit cell. Column multiplexing circuits multiplex the output signals provided by each of the amplifiers. Column address circuits are coupled to the column multiplexing circuits which couple output signals from each of the multiplexer circuits as the output from the readout circuit.

15 Claims, 2 Drawing Sheets





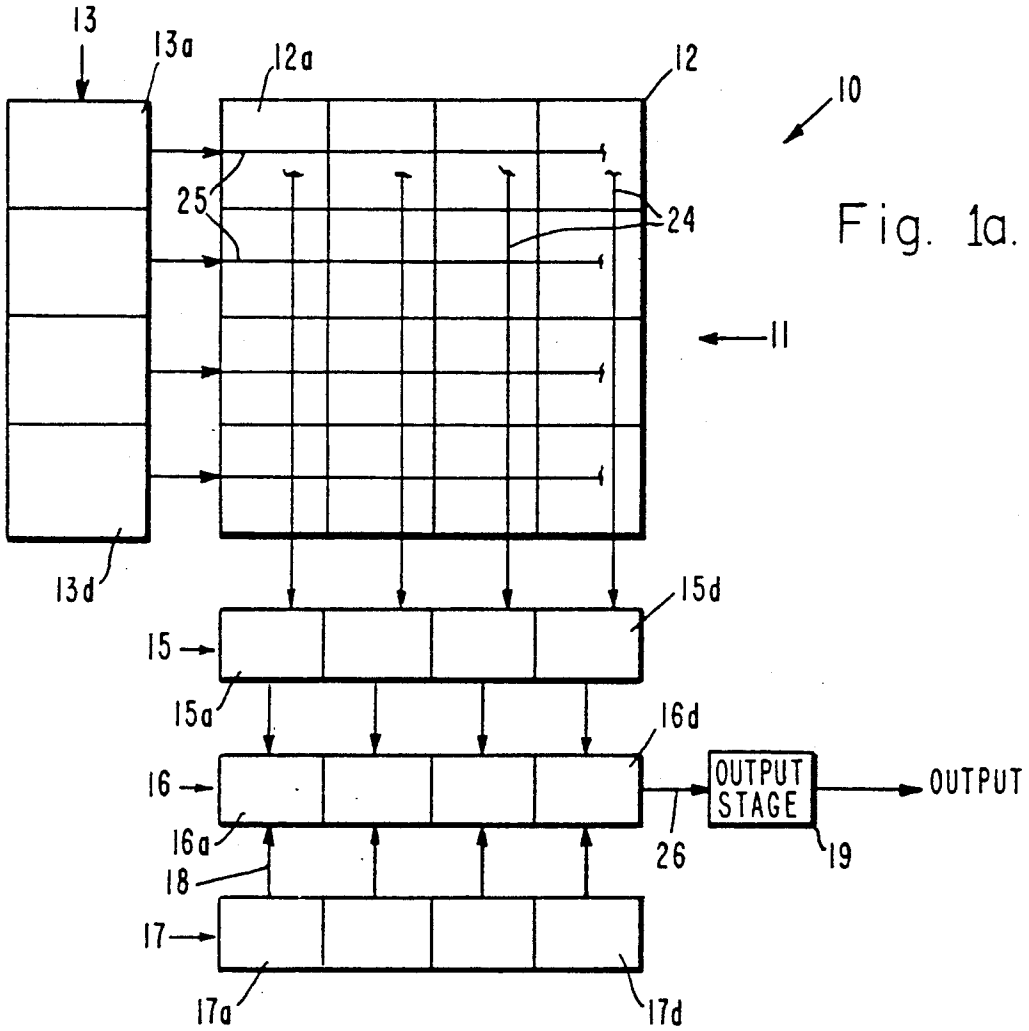


Fig. 1a.

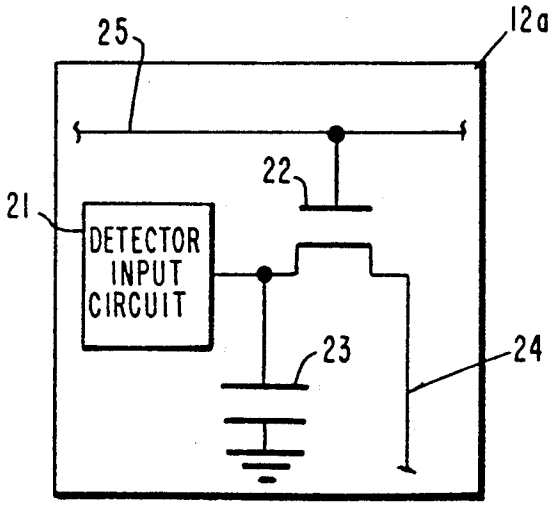
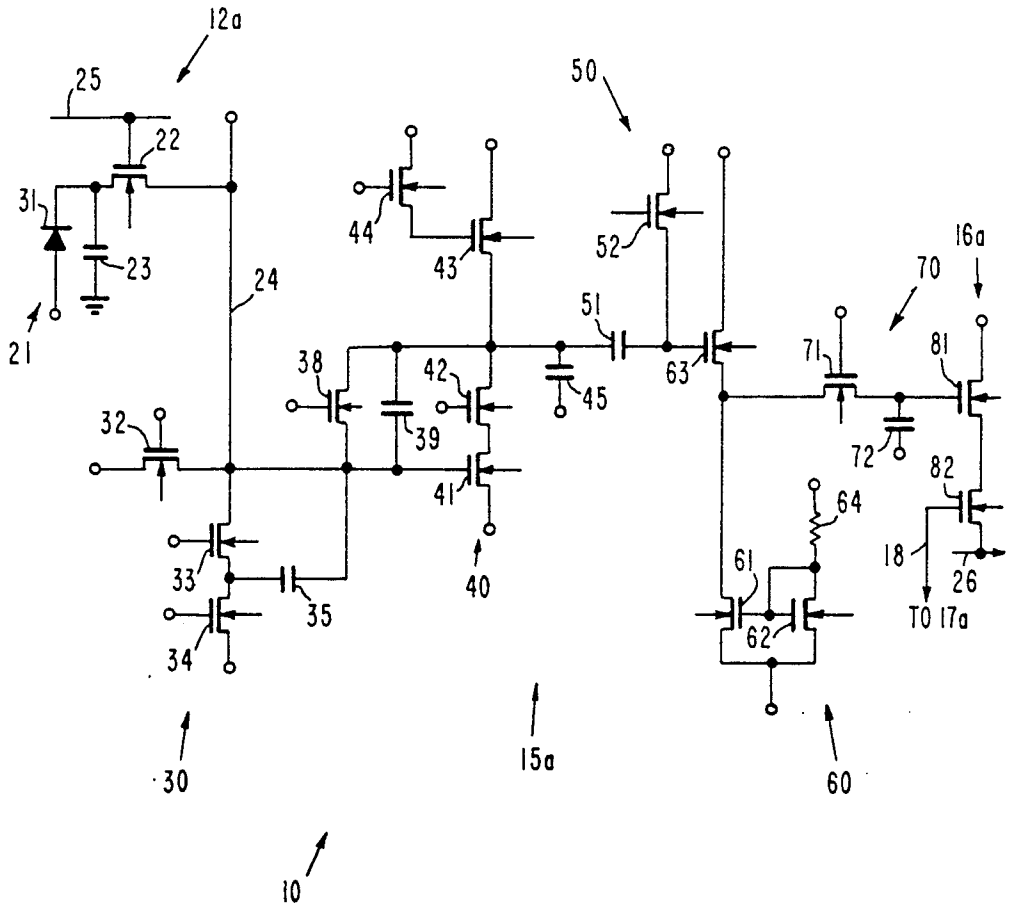


Fig. 1b.

Fig. 2.



FOCAL PLANE ARRAY READOUT EMPLOYING ONE CAPACITIVE FEEDBACK TRANSIMPEDANCE AMPLIFIER FOR EACH COLUMN

BACKGROUND

The present invention generally relates to focal plane arrays and more particularly to a focal plane array readout that employs a single capacitive feedback transimpedance amplifier for each column in the focal plane array.

Existing high performance direct readout devices for focal plane arrays generally require several transistors in each unit cell, a unit cell being the circuit that stores charge from the detector elements of the focal plane array. Typically the number of transistors employed in the unit cell is four. Consequently, it is generally not possible to build monolithic focal plane arrays with small unit cells and high fill factors, meaning the ratio of detector area to total unit cell area. For hybrid focal plane arrays, input circuit performance is generally compromised using such conventional circuits. Charge coupled device readouts also require large amounts of space in the unit cell, and therefore have similar drawbacks.

Readout devices have been developed which require only two transistors in the unit cell. Such devices are described in a publication entitled "A Solid State Color Video Camera with a Horizontal Readout MOS Imager," authored by Masaru Noda, et al, published in IEEE Transactions on consumer Electronics, Vol. CE-32, No. 3, August 1986. In addition to requiring more space in the unit cell this approach requires a very high speed amplifier with low noise, a combination that is very difficult to achieve in practice.

Single transistor unit cells have been used in the past for reading out photodiode arrays. However, the reported devices have employed signal extraction circuitry, such as feedback enhanced direct injection circuits, whose noise performance is somewhat less than desirable. Typical of such single transistor unit cells are those referenced in "Design Consideration and Performance of a New MOS Imaging Device," authored by Haruhisa Ando, et al, in IEEE Transactions on Electron Devices, Vol ED-32, No. 8, August 1985.

SUMMARY OF THE INVENTION

In order to overcome some of the limitations of conventional focal plane readout devices, including relatively large unit cells and less than desirable circuit performance, the present invention provides for a readout device that employs a single transistor in each unit cell. In addition, a single capacitive feedback transimpedance amplifier is employed to process the outputs of each column of detector elements of the array. The capacitive feedback transimpedance amplifiers extract the signals associated with the pixels along a particular row of the array.

The present invention permits high performance readouts to be constructed with very little circuitry in the unit cells. Only a single minimum sized transistor switch is required in each unit cell to perform the readout and reset functions for the array. The remaining space in the unit cell is available to achieve high detector fill factors in monolithic focal plane arrays, or improved input circuit performance in hybrid focal plane arrays.

More specifically, in the disclosed embodiment, the present invention comprises a readout circuit for use with a focal plane array of detector elements. The readout circuit comprises an array of unit cells, each cell comprising a detector input circuit, a single transistor and a single charge storage capacitor. A plurality of row address circuits are individually coupled to the cells in a respective rows of the array. A plurality of capacitive feedback transimpedance amplifiers are individually coupled to the cells in a respective columns of the array. The amplifiers process charge derived from the detector elements and stored in the charge storage capacitor of each unit cell.

A plurality of column multiplexing circuits are coupled to respective ones of the capacitive feedback transimpedance amplifiers which multiplex the output signals provided by each of the amplifiers. A plurality of column address circuits are respectively coupled to the column multiplexing circuits which couple output signals from each of the multiplexer circuits as the output from the readout circuit.

BRIEF DESCRIPTION OF THE DRAWING

The various features and advantages of the present invention may be more readily understood with reference to the following detailed description taken in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and in which:

FIG. **1***a* shows a block diagram of a focal plane array readout circuit in accordance with the principles of the present invention;

FIG. **1***b* shows a diagram of a unit cell of the readout circuit of FIG. **1***a*; and

FIG. **2** shows a detailed diagram of a capacitive feedback transimpedance amplifier and unit cell employed in a focal plane array readout circuit in accordance with the principles of the present invention.

DETAILED DESCRIPTION

Referring to FIG. **1***a*, a block diagram of a focal plane array readout circuit **10** in accordance with the principles of the present invention is shown. The readout circuit **10** comprises an array **11** of unit cells **12**, shown in FIG. **1***a* as a 4×4 array of cells. Row address circuitry **13** comprising a plurality of row (Y) address circuits **13***a*–**13***d*, are coupled to each of the cells **11** in a particular row of the array **11**. The specific interconnection to the cells **12** will be described with reference to FIG. **1***b*.

With reference to FIG. **1***b*, a diagram of a unit cell of the readout device **10** of FIG. **1***a* is shown. The unit cell **12** comprises a detector input circuit **21**, whose input is coupled to a detector element in the focal plane array, and whose output is coupled through a unit cell transistor **22** which operates as a switch. A charge storage capacitor **23** is coupled from a point between the detector input circuit **21** and the transistor **22** and ground. The gate of the transistor **22** is coupled to a selected row address circuit **13***a*–**13***d* employed to address the row in which the particular cell **12** resides along a horizontal signal line **25**. The drain of the transistor **22** is coupled to a vertical signal line **24** which couples charge out of the unit cell **12**.

Referring again to FIG. **1***a*, the vertical signal lines of each column of the array are respectively coupled to

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