EXHIBIT 1029

T. Ozaki, *et al*., "A Low-Noise Line-Amplified MOS Imaging Devices",

IEEE Transactions on Electron Devices, Vol. 38, No. 5 (May 1991)

TRW Automotive U.S. LLC: EXHIBIT 1029
PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NUMBER 8,599,001
IPR2015-00436

A Low-Noise Line-Amplified MOS Imaging Devices

Toshifumi Ozaki, Hajime Kinugasa, and Takashi Nishida

***Abstract*—A new MOS imaging device is proposed. It has an amplifier and a correlated double sampling (CDS) circuit at each vertical signal line and an offchip smear differential gear. The 1/2-in image format, 500 × 485 pixels, is designed on 1.5-μm CMOS technology and its fundamental characteristics are analyzed. Random noise is 120 pA, and the aperture ratio is greater than 70%. The smear level is 100 dB. The fixed pattern noise is 2000 pA in the dark, 0.62% in light. Some advantages of this device include a 5-V power supply requirement, a high saturation current, a high signal-to-random-noise ratio and a low smear level. However, the fixed pattern noise in the dark must to be lowered.**

I. Introduction

Solid-state imaging devices have been widely used for home video cameras. However, there is a great need to reduce the image format, thereby making the camera more compact. Conversely, future high-definition TV systems will require 5 to 8 times as many pixels as current devices contain [1]–[4]. In order to meet these requirements, the size of each pixel element needs to be reduced to allow for a higher pixel density.

There are two types of imaging devices: a CCD type and an *X–Y* addressable MOS type. Currently, an interline-CCD [5], [6] is mainly used commercially because of its low random noise characteristics. In the CCD device, however, the photodiode and vertical transfer structure exist on the same plane. As a result, two problems prevent a reduction of the pixel size, even if fine process technology were used. First, the area of the vertical-transfer structure cannot be reduced since it must be capable of storing the charge for a saturated signal. Secondly, the isolation length between the vertical-transfer structure and photodiode must be preserved in order to maintain the smear level.

A pixel of an *X–Y* addressable MOS sensor [7], [8] could be scaled down by implementing a smaller process technology. There would be no similar problems as those encountered with the interline CCD. However, parasitic capacitance of a signal line does cause a 10 times greater random noise level than in CCD. Accordingly, the authors propose a new *X–Y* address MOS type device to improve random noise characteristics. This device differs from the conventional MOS sensor in that is has an amplifier and a correlated double sampling (CDS) circuit [9] for each vertical signal line. This device is called Line-Amplified-MOS Imaging Device (LAM). Section II describes the circuit configuration and operation. After the analysis of random noise and design considerations, the new structure's effect on random noise is discussed in Section III. Methods for suppression of smear, which prevent pixel size reduction, are presented in Section IV. In Section V, the fixed pattern noise introduced by the LAM device is discussed in terms of its origin and suppression method. Finally, the results of the analysis are summarized in Section VI. The analyzed values are for a 1/2-in, 500 × 485 image sensor built on 1.5-μm CMOS process.

Manuscript received May 22, 1990; revised September 27, 1990.

T. Ozaki and T. Nishida are with the Central Research Laboratory, Hitachi Ltd., Kokubunji, Tokyo 185, Japan.

H. Kinugasa is with Hitachi Device Engineering, Co., Ltd., Mobara, Chiba 297, Japan.

IEEE Log Number 9142978.

II. Configuration and Operation

A schematic diagram of LAM is given in Fig. 1. Similarly to a conventional MOS device [7], the photodiode is addressed by a vertical scanner, which scans the vertical switch, and a horizontal scanner, which scans the horizontal switch. In addition, LAM has a line amplifier and a CDS circuit [9] at each vertical signal line and off-chip smear differential gear [10].

The circuit diagram of the signal readout path and clock timing is shown in Fig. 2. LAM operates in the following sequence:

1) $t = t_1$–t_4: In the first increment of horizontal blanking time, smear reads out to memory capacitance C_{M1}.

$t = t_1$: Switch S_1 is on to reset the vertical signal-line capacitance C_V.

$t = t_2$: Switch S_1 is off to activate the line amplifier. At the same time, KTC noise generates on the vertical signal-line capacitance C_V.

$t = t_3$: Switch S_2 is off to activate the source-follower. Smear without KTC noise is transferred to memory capacitance C_{M1} through coupling capacitance C_C (clamp).

$t = t_4$: Switch S_3 is off and smear has been held on the memory capacitance C_{M1} (sample-and-hold).

2) $t = t_5$-t_9: The second increment of horizontal blanking time is similar to the first increment, except that the signal with smear is now read out to memory capacitance C_{M2}. In this case, the vertical switch S_{PD} is on at time t_7.

3) During the horizontal scanning period, switches S_{R1} and S_{H1} are sequentially enabled together to read out smear from memory capacitance C_{M1} through the output source-follower. Then, after one horizontal clock delay, the signal with smear is read out in the same way by enabling S_{R2} and S_{H2}.

4) After the smear charge is delayed one horizontal

0018-9383/91/0500-0969$01.00

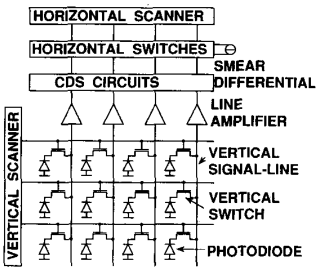

Fig. 1. Schematic diagram of the line-amplified MOS imaging device.

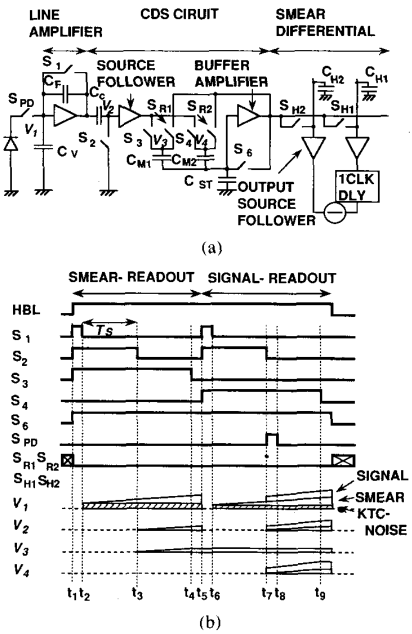

Fig. 2. Basic operation of LAM. (a) Circuit diagram of signal readout path. (b) Clock timing and voltage of each node.

clock, the smear-only charge and the signal with smear charge are differentiated to obtain just the signal charge.

LAM's configuration and operation offers many advantages including:

1) a photosite of a high aperture ratio (more than 70%); a pixel consisting of one photodiode and one switch;
2) low random noise; the line amplifier leads to 1/5 input capacitance and 1/6 noise band compared to a conventional MOS device [7], [8]: the CDS circuit cancels the KTC noise;
3) low smear; smear merges into the signal in only one sampling period T_s, which is 1/60 as short as the conventional value [7]; an off-chip smear differential gear separates smear from the signal.

The configuration of each amplifier is shown in Fig. 3. The line amplifier consists of a cascoded CMOS inverting amplifier [14] due to high voltage gain. The PMOS driver of the source-follower is formed in a separate well which is connected to the output. As a result, the circuit is free from body effect and its voltage gain is unity. The buffer amplifier consists of a CMOS inverter with an NMOS driver. The output source-follower has the same circuit configuration as the source-follower.

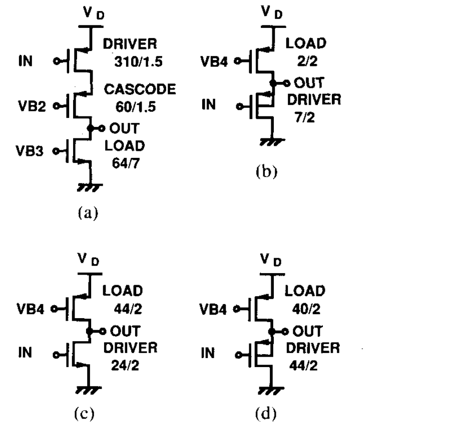

Fig. 3. Amplifiers. The channel width (W) and length (L) is indicated in micrometers for each device (W/L). V_{B2}, V_{B3}, V_{B4} are bias voltages. (a) Line amplifier. (b) Source-follower. (c) Buffer amplifier. (d) Output source-follower.

III. Random Noise

In this section, random noise is analyzed. Based on the results, design methods to reduce random noise are considered. Finally, noise values are presented.

A. Theoretical Analysis

LAM has the following two noise origins: one is from a MOS transistor in each amplifier and the other comes from each switch when the switch is off. The noise voltages referred to the input of each line amplifier V_{RNA} can be expressed as

$$V_{RNA} = \int_0^{f_c} 2\, F_l F_A S_f \sum_{i=1}^{n} \sum_{j=1}^{n} I_i I_j \cos 2\pi f T_A (I_i - I_j)\, df. \tag{1}$$

In (1), S_f is the noise power spectrum density of the MOS transistor referred to the input of the transistor [11], [12]. F_A is the reference coefficient from the input of the transistor to the input of the amplifier [11]. F_l is the reference coefficient from the input of the amplifier to the input of the line amplifier. T_A is the sampling period of the amplifier output, and n is the sampling number of the amplifier output in one readout sequence. I_i is the arithmetic sign in the signal of the sampled output of the amplifier (+ or −) and f_c is the noise bandwidth when the output of the amplifier is sampled.

Otherwise, the noise voltage referred to the input of the line amplifier of each switch V_{NRS} can be given as

$$V_{NRS} = F_R n_R KT/C_R. \tag{2}$$

TABLE I
RANDOM NOISE SUPPRESSION METHODS

Source	Suppression Method	Reference Coefficient F_I
Noise form MOS Transistor in Each Amplifier		
Line amplifier	—	1
Source-follower	line amplifier	$1/G_F^2$
Buffer amplifier	line amplifier	$1/G_F^2$
Output source-follower	line amplifier	$1/G_F^2$
Noise from Each Switch		
Source	Suppression Method	Reference Coefficient F_R
S_1 (C_V)	CDS circuit	$\exp(-4\pi f_{CF} T_s)$
S_2 (C_C)	line amplifier	$1/G_F^2$
S_3 (C_{M1}), S_4 (C_{M2})	line amplifier	$1/G_F^2$
S_6 (C_{ST})	line amplifier differential	$1/G_F^2 \exp(-D/10)$
S_{H1} (C_{H1}), S_{H2} (C_{H2})	line amplifier	$1/G_F^2$

G_F Gain of line amplifier
T_s Sampling period.
f_{CF} Cutoff frequency for line amplifier.
D Differential factor.
( ) Reset capacitance

In (2), C_R is the value of the capacitance which is reset by the switch, K is Bolzmann's constant, and T is absolute temperature. F_R is the reference coefficient from the input of reset capacitance to the input of the line amplifier, and n_R is the switching number of the switch in one readout sequence.

Since signal is expressed as charge in an imaging device, noise should also be expressed in charge or current. Thus noise voltage V_N is converted to noise current I_N by

$$I_N = V_N C_V \sqrt{2 f_H f_B}. \tag{3}$$

In (3), C_V is the capacitance value at the input of the line amplifier, f_H is the driving frequency of the horizontal scanner, and f_B is signal bandwidth at the device output.

B. Design Consideration

The reference coefficients F_I, F_R, which are given in Table I, express the response of the total circuit to each noise source. The voltage gain of the souce-follower and buffer are assumed to be 1. Since the line amplifier has a high voltage gain G_F (45 in design), noises other than from the line amplifier and switch S_1 can be negligibly small. Moreover, the CDS circuit reduces the reset noise of switch S_1 by choosing a cutoff frequency f_{CF} just wide enough for the line amplifier. Accordingly, the main source of LAM is the line amplifier.

Ordinary noise voltage decreases as noise band decreases [13]. Thus the noise bandwidth f_C of the line amplifier is limited, as shown in Fig. 4. When switch S_2 is off, the noise below the cutoff frequency $1/2\pi R_{S2} C_C$ of the high-pass filter, which consists of the coupling capacitances C_C and the on-resistance of switch S_2, is clamped and merged into one signal. When switch S_3 or S_4 is off, the noise below the cutoff frequency $1/2\pi R_{S3} C_M$ of the low-pass filter, which consists of the memory capacitance C_M and the on-resistance of switch S_3 or S_4, is sampled and held and then merged into one signal. Since readout to memory capacitance C_M is done in the horizontal blanking period of about 10 μs, each sampling interval can be selected at 1 μs. According to the Nyquist criterion, these cutoff frequencies are designed to be 500 kHz. Moreover, switch S_3 and S_4 contain a complementery MOS transistor to prevent variation of on-resistance associated with signal level variation.

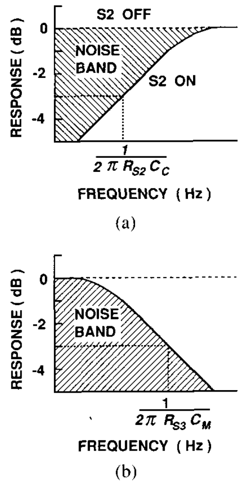

Fig. 4. Random noise band for line amplifier output, (a) when switch S_2 is off (clamp), (b) when switch S_3 is off (sample and hold). R_{S2}, R_{S3} are, respectively, the on-resistance of switches S_2, S_3. C_C is coupling capacitance and C_M is memory capacitance.

The reference coefficient F_A of each transistor of the line amplifier is, respectively, given by

$$1, \quad \text{for the driver} \tag{4a}$$

$$(g_{mL}/g_{mD})^2, \quad \text{for the load} \tag{4b}$$

$$0, \quad \text{for the cascode.} \tag{4c}$$

Here, g_{mD} is the transconductance of the driver and g_{mL} is the transconductance of the load. The transconductance of the load can be made much lower than the driver's without strongly affecting circuit performance. So, the driver is the primary noise source.

A MOS transistor has two noise origins: thermal noise and $1/f$ noise. Noise power spectrum density S_f [11], [12] is proportional, respectively, to one over the square root of the ratio of channel width to channel length (current I constant) and to one over the channel area. Accordingly, its noise voltage can be reduced by using the minimum channel length and a wide channel width. In the case of the driver, however, the total input capacitance of the line amplifier, including the gate capacitance of the driver, increases as the channel width increases. So, signal voltage is also reduced and a minimum random noise current is

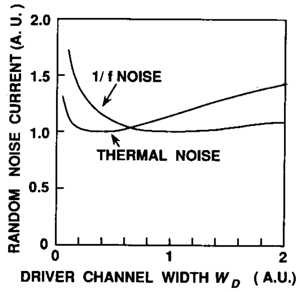

Fig. 5. Driver channel width dependence of random noise current in line amplifier.

reached. The dependence of the noise current on the driver channel width is shown in Fig. 5. The noise current that is generated by $1/f$ noise has a minimum value at the point where the gate capacitance of the driver $C_G W_D(L_D + 2X_j)$ is equal to the vertical signal line capacitance C_{VO}. W_D is the channel width of the driver; L_D is the effective channel length of the driver; C_G is the unit gate capacitance; and X_j is the depth of the diffused layer. The noise current that is generated by thermal noise reaches a minimum value at a channel width of $1/3$.

Finally, the transistor type is considered. The minimum current of the driver is calculated for the NMOS driver and PMOS driver, as shown in Fig. 6. Here, μ is the mobility, n_{TE} is the effective trap density of $1/f$ noise, and γ is the inclination of $1/f$ noise power spectrum [12], which is obtained from experiment. Thermal noise is higher in the PMOS driver than in the NMOS driver due to the lower mobility. However, $1/f$ noise, though, is lower in PMOS driver due to the higher inclination of $1/f$ noise power spectrum. Since total noise at a sampling period of 1 μs is lower in the PMOS driver, it is selected and the gate capacitance was designed to be $1/3$ of the vertical signal capacitance to minimize thermal noise.

C. Random Noise Value

The calculated random noise value for each noise source is shown in Table II. The total noise of the LAM is 120 pA, which is about four times as large as the interline CCD's (30 pA) [6]. However, the aperture of LAM (71%) is about three times as large as that of the interline-CCD (24%) [6]. Therefore, the signal-to-noise ratio in LAM is about the same as in the interline CCD.

IV. Smear

When pixel size is scaled down, smear increases, due to a reduction of the isolation length. Thus suppression of smear is an important problem in solid-state imaging devices. In this section, methods for smear reduction are presented. A technique for widening the dynamic range, which enhances smear reduction, is also explained.

A. Methods for Smear Reduction

Smear in a MOS device is caused by the photo-generated carriers diffusing into the vertical signal line during the horizontal scanning period. In LAM, pixels are constructed on a p-type substrate to avoid voltage modulation [15] caused by parallel operation of the line amplifiers.

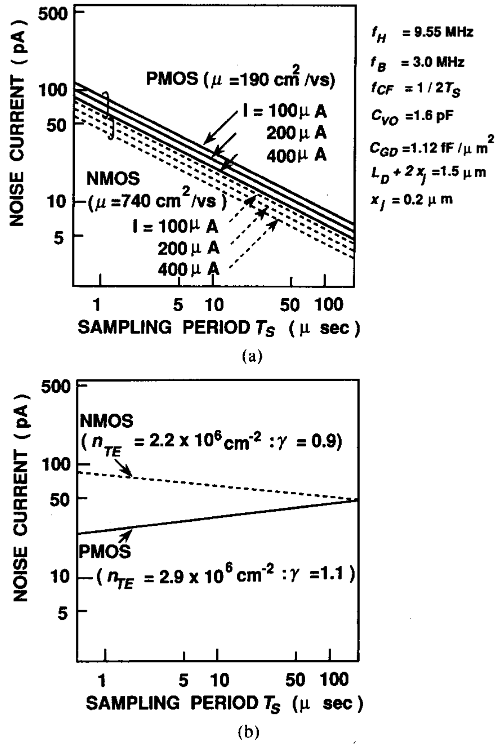

Fig. 6. Comparison of minimum random noise current for p-channel driver and n-channel driver in line amplifier. (a) Thermal noise. (b) $1/f$ noise. Noise band for line amplifier f_{CF} is assumed to be $1/2T_S$.

TABLE II
RANDOM NOISE CURRENT

Source		Thermal	$1/f$
Line amplifier	driver	59	30
	cascode	0	0
	load	37	61
Source-follower	driver	6.7	3.3
	load	4.9	4.2
Buffer amplifier	driver	7.6	13
	load	6.9	0.9
Output source-follower	driver	4.7	4.1
	load	4.9	4.1
Subtotal		71	70
S_1		43	
S_2		35	
$S_3 + S_4$		35	
S_6		7.1	
$S_{H1} + S_{H2}$		15	
Subtotal		67	
Total		120	

Units: picoamperes.

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.

WHAT WILL YOU BUILD? | sales@docketalarm.com | 1-866-77-FASTCASE