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ASIC IMAGE SENSORS

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§1 : ABSTRACT

This paper describes two image array sensors designed and fabricated using a standard 2 level metal ASIC CMOS process. The results show that *(i)* good quality, grey-level images can be formed and *(ii)* CMOS sensor arrays can be successfully integrated with efficient analogue sense amplifiers and with digital control/image processing logic. The first sensor is a proto-type 128×128 pixel test array. The second is a 312×287 pixel image sensor chip, which includes all the necessary circuitry to produce full PAL format video output, as well as automatic, electronic exposure control and built-in test circuits. Test results characterising the devices are also given, covering dynamic range, spectral response, sensitivity, resistance to blooming etc. Finally, some potential applications for such devices are mentioned.

§2 : INTRODUCTION

Solid state image sensors have been designed and demonstrated by various researchers and companies. Available devices e.g., [1,2,3] are capable of delivering good quality grey-level images. They use either CCD or photodiode array technologies, which are non-standard MOS processes. Imaging DRAM devices [4], using MOS memory processes, have also been demonstrated but are unsuitable for many applications, as they give binarized, rather than grey-level data. Other MOS sensors [9] require off chip sense and amplification circuitry. Some researchers have developed special purpose image sensors [5,6,8] using low cost ASIC CMOS processes. These devices, although very interesting architecturally and useful for single, specific functions, do not demonstrate good quality general-purpose grey-level image sensing capability.

A major disadvantage of all commercially available image sensors chips is their requirement for off-chip sense and/or amplification circuitry, for off-chip digital control circuitry, and for multiple supply voltage levels. The experimental work reported here demonstrates that good quality images can be obtained from devices fabricated on a standard, low-cost ASIC CMOS process, that they require very low power, single voltage supply and that the analogue and digital circuitry required to provide the complete sensor function can be integrated on the chip.

In a standard, low-cost ASIC CMOS process there are three possible photodetector device structures available : photoconductor, photo-diode and photo-transistor. Factors affecting the choice of device include device area, response time, and gain. The theory of operation of these devices and design using them are well documented [7]. Photoconductors are unsuited to use in array sensor devices, due to large area and slow response time. Comparing photodiode with phototransistor, the photodiode has advantages of simpler structure, smaller area and faster response time. The phototransistor benefits from greater gain but its use in array devices is complicated by inevitable device and operating condition variation. For these reasons the photodiode is the basic sensing element used in both designs.

§3 : SENSOR 1

- Design :- Our first CMOS sensor chip comprises a 128×128 pixel photodiode array, which includes all the address, sense and amplification circuitry necessary to provide a self-scanned 1 volt peak-to-peak grey-level output signal. The device was designed and built specifically to test the suitability of a standard CMOS ASIC process for image sensing, with the eventual aim of developing low-cost, low-power ASIC image processing and sensing chips.

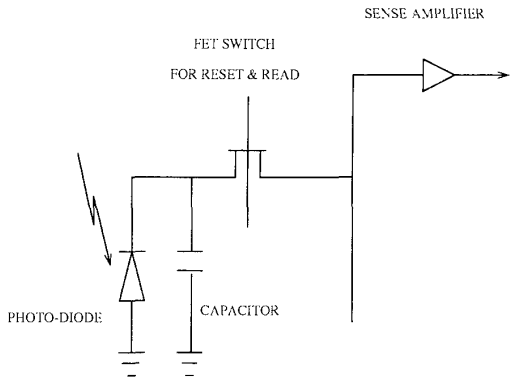

Figure 1 : CMOS sensor pixel & sense amplifier.

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The sensor circuit used is shown in *Figure 1*. In operation, the photodiode capacitor is reset to a voltage reference level V_{ref} by opening the FET switch. This stores a fixed charge on the capacitor. The photodiode and capacitor are then isolated. Photocurrent, produced by the effect of photons impinging on the diode, discharges the capacitor. The rate of discharge is proportional to the photocurrent, which is in turn proportional to the incident light level. The final charge retained on the capacitor, after a fixed time interval will represent the light intensity at that point of the image. Thus the photodiode must be accessed through the FET switch after a fixed time interval and the remaining charge sensed; this is the read operation. Key to the success of operation is the performance of the charge sensing function. Pixel design was contained by a 20μm pitch in both X and Y dimensions. (This may be tailored in application specific redesign.) The sensor architecture is shown in *Figure 2*.

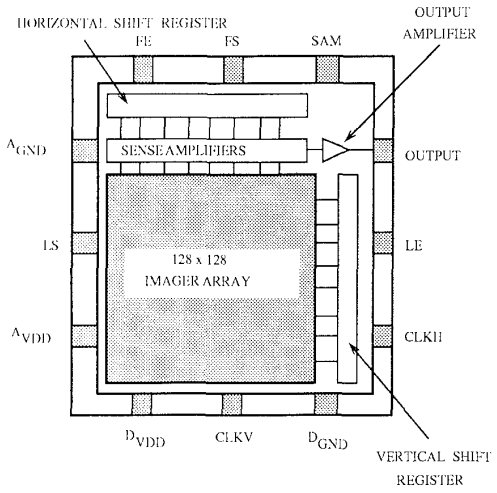

Figure 2 : CMOS sensor array architecture.

The pixels of a line of photodiodes are read and then reset in parallel. The row-read operation uses a row of sensitive charge integrators to perform the essential charge-sensing operation on-chip : a novel feature of this device. These sense amplifiers must be small enough to pitch-match the pixels, yet sensitive enough to give a good signal to noise ratio on the sensed signal; they must also be insensitive to at least the first order process parameter variations. The results of the read operation are held capacitively and then read out sequentially through an output amplifier, to give a line scan. Each line is accessed in sequence. (Alternative application specific redesigns could allow parallel read out of the full line, or part of it.) The chip is supplied with clock and initialisation signals and a single 5 volt supply. The read-out rate and exposure (integration) time are variable. The small active area (11 sq. mm.) allows for integration of other processing logic.

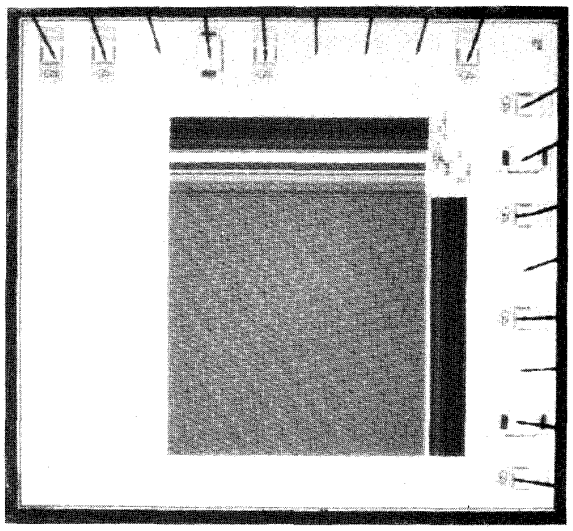

Figure 3 : Prototype CMOS 128×128 sensor array.

- Test and Characterisation Results :- The design was fabricated using ES2 2μm ASIC CMOS process. Samples (*Figure 3*) have been tested and characterised. Initial testing included display of visual images on an oscilloscope screen, for frame rates of 60 f.p.s. To evaluate the quality achievable on a conventional monitor display, (*Figures 4, 5*) a PC with enhanced VGA was used together with an ADC and dedicated RAM frame-store interface. The images obtained displayed unexpectedly good grey-level quality, with excellent uniformity.

Figure 4 : Grey-scale image formed by 128×128 pixel prototype sensor.

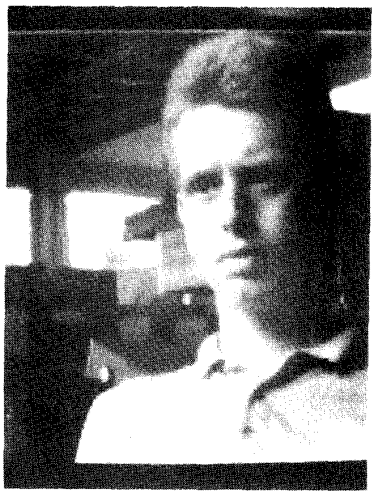

Figure 5 : Grey-scale image formed by 128×128 pixel prototype sensor.

In order to characterise the imager, an optical test measurement set-up, was used. *Table 1* (at the end of this paper) summarises the measured results of the performance characterisation experiments. There was no observable cross-talk, ghosting or smear. Anti-blooming performance is comparable with commercially available CCD and photodiode devices. Over-exposure on one frame has no measurable persistence effect on subsequent frames. The sensitivity and spectral response (*Figure 6*) are particularly well suited to the visible spectrum and exhibit only low ripple (probably due to effects in the passivation layer). Performance is well maintained over a range of operating supply voltages (3.5V - 12V) and temperatures. Notably the entire sensor system may be operated successfully from a single 5V supply.

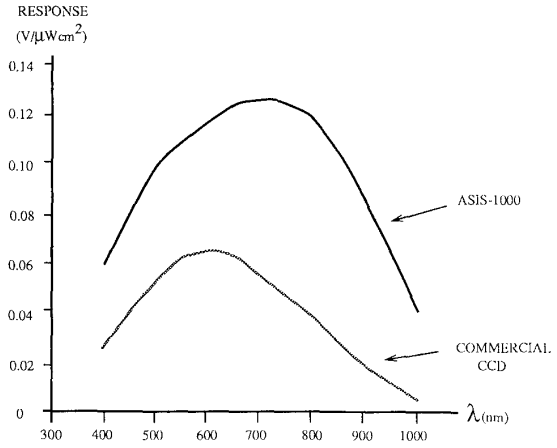

Figure 6 : Comparison of spectral response of 128×128 pixel prototype sensor with that of a commercial CCD device.

§4 : SENSOR 2

- Design :- The second sensor (*Figure 7*) has been designed to demonstrate the potential of ASIC CMOS for building fully integrated image sensor-processors. It comprises a 312×287 pixel photodiode array, similar to that in Sensor 1. In addition to the basic sense and control circuits used in sensor 1 there are circuits which provide the following functions:

1. 256×256 selected scan image output
2. full interlaced video format (CCITT) output
3. electronically adjustable exposure (via control of integration time)
4. automatic electronic control of exposure setting

These additional functions are provided through a 4,000 gate processor, adjacent to the sensor array. This device is, therefore, a single chip video camera : provided with a 5 volt power supply and focused light images it provides a black and white CCITT format video output. To our knowledge, all previously developed video imagers require one or more boards of surface mount components to achieve this. This design has been completed and is at present in fabrication. Details of the design and test results can be summarised at the Symposium.

§5 : CONCLUSIONS

The design and performance of ASIC CMOS VLSI image sensors has been reported here. Extension of the design to produce integrated ASIC sensor-processors has also been described. Their features of low cost processing technology, single low-voltage supply requirement, low power dissipation and potential for integration of digital logic demonstrate the viability of CMOS for single chip combined image sensing and processing devices. In the near future, as a development of this, we may expect to see an increasing number of products based on such technology. Applications would include security and surveillance cameras, remote sensing devices and special purpose image sensor-processors, where tailoring of the architecture of the sensor or its interface gives real advantages.

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TABLE 1

Parameter	Minimum	Nominal	Maximum	Units
Integration time	17.5		300	ms
Refresh rate	3.3		57	frames/sec
O/P voltage swing (peak to peak)		1.0		Volts
Operating voltage	3.5	5.0	12.0	Volts
Power dissipation		3.0		mW
SNR (measured)		51		dB
Blooming protection†		500×		
Dark current ‡		0.01		‡
Operating Temperature range	<-20	25	+80	°C

† Over-exposure which causes a small bright spot to form a detectable streak.
‡ Dark current, measured at 25°C, expressed as % of saturation exposure over an integration time of 20 msec.

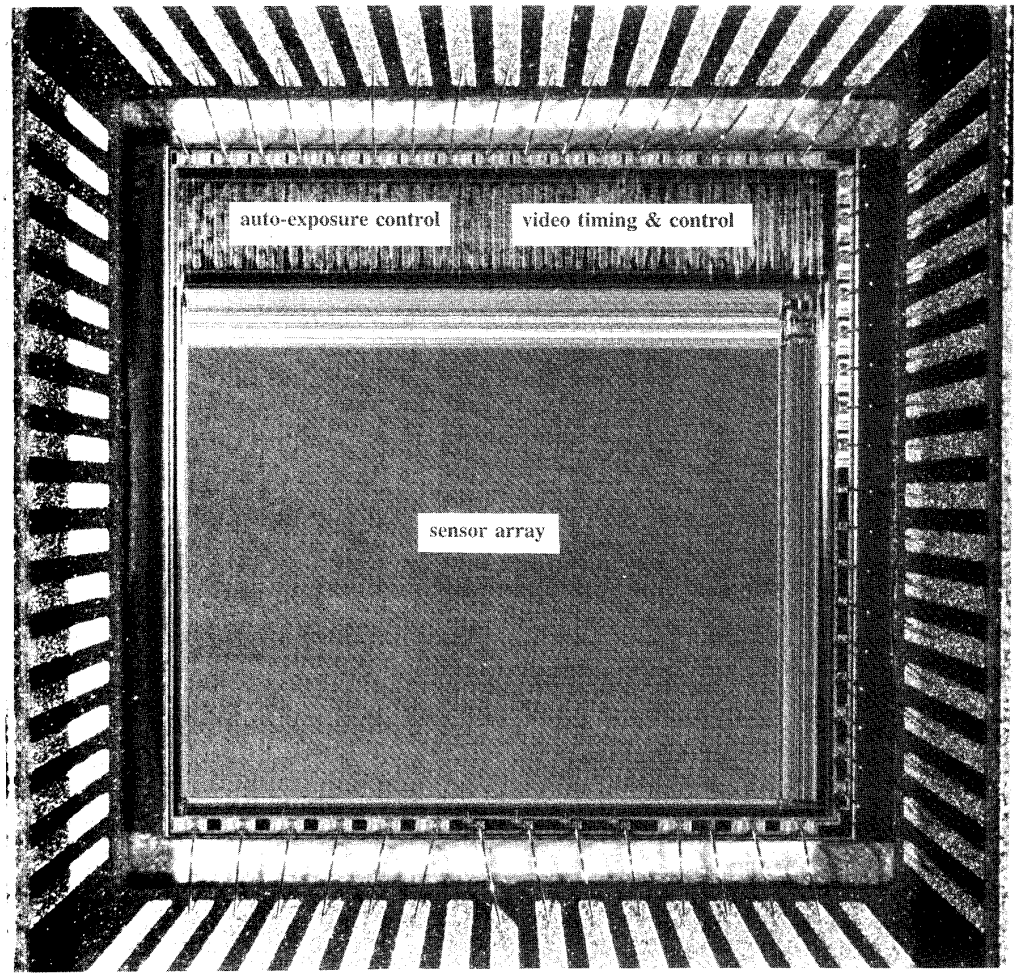

Figure 7 : Integrated ASIC camera chip